XDF XILINX DEVELOPER FORUM

Scaling FPGA Application Development

Presented By

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XILINX

The Need for Adaptable Intelligence

Everything Intelligent & Connected

Deployed at Global Scale

Dynamic Needs & Rapid Innovation

The intelligent connected world needs adaptable accelerated computing

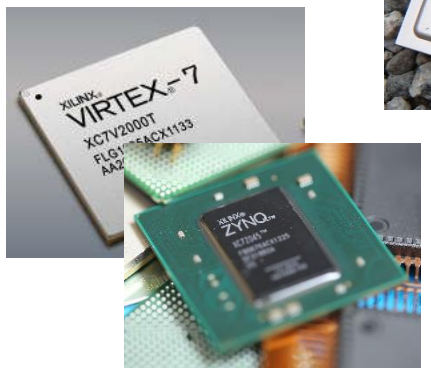
From Hardware to Software Programmable

World's
First FPGA

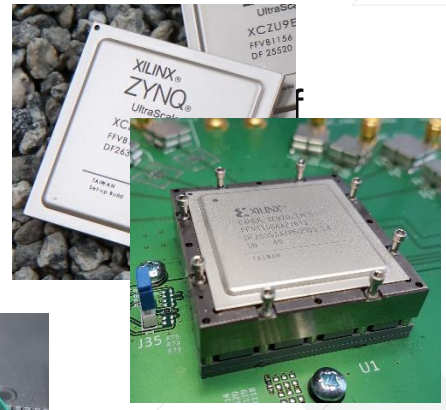
First
Virtex FPGA

Virtex-2 Pro

First 3D FPGA
& HW/SW
Programmable SoC



First
MPSoC & RFSoC



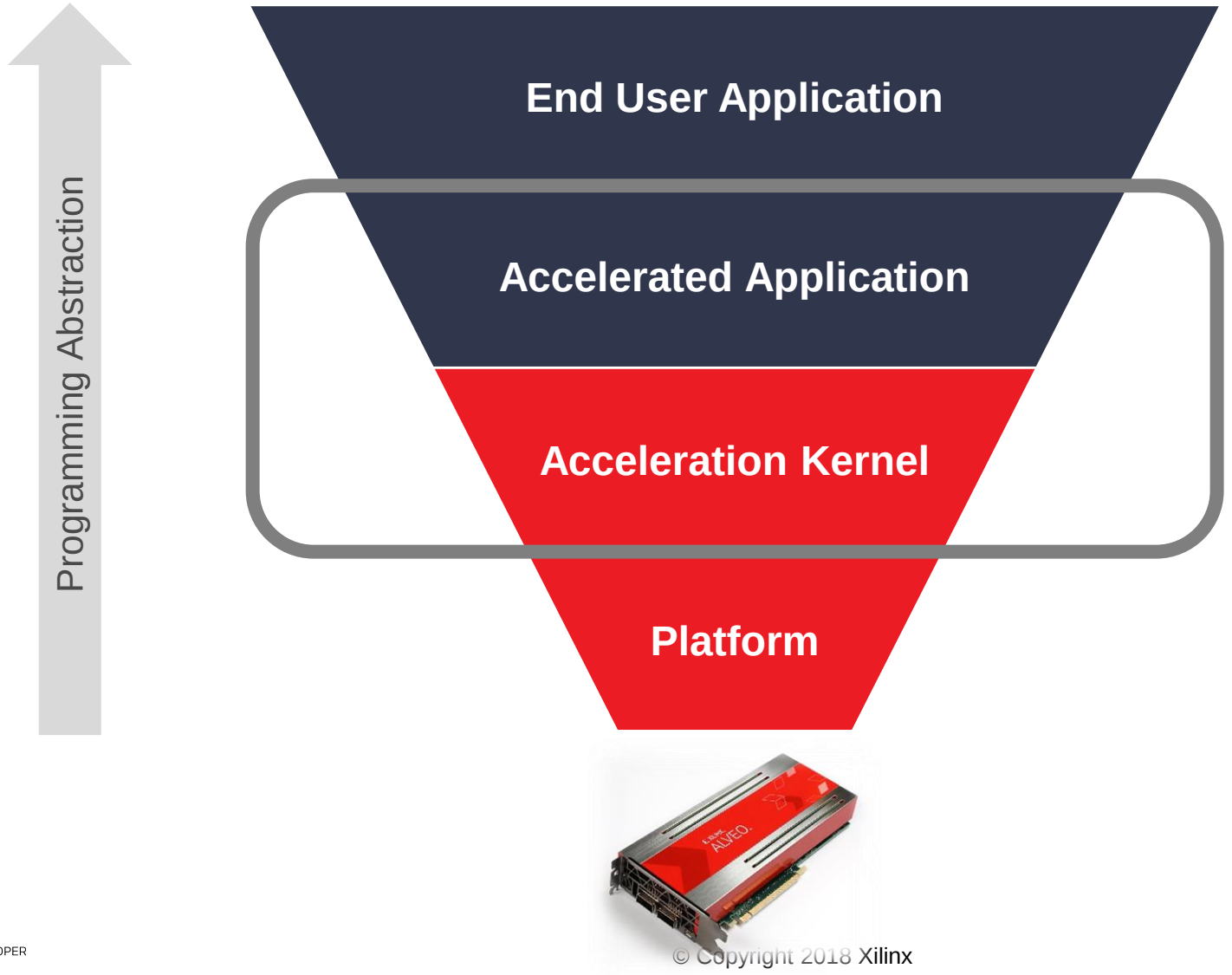
ACAP

1980 1990 2000 2010 2020

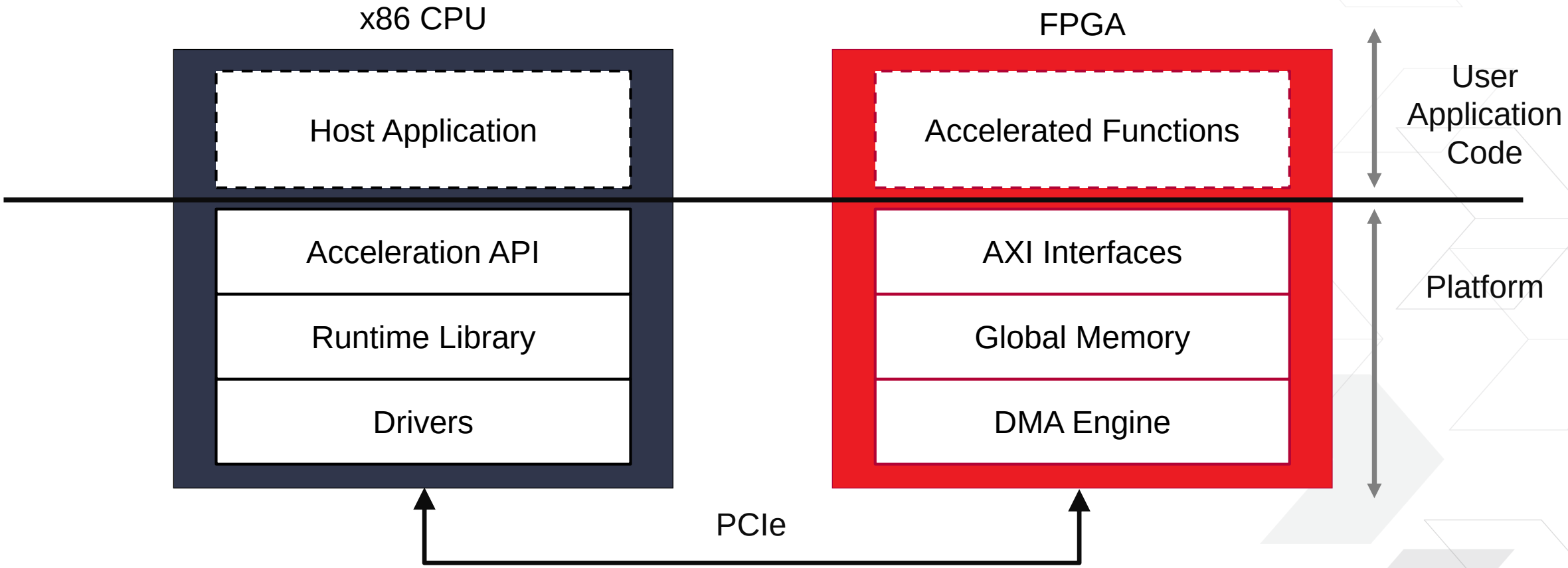
Software Programmability

How We Scale Application Development

The FPGA Software Programmability Stack



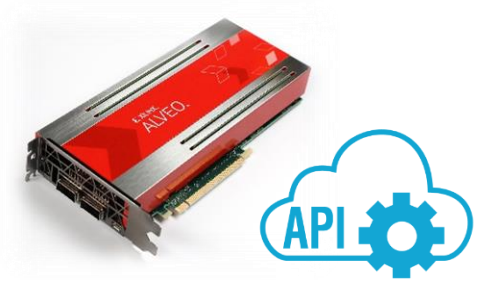
The Anatomy of an Accelerated Application



Explicit Execution Model Enabled by a Rich Runtime Library

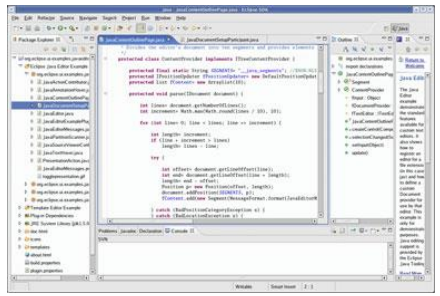
The Application Development Environment

SDAccel™ Environment



High Performance Platform and Runtime Library

Advanced FPGA Compiler

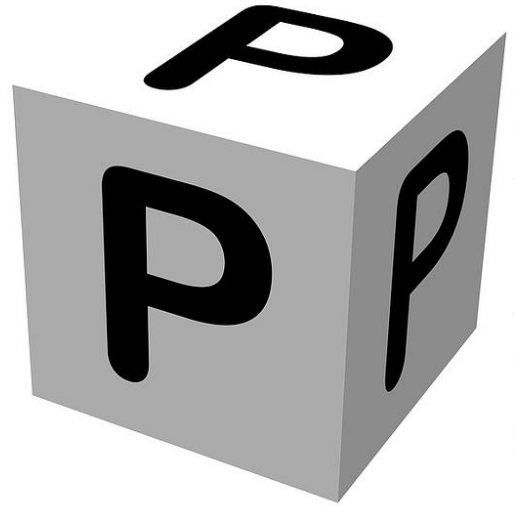


Productive IDE & Optimized Libraries

User Onboarding

The Benefits of SDAccel

- Platform and runtime library optimized for performance
- HLS or RTL for acceleration kernel
- Dedicated visualization, profiling and debug tools
- Optimized libraries
- Write once, deploy anywhere

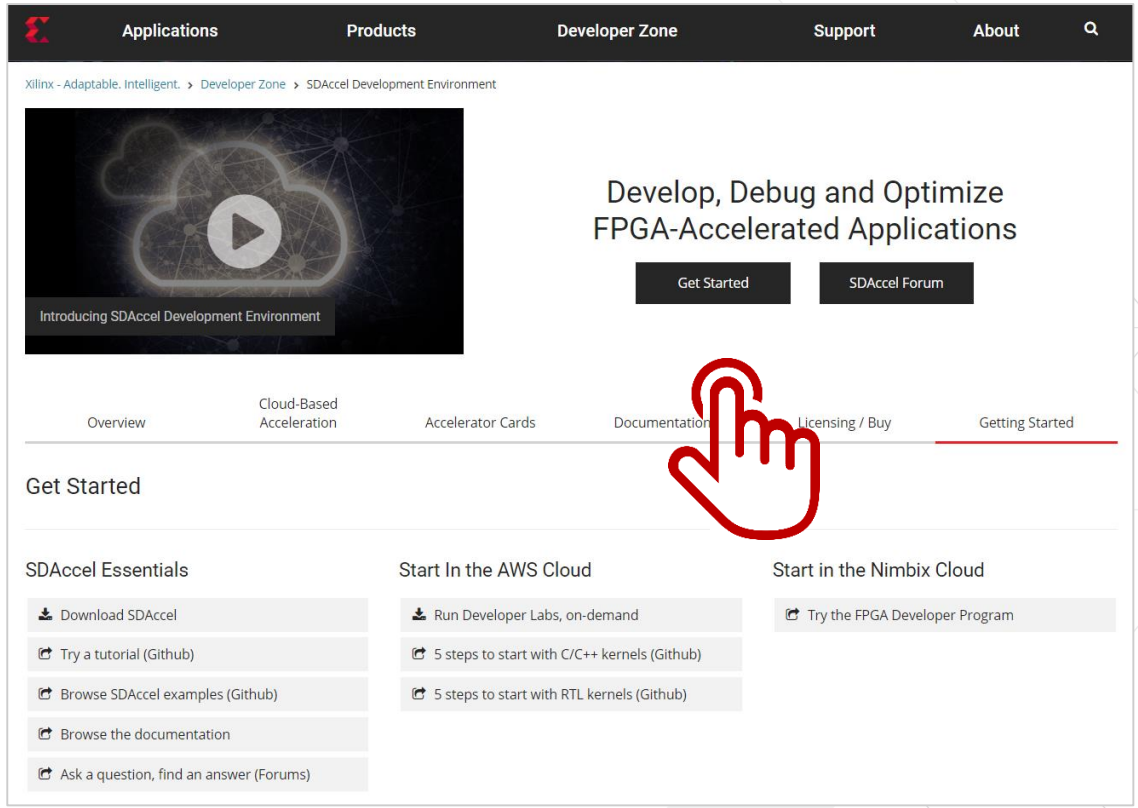


SDAccel™ Environment

Performance, Productivity, Portability

Scalability: Methodology, Onboarding and Support

- **Comprehensive "how-to" guides**
  - SDAccel Programmer's Guide
  - SDAccel Optimization Guide
  - SDAccel Debug Guide
- **Learn by practicing**
  - Over 50 examples to illustrate key concepts
  - Expanding set of tutorials, aligned with methodologies
- **Convenient access**
  - New "Getting Started" page
  - Groups all onboarding resources
  - On-premise and Cloud

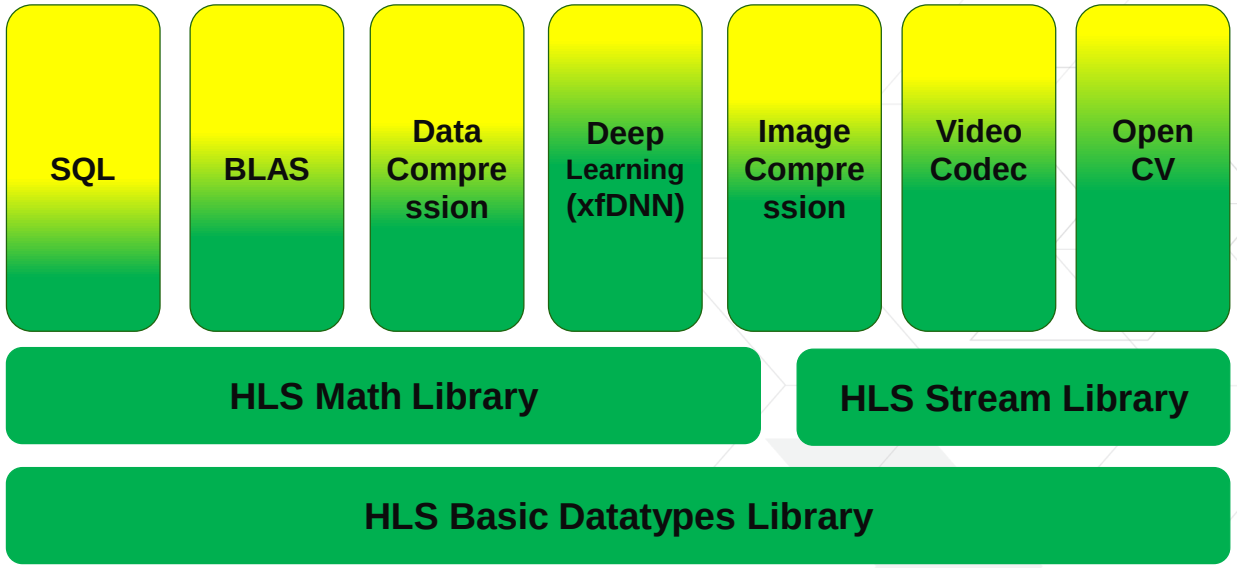


www.xilinx.com/sdaccel

Methodology is the Key to Success

Scalability: SDAccel Optimized Libraries

- **Rapidly expanding SDAccel portfolio**
  - Open Sourced whenever possible
- **Multiple levels of usage abstraction**
  - L1: HLS Interface for use inside kernel
  - L2: C/C+ API for use as kernel
  - L3: C/C++ API w/overlay architecture
- **Committed Investment by Xilinx**
  - Roadmap driven by customer demand



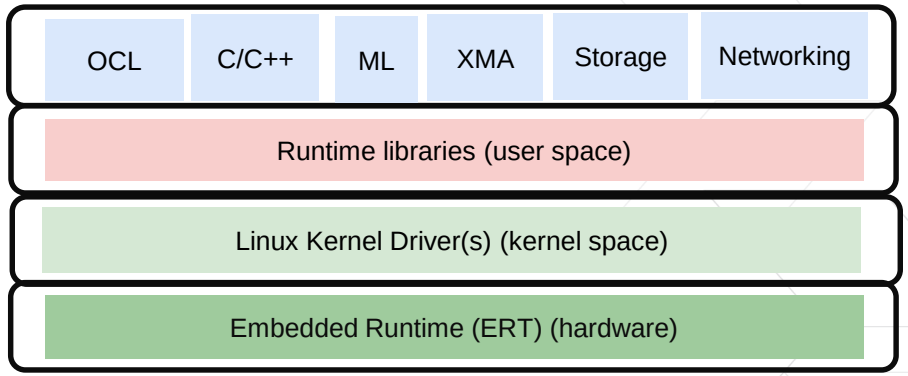
Roadmap: FinTech, Graph & Statistics

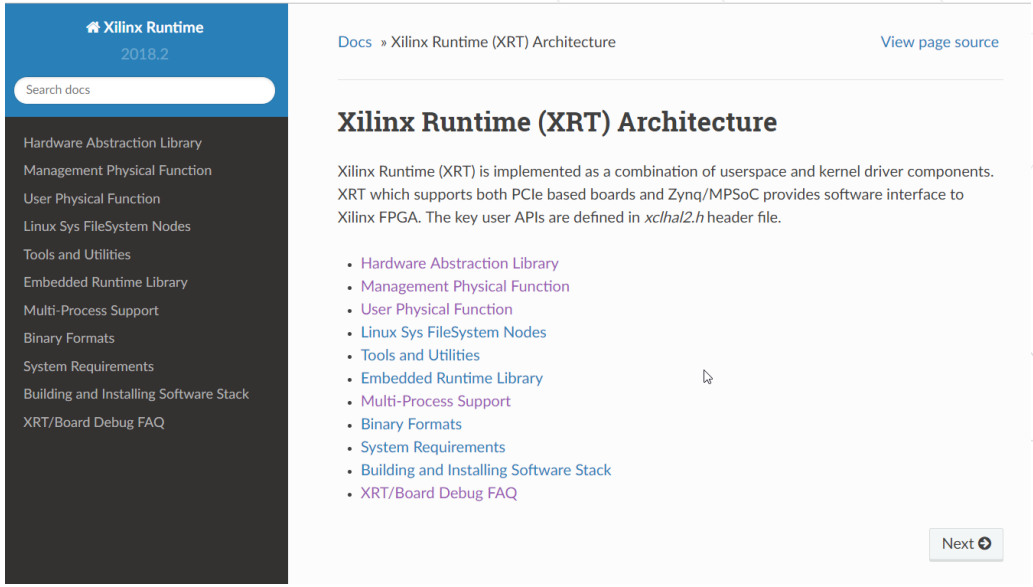
Scalability: Open Source Xilinx Runtime, Starting Today!

- **All XRT source code now available on GitHub!**
  https://github.com/Xilinx/XRT

- **Friendly License Terms**
  - Apache: User Space Libraries
  - GPL: Linux Kernel Drivers

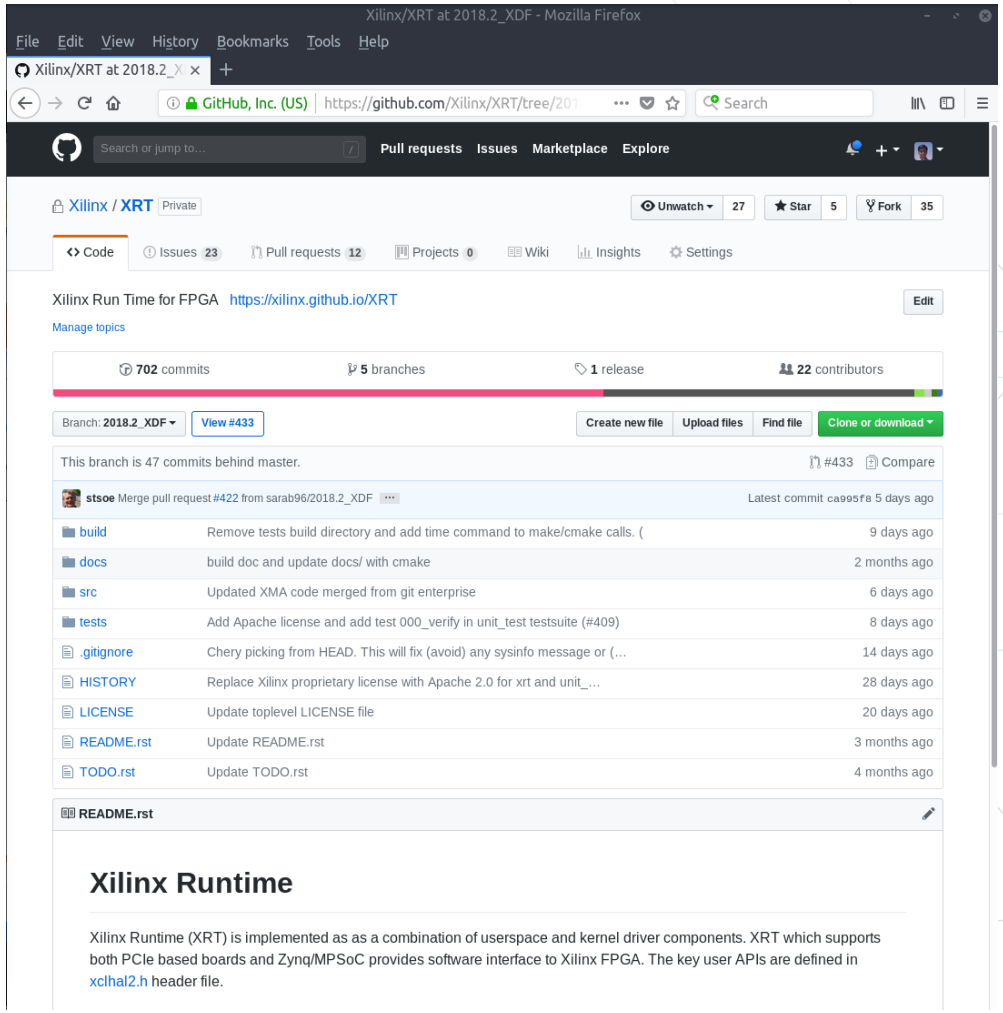
- **Full Commitment by Xilinx**
  - Well Documented
  - Validation Test Suite
  - Xilinx Gatekeeper





Xilinx Runtime Library – Why Open Source?

- **Foster Innovation**
  - Customers can focus on adding value on top of common components
  - Opens collaboration with Xilinx on evolving the FPGA runtime
- **Build Community**
  - An open Standard Runtime for FPGA acceleration
  - Leverage the “Power of Many"
- **Customers have been asking!**



Acceleration Case Study: SumUp Analytics

Company Summary

- SaaS solution targeting financial professionals providing topic extraction, summarization and sentiment analysis

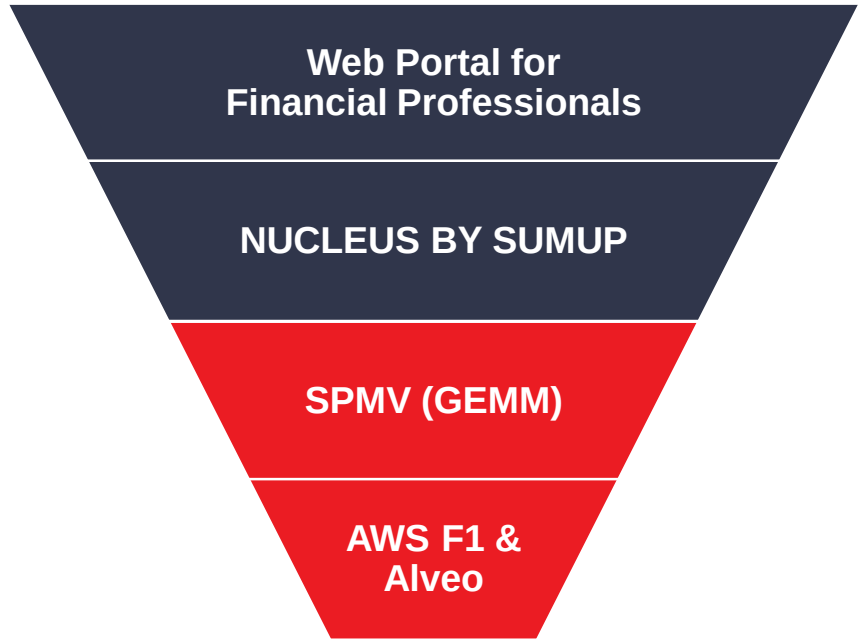
Value Proposition

- Accelerate this real time workload from many hours to minutes

Approach

- Using SDAccel methodology
- Leveraging Xilinx Optimized Libraries (e.g. GEMM)
- Deployed on AWS F1 and Alveo for On-Prem application

SUMUP ANALYTICS



4X end-to-end acceleration improvement over an optimized software solution

Acceleration Case Study: Big Zetta Systems

Company Summary

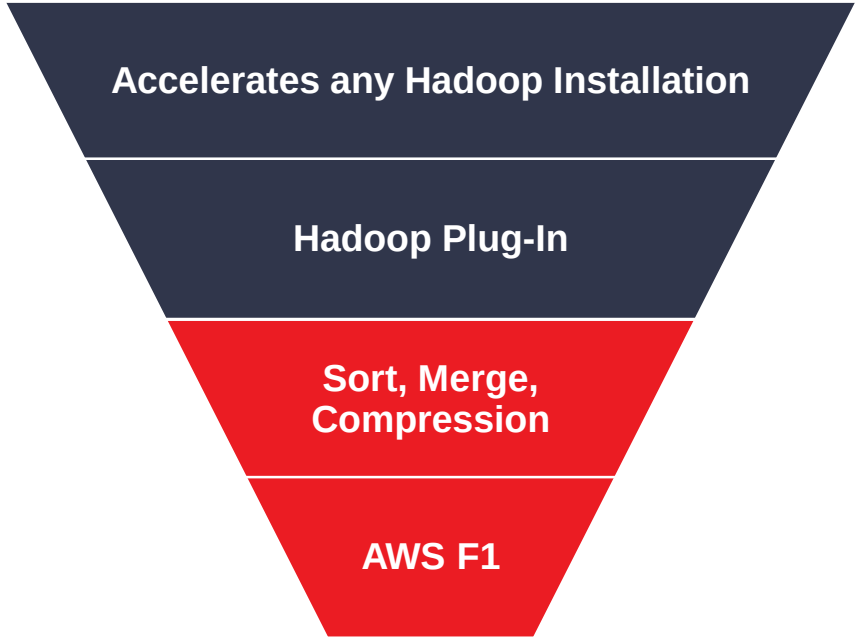
- SaaS solution accelerating Big-Data computations

Value proposition

- Reduce TCO by accelerating Map-Reduce infrastructure bottlenecks like sort, shuffle, compression and merge with a Hadoop Plug-In

Approach

- Using SDAccel methodology
- Developed sort and merge kernels using HLS
- Leveraging Xilinx LZ4 data compression
- Initial deployment on AWS F1



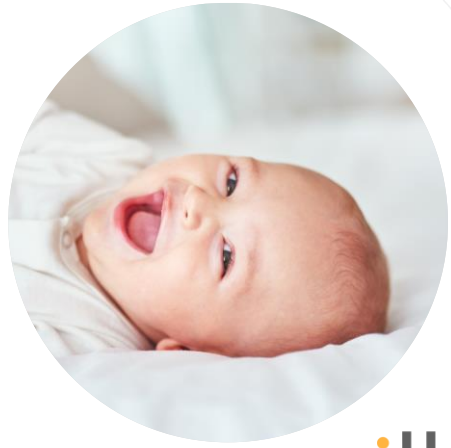
Achieved 3-10X acceleration and 10X TCO benefits

The Opportunity

Why this Matters to You

Re-Inventing the Acceleration Business Model

- **Technology Innovation Drives Business Innovation**
  - Explosive growth of “Cloud”
  - FPGA computing on a standard platform
- **Much lower barrier to entry for building and deploying Acceleration Applications**
  - No longer need to develop a custom product
- **Many ways to scale your application**
  - Software as a Service (SaaS) on Cloud
  - Develop & evaluate on Cloud, deploy on-premise



MAYO CLINIC

illumina®

edico genome

aws

The Advanced Compute Acceleration Platform

- **Engineered for Acceleration from the ground up**
  - Hardened hardware platform
  - Hardened array of programmable engines for Machine Learning and other computational intense workloads
  - Rich fabric and advanced DSP for custom kernels
  - High speed Network-on-Chip for data communication
  - Embedded Application Processors for host offload and Edge acceleration

Turbocharge Existing Applications, Create the Next Generation of Applications

The Era of FPGA Acceleration is Now

Favorable Conditions for Business Success

> FaaS, Cloud Adoption, Alveo boards and platforms

Xilinx is Committed to Scaling Application Development

> Methodology, Development Tools, Libraries, Community and Support

Get on Board!

> The Advanced Compute Acceleration Platform will change the game

Abstract

State of Scaling FPGA Application Development
Speaker: Dan Gibbons
Duration: 45 minutes
Abstract: FPGAs have been established in the industry as mainstream acceleration devices and Xilinx is leading the industry in FPGA as a Service (FaaS) with our flagship deployment in AWS F1 and with most major cloud providers. FPGAs true potential can be reached with a rich ecosystem of accelerated applications. Historically FPGAs have been programed using Hardware Description Languages and were considered difficult to use by software developers. But this paradigm is rapidly changing. Xilinx has been investing substantially to create a rich environment for enabling far more developers to tap into the power of FPGA acceleration. For software developers we are offering a native experience with vastly improved Ease of Use and for those with prior FPGA experience we are offering a whole new level of development productivity. Come learn about our vision for software programmability, our progress and roadmap, and why, as an active or potential FPGA application developer, this is important for you.
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