XDF XILINX DEVELOPER FORUM

AGENDA

December 10th

07:30

Registration Open

09:00 - 10:00

Keynote: Ivo Bolsens, Chief Technical Officer - Xilinx

10:00 - 11:00

Disruptive Innovation: Introduction to Xilinx Versal – Kirk Saban, Vice President of Product & Technical Marketing – Xilinx

11:00 - 18:00

Breakout Sessions

Hardware Design	Embedded System Software	Edge Software Development	Cloud Software Development

Exhibit Hall: Technology Demos & Networking Area

18:00

Reception

**Updated 12/06 (Subject to change)

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Hardware Design - Platinum Ballroom 1

This track is intended for hardware designers and system architects who want to learn best practices in using Vivado (timing, synthesis, partial reconfiguration), HLS/IPI, Model Composer and other tools. It will consist of sessions conducted by Xilinx technologists, guest speakers, and conclude with an expert panel discussion and Q&A. This popular track is suited for hardware designers using FPGAs for a wide variety of traditional FPGA applications.

11:00 - 18:00

- **Session**: IPI Methodology
  Speaker: Dan Michek
  Xilinx
  Time: 11:15 - 12:00

- **Session**: Revision Control Methodology
  Speaker: Brian Lay
  Xilinx
  Time: 12:15 - 13:00

- **Session**: HLS Methodology
  Speaker: Frederic Rivoallon
  Xilinx
  Time: 13:45 - 14:30

- **Session**: RTL Synthesis Methodology
  Speaker: Bala Krishnamurthy
  Xilinx
  Time: 14:30 - 15:00

- **Session**: Timing Closure Tips and Tricks
  Speaker: Ron Plyler
  Xilinx
  Time: 15:00 - 15:45

- **Session**: Partial Reconfiguration: An Evolution of Reconfigurable Platforms
  Speaker: David Dye
  Xilinx
  Time: 16:00 - 16:45

- **Session**: Expert Panel
  Speaker: Premduth Vidyanandan
  Xilinx
  Time: 16:45 - 17:30

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Embedded System Software - Gold 2

This track is intended for developers of software for embedded systems who want to hear about best practices for heterogeneous runtime design. Technical content in this track will cover open source OS and hypervisor considerations as well as multimedia and platform management. Discussions in this track will focus on ARM-based Xilinx SoC and RFSoC platforms.

11:00 - 18:00

- **Session**: Xilinx Software Strategy & Development Introduction **Speaker**: Tony McDowell
  Xilinx
  Time: 11:15 - 12:00

- **Session**: SoC Platform Management
  Speaker: Aniket Kolarkar
  Xilinx
  Time: 12:15 - 13:00

- **Session**: Heterogenous Realtime Software Architecture
  Speaker: Edgar Igesias
  Xilinx
  Time: 13:45 - 14:30

- **Session**: ENEA: High-Performance Real-Time Linux Solution for Xilinx Ultrascale+
  Speaker: Patrik Strömblad, ENEA
  Time: 14:30 - 15:00

- **Session**: Multimedia SoC System Solutions Speaker:
  Speaker: Forrest Pickett
  Xilinx
  Time: 15:00 - 15:45

- **Session**: RF Soloutions
  Speaker: Glenn Steiner, Xilinx
  Room: Basalt
  Time: 13:45 - 15:15

- **Session**: System Design from Antenna to Digital with Zynq UltraScale+ RFSoC
  Speaker: Ian Greenshields, EBV
  Room: Basalt
  Time: 15:15 - 15:45

- **Session**: Cortex-M1 for Xilinx Programmable Platforms
  Speaker: Simon George & Phil Burr
  Xilinx & ARM
  Time: 16:00 - 17:00

- **Session**: AI and computer vision accelerated multi-camera development
  Speaker: Michaël Uyttersprot Silica
  Time: 17:15 - 17:45

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Edge Software Development - Platinum Ballroom 2

This track is intended for software application developers and system architects who are designing accelerated systems on the edge – in automotive, smart city, machine vision and more. Emphasis will be on intelligent vision applications, leveraging accelerated computer vision and/or machine learning inference. SDSoC tools and CV libraries will be discussed in addition to machine learning stack and tools (pruning, compression, quantization) from DeePhi. Target platforms for this track will be focused on Xilinx Zynq SoC.

11:00 - 18:00

- **Session**: Xilinx Machine Learning Strategies with Deephi Acquisition
  Speaker: Yi Shan
  Xilinx
  Time: 11:15 - 12:00

- **Session**: Machine Learning for Embedded Deep Dive
  Speaker: Jingxui Lui
  Xilinx
  Time: 12:00 - 12:30

- **Session**: Using Machine Learning with SDSoC to Create Embedded Vision Systems
  Speaker: Rob Armstrong
  Xilinx
  Time: 12:30 - 13:00

- **Lab**: Design Accelerators for Vision Systems using Simulink®, Xilinx Model Composer and SDSoC
  Room: Lux
  Speaker: Uttara Kumar, Xilinx
  Time: 11:15 - 13:15 and 14:00 - 16:00

- **Lab**: Machine Learning for Embedded
  Speaker: Shuai Zhang
  Xilinx
  Time: 13:45 - 14:45

- **Lab**: Machine Learning for Embedded
  Speaker: Shuai Zhang
  Xilinx
  Time: 14:45 - 15:45

- **Lab**: Building Vision Systems using ML + CV + Sensors with SDSoC
  Speaker: Rob Armstrong
  Xilinx
  Time: 16:00 - 17:00

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Cloud Software Development - Gold 3

This track is intended for application developers and system architects who are designing accelerated applications in the data center or cloud – for data analytics, financial, genomics, video streaming and more. Emphasis will be on development and deployment with SDAccel and compute acceleration libraries that form the software acceleration stack for high performance Xilinx Virtex FPGAs used in cloud and on-premise data centers. Cloud FPGA computing services like AWS F1 as well as data center hardware accelerator platforms will be covered.

11:00 - 18:00

- **Session**: State of FPGA Based Acceleration
  Speaker: Vinay Singh
  Xilinx
  Time: 11:15 - 11:45

- **Session**: Fundamentals of FPGA Based Acceleration
  Speaker: Sergei Storojev
  Xilinx
  Time: 11:45 - 12:30

- **Session**: NGCodec
  Speaker: Ian Jefferson
  NGCodec
  Time: 12:30 - 13:00

- **Session**: V-Nova
  Speaker: Fabio Murra
  V-Nova
  Time: 13:45 - 14:15

- **Session**: Scaleflux - Computational Storage: Acceleration Through Intelligence & Agility
  Speaker: Thad Omura
  Scaleflux - EVP Marketing
  Time: 14:15 - 14:45

- **Session**: Maxeler: Amplifying the Power of Xilinx Datacenter Solutions in Finance and HPC
  Speaker: Georgi Gaydadjiev
  Maxeler
  Time: 14:45 - 15:15

- **Session**: Politecnico Di Torino: F1 Acceleration for Montecarlo: Financial Algorithms on FPGAs
  Speaker: Liang Ma
  Politecnico Di Torino
  Time: 15:15 - 15:45

- **Session**: Xelera
  Speaker: Felix Winterstein
  Xelera - CEO
  Time: 16:00 - 16:30

- **Session**: Accelerating AI in Datacenters: Xilinx ML Suite
  Room - Basalt
  Speaker: Kamran Khan, Xilinx
  Time: 16:00 - 17:00

- **Session**: InAccel: Cloud FPGA-Acceleration of Spark ML using Containers
  Speaker: Chris Kachris
  InAccel - CEO, Co-Founder
  Time: 16:30 - 17:00

- **Session**: Accelerating Databases with FPGA
  Speaker: Prasanna Sukumar
  Reniac - Head of Engineering
  Time: 17:00 - 17:30

- Session: Omnitek: An FPGA CNN for Intelligent Video/Vision Systems
  Room - Basalt
  Speaker: Roger Fawcett, Omnitek
  Time: 17:00 - 17:30

- **Session**: Accelerating Memcached on Cloud FPGAs
  Speaker: Andrew Canis & Ruolong Lian
  LegUp Computing - CEO & COO
  Time: 17:30 - 18:00

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A Look into Versal - Basalt

In addition to the other tracks, we will be holding two sessions that take a deep dive into Versal, the industry's first ACAP. These sessions will include an overview of the architecture of the Versal Platform as well as deep dive into the Software Programmable Engine and Programming Enviornment.

11:00 - 18:00

- **Session**: Project Everest: A Look Inside the First ACAP
  Speaker: Sumit Shah
  Xilinx
  Time: 11:15 - 12:00

- **Session**: Project Everest: Software Programmable Engine and Programming Environment
  Speaker: Ambrose Finnerty
  Xilinx
  Time: 12:00 - 13:00

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