5 REASONS TO CHOOSE AMD SPARTAN™ ULTRASCALE+™ FPGAS FOR YOUR EMBEDDED APPLICATIONS

At a glance

The new AMD Spartan™ UltraScale+™ FPGA family offers a competitive balance of price, power, features, and size. Explore how these devices help designers achieve rapid time-to-market at a low cost for I/O-intensive applications.

1

BENEFIT FROM MORE FEATURES IN A SMALLER PACKAGE

Experience the industry's highest I/O-to-logic-cell ratio ≤28 nm process[1]

The Spartan UltraScale+ FPGA family offers ratios ranging from 304 I/O at 11K logic cells to 572 I/O at 218K logic cells—minimizing additional components while maximizing your ability to design feature-rich applications with any-to-any connectivity.

IS SPACE AT A PREMIUM FOR YOUR USE CASE?

Spartan UltraScale+ FPGAs start at 10x10 mm, and Spartan 7 FPGAs come in the smallest packages of all, starting at just 8x8 mm.

2

GET FAST INTERFACING WITH ADVANCED CONNECTIVITY OPTIONS

Tap into versatile support for an array of communication protocols

Spartan UltraScale+ FPGAs offer up to eight GTH transceivers running at 16.3 Gb/s for high-speed data transfer and added bandwidth. Comprehensive MIPI D-PHY interfaces up to 3.2 Gb/s and multiple PCIe® Gen4 interfaces provide exceptional design flexibility.

NEED MORE SIGNAL PROCESSING HORSEPOWER AND TRANSCEIVER BANDWIDTH?

AMD Artix™ 7 and Artix UltraScale+ devices excel in compute density and transceiver bandwidth at a small size, offering up to 1,200 DSP slices and up to 12 transceivers running at 16.3 Gb/s.

3

CAPTURE POWER SAVINGS WITHOUT SACRIFICING PERFORMANCE

Select from nine device options to support a range of requirements

The proven 16 nm architecture offers significant power savings—projected to offer up to a 30% reduction in total power compared to the previous 28 nm series on lower densities[2]—while delivering up to 1.9X fabric performance.[3] For applications requiring high-performance interfaces like LPDDR4x/LPDDR5 memory or PCIe® Gen4, the larger Spartan UltraScale+ FPGAs also include hardened IP, projected to improve overall power efficiency up to 60%[4] and enhance overall system performance.

WANT AN EXTRA BOOST IN PERFORMANCE, BUT DON'T NEED LPDDR4X/LPDDR5?

Artix UltraScale+ FPGAs are built on the same 16 nm process node and offer up to 308K logic cells.

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4

PROTECT YOUR DESIGNS—TODAY AND TOMORROW

Leverage state-of-the-art security features for a proactive defense

Spartan UltraScale+ devices come with robust security features to help protect your IP, prevent tampering, and maximize uptime. These include physical unclonable function (PUF), primary public key/secondary public key (PPK/SPK) for authentication, true number random generator (TRNG) for encryption, and more.

DOES YOUR DESIGN REQUIRE A FORWARD-LOOKING APPROACH TO SECURITY?

Spartan UltraScale+ devices help you get ahead of emerging threats—supporting post-quantum cryptography (PQC) and a permanent tamper penalty to protect against misuse.

5

FINALIZE DESIGNS QUICKLY WITH EASY-TO-USE SOFTWARE

Create, integrate, and implement designs with an intuitive, all-in-one tool

Speed design cycles with a single tool that stands apart from the rest—the AMD Vivado™ Design Suite. This software supports the entire design flow, while other FPGA vendors' products often necessitate the use of multiple tools. Leverage a rich IP catalog and machine-learning-based power optimization capabilities to work more productively.

DID YOU KNOW THE VIVADO DESIGN SUITE IS AVAILABLE AT NO COST FOR DEVICES IN THE AMD COST-OPTIMIZED PORTFOLIO?

You can build affordable designs using Spartan UltraScale+, Artix UltraScale+, Spartan 7, or Artix 7 series devices.

ACCELERATE TIME-TO-MARKET FOR *COST-SENSITIVE DESIGNS*

Experience the latest addition to a broad portfolio of FPGAs spanning 40 years.

Learn more about how AMD Spartan UltraScale+ FPGAs can help you maximize efficiency, capabilities, and security while reducing cost[5,6] and power consumption.[7,8]

1. Based on product data sheets for AMD Spartan™ UltraScale+™ FPGAs versus Efinix, Intel, Lattice, and Microchip, as of February 2024, comparing the total I/O-to-logic-cell ratios of comparable 28 nm and lower node size FPGAs. (SUS-11)
2. Projection is based on AMD labs internal analysis in January 2024, using Total Power calculation (Static plus Dynamic power) based on the difference in logic cell count of an AMD Artix™ UltraScale+ AU7P FPGA, to estimate the power of a 16 nm AMD Spartan™ UltraScale+ SU35P FPGA versus a 28 nm AMD Artix 7 7A35T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total Power will vary when final products are released in market, based on configuration, design, usage, and other factors. (SUS-03)
3. Projection is based on AMD labs internal analysis in January 2024, using nine different designs on two devices, Artix™ UltraScale+™ AU10P FPGA as a scale to Spartan™ UltraScale+ FPGA versus a 28 nm Artix 7 7A100T FPGA, that were run at different clocks for Fmax calculation. The constraints were set so that the device ran at its max performance. Performance results may vary based on configuration, usage, and other factors. (SUS-04)
4. Projection is based on AMD internal analysis in January 2024, using a Total Power calculation (Static plus Dynamic power) based on the logic scale count of an AMD Artix™ UltraScale+™ AU7P FPGA to estimate the total power of Spartan™ UltraScale+ SU200P FPGA versus Artix 7 7A200T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total Power interfacing may vary when products are released in market, based on configuration, usage, and other factors. (SUS-06)
5. Based on data sheet comparison of the AMD Spartan™ UltraScale+™ SU10P FPGA to the Spartan 7 7S50 FPGA and calculating cost savings per I/O based on AMD list prices as of February 2024, for user designs requiring at least 200 GPIO. Prices subject to change, results may vary. (SUS-09)
6. Based on data sheet comparison of the AMD Spartan™ UltraScale+™ SU55P FPGA versus the AMD Artix™ 7 7A100T FPGA, calculating a reduction in programmable logic requirements of the Spartan UltraScale+ SU55P FPGA and the resulting cost savings using AMD list prices as of February 2024. Prices are subject to change, results may vary. (SUS-10)
7. See note 2 above.
8. See note 4 above.

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