Implementing Multi-Gigabit Serial Links in a System of PCBs

日本ケイデンス・デザイン・システムズ社
PCBシステム事業本部 プロダクトマーケティングマネジャー
益子 行雄
2002年7月9日
Multi-Gigabit Links on PCBs

AGENDA

• Industry Trends
• Process Overview
• Process Step Details
• Summary & Resources
Multi-Gigabit Links on PCBs

AGENDA

• Industry Trends
  – Data Movement
  – Analog Challenges
  – Higher Integration
  – New Solutions

• Process Overview
• Process Step Details
• Summary & Resources
#1: Data Movement

"Data Processing" to "Packet Switching"

Interconnects

Fabrics
“A state-of-the-art serial link can move 3.125 Gbits/s – three to four times faster than Rambus and other high-speed interfaces. Achieving that speed across a backplane is not easy. …fabric designers must possess high-speed analog expertise to keep pace.”

Linley Gwennap “Fabrics make the switch”, EETimes January 14, 2002 – page 37
3: Higher Integration

“We’re now at the point where it’s getting cheaper to put more gates behind a fast serial line than to lay down copper traces.”

Jim Pappas, Intel – commenting on why 3GIO used serial technology and PCI used parallel – EETimes February 18, 2002 page 92
New Solutions

• Virtex-II Pro™ FPGA with Rocket I/O™ transceivers
  – Up to 3.125 Gbits/s
  – Supports XAUI, Infiniband, 3GIO, …

• SPECCTRAQuest
  – High-speed PCB constraint & analysis
  – Integrated IC and PCB simulation

• High-Speed Design Kits
  – Fastlane to implementation
  – First of its kind offering
Multi-Gigabit Links on PCBs

AGENDA

• Industry Trends

• Process Overview
  – Flow Diagram
  – Iterations
  – Getting Started

• Process Step Details

• Summary & Resources
Remove Iterations

Propose System Architecture
Feasibility Simulations
Solution Space Simulations
Capture & Bind Constraints
High-Speed PCB Layout
Virtual Verification
Product $
Manufacture
Hardware Test & Verify
Fab & Assemble Prototype

Time, Dollars, Opportunity
Getting Started

Start by gathering these components

- IC / PCB Models
- Starter Simulations
- Layout Constraints
- Documentation

- IC Simulator
- PCB Simulator
- Constraint-Driven Layout
- GUI & PCB Interfaces

Xilinx Design Kit

SPECTRAQuest
Multi-Gigabit Links on PCBs

AGENDA

• Industry Trends
• Process Overview

• Process Step Details
  – Challenges & solutions for each step

• Summary & Resources
#1: Architecture

- IC Options?
- distance?
- Cable? Connectors?
- Serial Standard?
- How Wide?
- PCB Construction?
#2: Feasibility

Simulations

Distance?

Cable? Connectors?
#2: Feasibility cont’d

Feasibility Simulations

PCB Construction?
1 & 2: Concurrency

- Direct use of silicon model in SPECCTRAQuest
  - Encrypted too
- > 20x faster to include
  - Compared to conversion to behavioral model
    (data in notes)
- SPECCTRAQuest
  - Supports IBIS 3.2, Hspice, and MacroModel structures

Can use structural transistor-level (Hspice) models concurrent with IC development & test
Simulator Option

Can use Hspice option for:
1. Concurrent IC/PCB Design
2. Complex Silicon Models
#3: Solution Space

- **Test / Determine**
  - Voltage Swing
  - Pre-emphasis
  - AC Coupling
  - Impedance Match
  - Terminations
  - ISI, PRBS, 8b/10b
  - Jitter Tolerance

- **Target / Tolerance**
  - PCB Stackup
  - PCB Materials
  - Trace Geometries
  - Xtalk Spacing
  - Signal Attenuation
  - Route Mis-match
  - Power Rails

ISI=Inter-Symbol Interference, PRBS=Pseudo-Random Bit Sequence, 8b/10b=see notes
#3: Solution Space cont’d

- Same Environment
- Sweep Simulations
- Stimulus Patterns
- Eye Diagrams
- Bound Solution
#4: Constraints

- Same Environment
- Capture Electronically
- Bind in Layout Database
- Constraint Manager
  - Schematic, Simulation, Layout Tools
#5: PCB Layout

- High-speed constraints
  - Electrical
  - Physical
  - Timing
- Real-time margins in Constraint Manager
#6: Verification

- DRC Reports
- CM “Green”
- Post-Layout Simulation
  - Direct from PCB
  - Waveforms
  - Reports
#6: Virtual Debug

1. Failure?
2. Extract differential net to electrical view
3. Examine, debug, simulate, fix
Process Review

Turning the corner to physical hardware

- Propose System Architecture
- Feasibility Simulations
- Solution Space Simulations
- Capture & Bind Constraints
- High-Speed PCB Layout
- Virtual Verification
- Manufacture
- Hardware Test & Verify
- Fab & Assemble Prototype
- Product $
#7: Tapeout!

By using the process, simulations, and automation described, you’re ready to tapeout an error-free Multi-Gigabit system design.
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Summary

• Multi-gigabit links are becoming mainstream
• A high-speed implementation process is needed for first-pass success
• High-speed Design Kits are available to assist
  – Xilinx Rocket I/O and Cadence SPECCTRAQuest
Recommended Resources

• Virtex II Pro FPGA
  – http://www.xilinx.com/virtex2pro/

• Rocket I/O

• Xilinx SPECCTRAQuest Design Kit
  – Click license NDA, download free Kit
  – http://www.xilinx.com/publications/xcelonline/partners/xc_speckit42.htm

• Cadence High-Speed PCB Tools
  – Visit the booth at the Conference
  – www.pcb.cadence.com
  – www.pcbhighspeed.com
  – www.specctraquest.com
Design Kit Contents

- Simulation Files
  Models, Topologies, etc.
- Automated Layout Guideline
- Constraint Files
- Scripts, Tools, Utilities
- Tutorial Movies
- ...all organized into a web-site