Delivering a Generation Ahead
The Strategic Partner of Choice

May 2014
Semiconductor Market Leader
All Programmable Devices

$2.38B FY14 revenue
50% market segment share
3,500+ employees worldwide

20,000 customers worldwide
3,500+ patents
60 industry firsts

Founded 1984

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Xilinx Management Team

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SVP & CTO

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SVP Corp Strategy & Marketing

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Vincent Tong
SVP WW Quality, NPI, & APAC Executive Leader

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SVP WW Sales

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XILINX ® ALL PROGRAMMABLE.
Expanding the Scope of our Business

ALL PROGRAMMABLE

➢ ALL Programmable Electronic Systems
➢ ALL Programmable Technologies
➢ ALL Programmable Devices
Enabling All Programmable and Smarter Systems

ENABLING SMARTER

Networks  Data Centers  Vision  Factories  Energy
Speeding Time to Differentiation and Integration

Fastest Time to
- Realize Unique IP
- Refine Unique IP
- Hi Performance
- Lowest Power
- Proof of Concept

Coupling Value of All Programmable Devices with Value of Design Acceleration

Fastest Time to
- Smarter Systems
- Flexible Integration
- Rapid Derivatives
- Max Design Reuse
- Lower BOM Cost
Delivering A Generation Ahead

28nm And Beyond

Programmable Logic Devices
Enables Programmable Logic

All Programmable Devices
Enables All Programmable & Smarter Systems
Vivado® Design Suite

Greatly Simplify Programming for a Broader Set of Users

Strategic Investments

- 5 years in the making
- 23 million lines of code
- 1,000 person years of development
- 3 corporate acquisitions
- 10+ technology acquisitions
Competency Expansion for Strategic Partnership

Customer With Xilinx

Abstract Programming
Integration Automation

System Architecture
Embedded Software
SoC Architecture

Implementation Software
Digital and AMS Circuits
Advanced Foundry

VIVADO

Smarts

3D IC

SoC

FPGA

AMS

Dual ARM

FPGA

AMBA

FPGA

Transceivers

Transceivers

Logic

μP

AMS

I/O

Protocols

Software
## Delivering A Generation Ahead: Xilinx Firsts

<table>
<thead>
<tr>
<th>Year</th>
<th>Event Description</th>
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</thead>
<tbody>
<tr>
<td>March 2011</td>
<td>First to 28nm</td>
</tr>
<tr>
<td>December 2011</td>
<td>First to SoC</td>
</tr>
<tr>
<td>October 2011</td>
<td>First to 3D IC</td>
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<tr>
<td>July 2012</td>
<td>First ASIC/SoC Class Tools</td>
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<tr>
<td>July 2012</td>
<td>First Design Methodology</td>
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<td>November 2013</td>
<td>First 20nm Ship</td>
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<tr>
<td>November 2013</td>
<td>First and Only High End</td>
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<tr>
<td>December 2013</td>
<td>First to 4M Logic Cells</td>
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</table>
Low-End Portfolio: Optimized for Best Value

Value

Performance

Power Efficiency

I/O Optimization

Integration

Performance

Power Efficiency

Transceiver Optimization

System Optimization

Broasted Cost Effective Low-End Portfolio
28nm Market Segment Share Momentum

Source: Company Reports
Xilinx: Sticking to the FACTS

Proven Formula
Repeated Across Nodes

28nm
20nm
16nm

5 ADVANTAGES
- Foundry
- Architecture
- Circuits
- Total Execution
- Software
Foundry: Significant Strategic Advantage at 20/16nm

- TSMC: 4 out of 4
- Design Enablement
- Process Technology
- Foundry Services and Lifetime Supply

SoC and 3D IC
Architecture: Strategic Advantage at 20/16nm

Add an Extra Node of Value with ASIC-Class 3D ICs and MPSoCs
Total Execution: With Superior Quality

- Zero errata
- < 2 ppm
- Scalability

Quality of Design
Quality of Silicon
Quality of Manufacturing
Quality of Software

- VIVADO
- UltraFAST
- All Programmable
- Abstractions

- 4X
- 10X
- 15X

Total Execution: With Superior Quality

- 28.05 Gb/s
- 13.1 Gb/s
- 12.5 Gb/s
- 6.6 Gb/s

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Software: Strategic Advantage at 20/16nm

- Greatly Simplify Programming for a Broader Set of Users
- Built for ASIC and SoC class designs
- Up to 15x front to back productivity gains
- Pairing with UltraFast for best practices
Co-optimizing Tools With Methodology

Design Methodology

Old Design Schedule

New Design Schedule

10x Time Savings with UltraFast

- Best Practices Manual, Videos, Training
- Design Checklists
- Automated Enforcement
Expanding the User Base, Improving Productivity

System/Software

All Programmable Abstractions

- Accelerated Development for Hardware Engineer
- Enabling Software Engineers with Hardware Performance
- Algorithm Deployment for Systems Engineers

Towards ‘Software Defined Specification’ Environments
Xilinx: Delivering A Generation Ahead

The De Facto Standard at 28nm
Proven - Zero Errata - >70% Overall Market Share - Over 95% Market Share of SoC

1.5-2X Better
- Performance
- Power
- Integration
- BOM Cost

The De Facto Standard at 20nm
Only ASIC Class Architecture and Design Tools - Only High-End - First to Ship - Best Quality

Another 2X
- System Performance
- Integration
- Scalability
- 1-2 Years Ahead
The De Facto Standard Design Suite

Only ASIC Strength Design Design Tools - 80% Use Vivado - Built for the Next Decade of Design

Up to 15X Superior
- Productivity
- Methodology
- Device Utilization
- Quality of Results

The De Facto Standard for Quality

28nm and 20nm - FPGA - SoC - 3D ICs - Vivado Design Suite

Absolute Quality
- Zero Errata
- <2 Parts Per Million
- 20-30% Better Utilization
- 20-30% Better QoR
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