THE HIGH-PERFORMANCE
PROGRAMMABLE SILICON FOUNDATION
FOR TARGETED DESIGN PLATFORMS

SATISFYING THE INSATIABLE DEMAND FOR HIGHER BANDWIDTH

The Programmable Imperative

- Competitive forces are driving infrastructure equipment manufacturers to focus on reducing system costs and operating expenses
- Next-generation applications across the spectrum of electronic equipment need more bandwidth
- Developers need heavy-duty computational capabilities, while simplifying and lowering the costs of their systems through integration

Targeted Design Platforms

- Targeted Design Platforms from Xilinx and its network of third parties provide system designers with simpler and smarter methodologies for creating FPGA-based system-on-chip solutions
- Targeted Design Platforms enable software and hardware designers to leverage open standards, common design methodologies, development tools, and run-time platforms
- Designers can spend less time developing the infrastructure of an application and more time building differentiating features into their products

The High-Performance Silicon Foundation

At up to 50% lower power and 20% lower cost than previous generations, the new Virtex®-6 FPGA Family delivers the right mix of flexibility, hard intellectual property (IP) cores, transceiver capabilities, and development tool support that enables Xilinx customers to meet the demands of markets with evolving standards and stringent performance requirements in the pursuit of higher bandwidth. For volume production, EasyPath™ FPGAs reduce cost for volume production with no risk of conversion and no hidden costs.

Advanced FPGA Technology for Complex Requirements

Built on a 40nm process using third-generation Xilinx ASMBL™ architecture, the Virtex-6 FPGA family is supported by a new generation of development tools and a vast library of IP to ensure productive development and efficient design migration from previous generations. Providing higher performance and lower power consumption compared to competitive FPGA offerings, the new devices operate on a 1.0V core voltage with an available 0.9V low-power option.

Greater System Integration with Next-Generation FPGAs

The combination of advanced 40nm process technology and enhanced architecture enables system-level integration and helps you meet aggressive performance targets in the least expensive speed grade, while increasing logic efficiency with integrated DSP slices, PCI Express® technology, and Ethernet MAC blocks. The significant reduction in power consumption allows board designers to select smaller heat sinks, fans, and power supplies while using fewer power rails than competing FPGAs.

XILINX®

Virtex-6 FPGAs help you to minimize design risk with integrated PCIe® interface blocks, DSP and other capabilities for building next-generation graphics, storage, networking, and system products. You can accelerate development with complete serial solutions for chip-to-chip, board-to-board, and box-to-box applications, while SelectIO™ technology and pre-verified IP cores make it easy to support all popular interface standards.

Virtex-6 FPGA Families

The Virtex-6 FPGA family comprises three domain-optimized FPGA platforms that deliver different feature mixes to best address a variety of customer applications:

Virtex-6 LXT FPGAs – optimized for applications that require high-performance logic, DSP, and serial connectivity with low-power GTX 6.5Gbps serial transceivers

Virtex-6 SXT FPGAs – optimized for applications that require ultra-high DSP performance and serial connectivity with low-power GTX 6.5Gbps serial transceivers

Virtex-6 HXT FPGAs – optimized for communications applications that require the highest-speed serial connectivity with a combination of up to 72 GTX transceivers and the new GTH transceivers that support line rates in excess of 11Gbps

Key Capability Overview

Hit Your Performance Targets Easily

- Achieve a one speed-grade performance gain with second-generation ExpressFabric™ technology, 600MHz clocking technology, and performance-tuned IP blocks
- Build high-bandwidth interfaces for DDR3 memory with flexible SelectIO™ technology
- Accelerate DSP performance with enhanced DSP48E1 slices

Optimize I/O Bandwidth, Power, and Cost with Easy-to-Use High-Speed Serial Solutions

- Choose between two varieties of low-power serial transceivers offering line rates in excess of 11Gbps
- Obtain assured compliance with popular standards such as 10/40/100G Ethernet, PCI Express®, OC-48, XAUI, SRIO, and HD-SDI
- Second-generation integrated PCI Express® blocks and third-generation Tri-mode Ethernet MAC blocks make it easy to implement popular interfaces

Meet Your Power Requirements while Maximizing Performance

- Advanced process, architecture, tools, and system-level optimizations reduce core power by 30%
- Available low-voltage option increases power savings to 50% while delivering performance comparable to standard devices
- Enhanced SelectIO technology reduces I/O power by up to 50%

Reduce System Cost

- 40nm process enables system-level integration and helps you meet aggressive performance targets in the least expensive speed grade
- Increase logic efficiency with integrated DSP slices, PCI Express technology, and Ethernet MAC blocks
- Select smaller heat sinks, fans, and power supplies enabled by reduced power consumption
- Simplify board design with significantly fewer power rails than competing FPGAs
- To reduce costs for volume production, use EasyPath™ devices once your design is fixed and no longer requires the Virtex FPGA's full programmability

Implement High-bandwidth Parallel Interfaces

- Support for multiple electrical standards in the same device with 30 individually configurable I/O banks
- Design with PCI, RapidIO, XSBI, SPI4.2, and more
- Configure SelectIO™ pins to support HSTL, LVDS (SDR and DDR), and more, at voltages from 1.0V to 2.5V

Increase DSP Algorithm Performance

- Increase DSP throughput using multiple channels or parallel hardware architectures
- Free up DSP processor CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor
- Obtain highest memory-to-logic ratio with Virtex-6 SXT FPGAs for efficiently implementing memory-intensive functions in video processing and medical imaging

Create Customized Embedded Systems

- Optimize performance and power by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors
- Offload CPU-intensive operations such as video processing, 3D data processing, and floating-point math

Bring Your Product to Market Faster

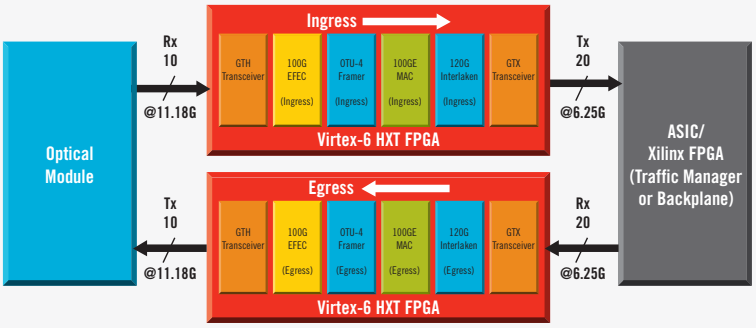
- Achieve maximum FPGA performance with ISE® Design Suite
- Design faster and reduce risk with pre-verified IP cores
- Debug logic and serial interfaces quickly with the real-time verification capabilities of ChipScope™ Pro tools

FEATURES OVERVIEW

40nm ExpressFabric™ Technology Achieve highest performance, most efficient utilization on 40nm triple-oxide process	▪ One speed-grade higher performance, 50% lower power than previous generation ▪ Second-generation six-input look-up table (LUT) architecture ▪ Highest flip-flop: LUT ratio enables enhanced pipelining
600MHz Clocking Technology Achieve highest speeds with high-precision, low-jitter clocking	▪ New PLL-based mixed-mode clock managers (MMCM) for lowest jitter, jitter filtering ▪ Improved frequency synthesis offers 8x finer control ▪ Mid-point buffering reduces skew and jitter in on-chip clock network
Memory Options Build the right memory for any application	▪ Distributed RAM enables 256-bit memory per CLB @ 64 bits per LUT ▪ 600MHz, 36Kbit Block RAM can be split into two 18Kbit blocks to double Block RAM bandwidth ▪ Interface to high-performance external memories such as DDR3, QDR II+, RDLRAM, and more
600MHz DSP48E1 Slice More than 1,000 GMACS performance using DSP48E1 slices	▪ Increased DSP resources in all devices, up to 2,016 slices in a Virtex-6 SX475T FPGA, supported by increased block RAM ▪ Enhanced architecture with a 25-bit pre-adder, 25 x 18 multiplier, 48-bit adder, and 48-bit accumulator (cascadable to 96 bits) ▪ 20% lower power consumption: 1.09mW/100MHz at a 38% toggle rate
1.40Gbps SelectIO™ interfaces with ChipSync™ Source-Synchronous Technology Implement industry-standard and custom protocols with DDR3 support and reduced power	▪ Simplify board design with built-in I/O delay circuits that compensate for unequal trace lengths with flexible per-bit deskew ▪ Synchronize incoming data to FPGA internal clock with built-in serializer/deserializer ▪ Adaptive delay setting recalibrates automatically to compensate for changing operating conditions
High-Speed Connectivity Implement serial protocols at the lowest power	▪ Flexible serial transceivers support multi-rate applications ▪ GTX transceivers run at 150Mbps to 6.5Gbps with 25% lower power consumption: < 150 mW (typ) at 6.5Gbps ▪ GTH transceivers support line rates beyond 11Gbps to enable 40G and 100G protocols and more with low power consumption: ~220mW (typ) at 10.3125Gbps
PCI Express Block: 1/2/4/8-lane; Gen1 and Gen2 Built-in support for ubiquitous standard	▪ PCI SIG-verified Gen1 and Gen2 compliance (on integrators list) ▪ Works with GTX transceivers to deliver PCIe endpoint and root port function ▪ Built-in hard IP frees user logic resources and reduces power ▪ Up to four PCIe blocks in a single device
Ethernet Media Access Controller: 10/100/1000 Mbps Connect to the Internet via an integrated tri-mode EMAC	▪ UNH-verified ▪ 2.5Gbps mode for higher bandwidth using custom protocols ▪ Up to four Ethernet MAC blocks in a single device
System Monitor and Analog-to-Digital Converter Simplify system management and diagnostics	▪ Fully specified 10-bit, 200k samples/sec ADC with programmable monitoring functions ▪ On-chip temperature and supply voltage sensors ▪ Analog measurements accessible via JTAG at any time, even before FPGA configuration
Enhanced Configuration and Bitstream Protection Reduce system cost, increase reliability, and safeguard your design	▪ Partial reconfiguration support for increased design flexibility and logic efficiency; now 10x faster ▪ Reliable in-system reconfiguration with multi-bitstream management ▪ Built-in error detection and correction for better SEU (single event upset) protection ▪ Protect your designs with 256-bit AES (Advanced Encryption Standard) security with battery-backed or non-volatile e-fuse key storage ▪ Device DNA enables protection against unauthorized overbuild
Third-generation Sparse Chevron Packaging Technology Keep system noise under control and simplify PCB layout	▪ Unique PWR/GND pin pattern minimizes crosstalk and reduces PCB layers ▪ On-substrate bypass capacitors shrink PCB area

How Targeted Design Platforms accelerate innovation

Wired Telecommunications



OTU-4 Framing and EFEC for Core Networks

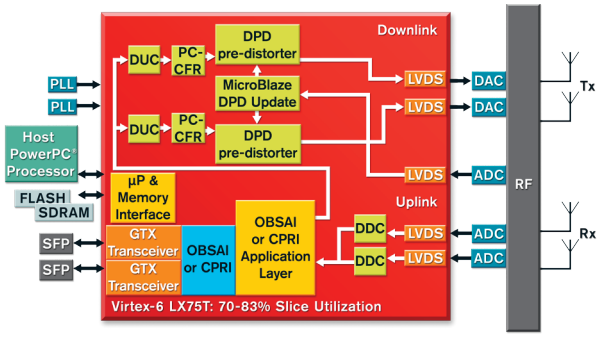
Implement an optical interface to 100GE MAC with framing, enhanced forward error correction (EFEC), and interface to ASIC (or backplane) via Interlaken using two Virtex-6 HX565T FPGAs.

Satisfy insatiable bandwidth demand

Virtex-6 FPGAs provide all the capabilities you need to develop products for a green central office.

- Reach higher performance and bandwidth within existing power and cooling footprints
- Integrate packet-processing and traffic-management functions with faster and wider data paths that satisfy tough throughput and latency requirements
- Simplify interfacing to DDR3, RLDRAM, and QDR SRAM with SelectIO™ technology
- Implement 40G and 100G bridging with IP for key protocols and flexible serial transceivers supporting line rates above 10Gbps

Wireless Infrastructure



Long Term Evolution (LTE) 2x2 Radio Design

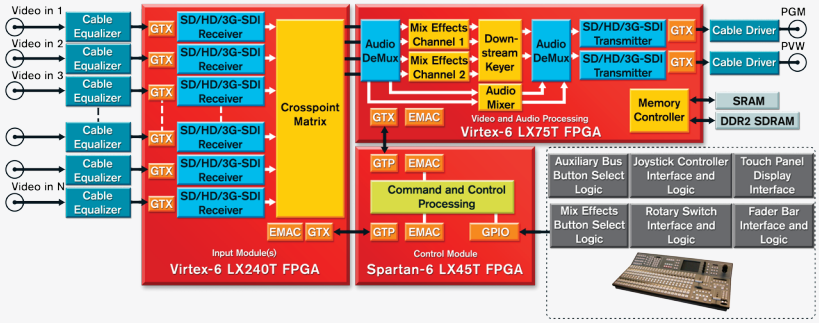
Achieve lower overall cost, lower power, and higher reliability with a single Virtex-6 LX75T FPGA. Pin-compatible architecture makes it easy to scale up to 2x4 and in the same package!

Enable "green" base stations

Virtex-6 FPGAs help you to reduce cost and power consumption, deliver scalable platforms, and support multiple air interface standards.

- Integrate crest factor reduction (CFR) and digital pre-distortion (DPD) algorithms to increase power amplifier efficiency up to 45% for reduced OPEX
- Reduce power consumption by over 50% compared to ASSP-based implementation by integrating radio function into a single FPGA with the optimal balance of logic, memory, and DSP resources
- Deliver flexible, multi-mode base stations that simplify the carriers' challenge of supporting multiple air interfaces
- Accelerate implementation with reusable IP for DUC/DDC, CFR, DPD, OBSAI, and CPRI

Broadcast



Next-Generation Production Switcher Supporting SD/HD/3G-SDI Interfaces

Achieve higher image quality and support more video streams while reducing power using Spartan-6 and Virtex-6 FPGAs.

Deliver dynamic, high-resolution video and audio content

Combine Virtex-6 and Spartan-6 FPGAs to build lower-cost IP-based equipment that bridges between broadcast and telecommunications networks.

- Reduce cost per-channel by integrating interfaces, codecs, and video processing algorithms in high-capacity FPGAs
- Differentiate your system with improved video quality enabled by integrated DSP resources
- Aggregate multiple uncompressed SDI video streams up to full 1080p60 HD onto 10Gbps Ethernet networks, or bridge multiple compressed ASI streams onto 1Gbps Ethernet for triple-play services using integrated low-power transceivers
- Accelerate implementation with reference designs for triple-rate SDI, audio mux/demux, and more

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