KC705 MIG Design Creation with Vivado

July 2013

XTP196

Revision History

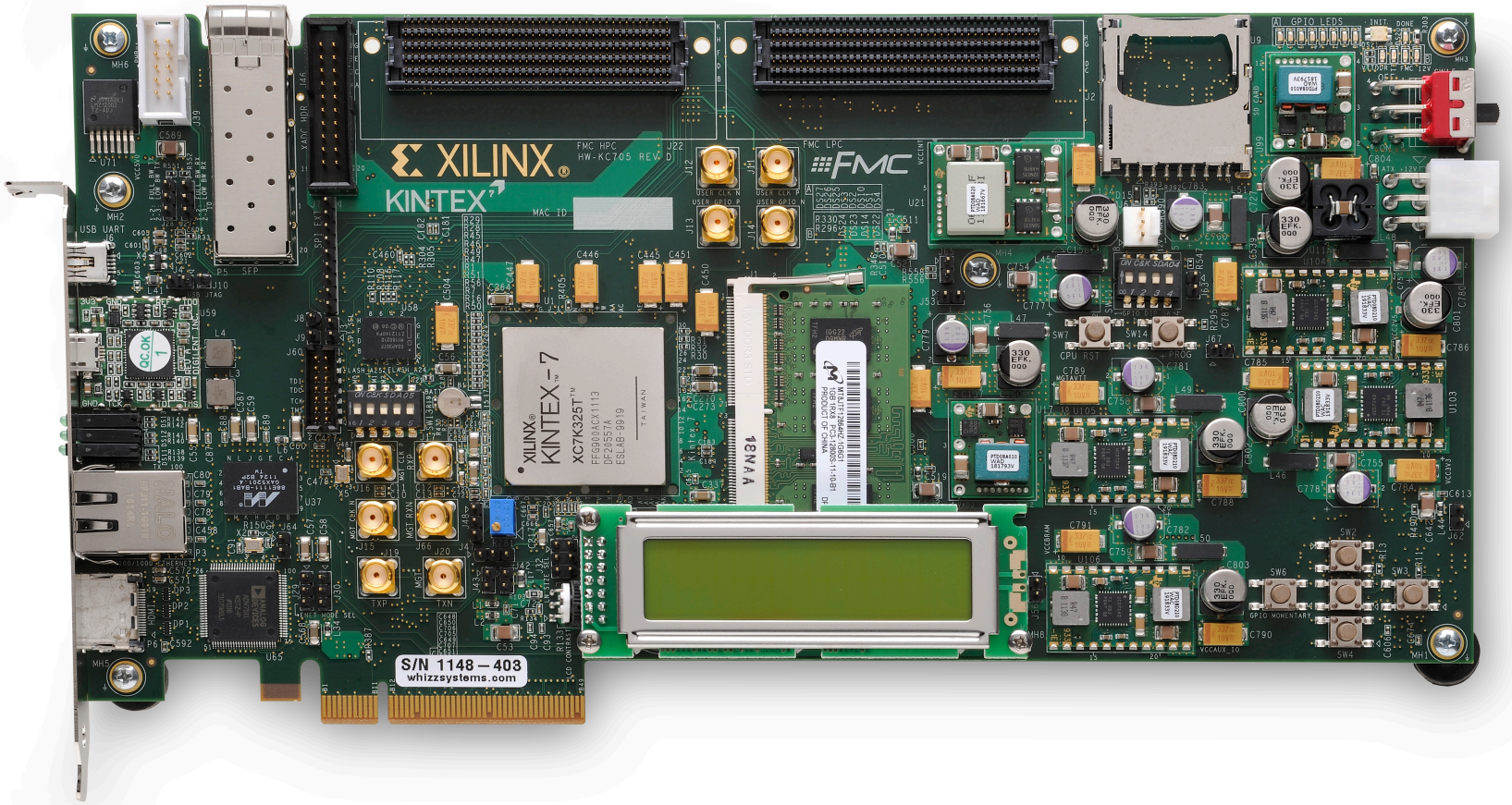
Date	Version	Description
07/30/13	5.1	Added missing files to RDF0186.
06/19/13	5.0	Recompiled for 2013.2
04/03/13	4.0	Recompiled for 2013.1. AR53420 fixed. Added AR55531.
02/22/13	3.1	Added AR53420.
12/18/12	3.0	Recompiled for 2012.4. Added AR53392.
10/23/12	2.0	Recompiled for 2012.3. Added AR52368.
07/25/12	1.0	Regenerated for 14.2. Added Vivado Flow. Added AR50886.

Overview

- KC705 Board
- KC705 Setup
- Generate MIG Example Design
- Modifications to Example Design
- Compile Example Design
- Run MIG Example Design
- References

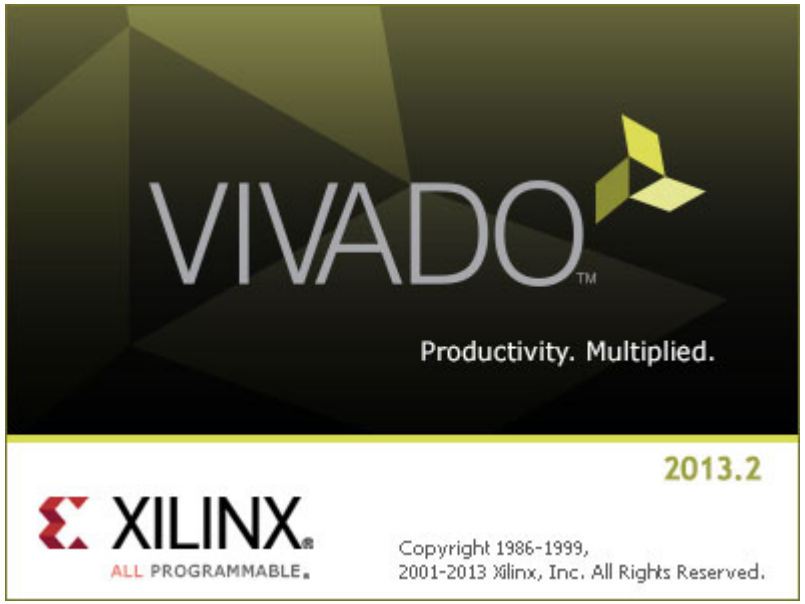
Note: This presentation applies to the KC705

Xilinx KC705 Board



Vivado Software Requirements

- Xilinx Vivado Design Suite 2013.2, Design Edition



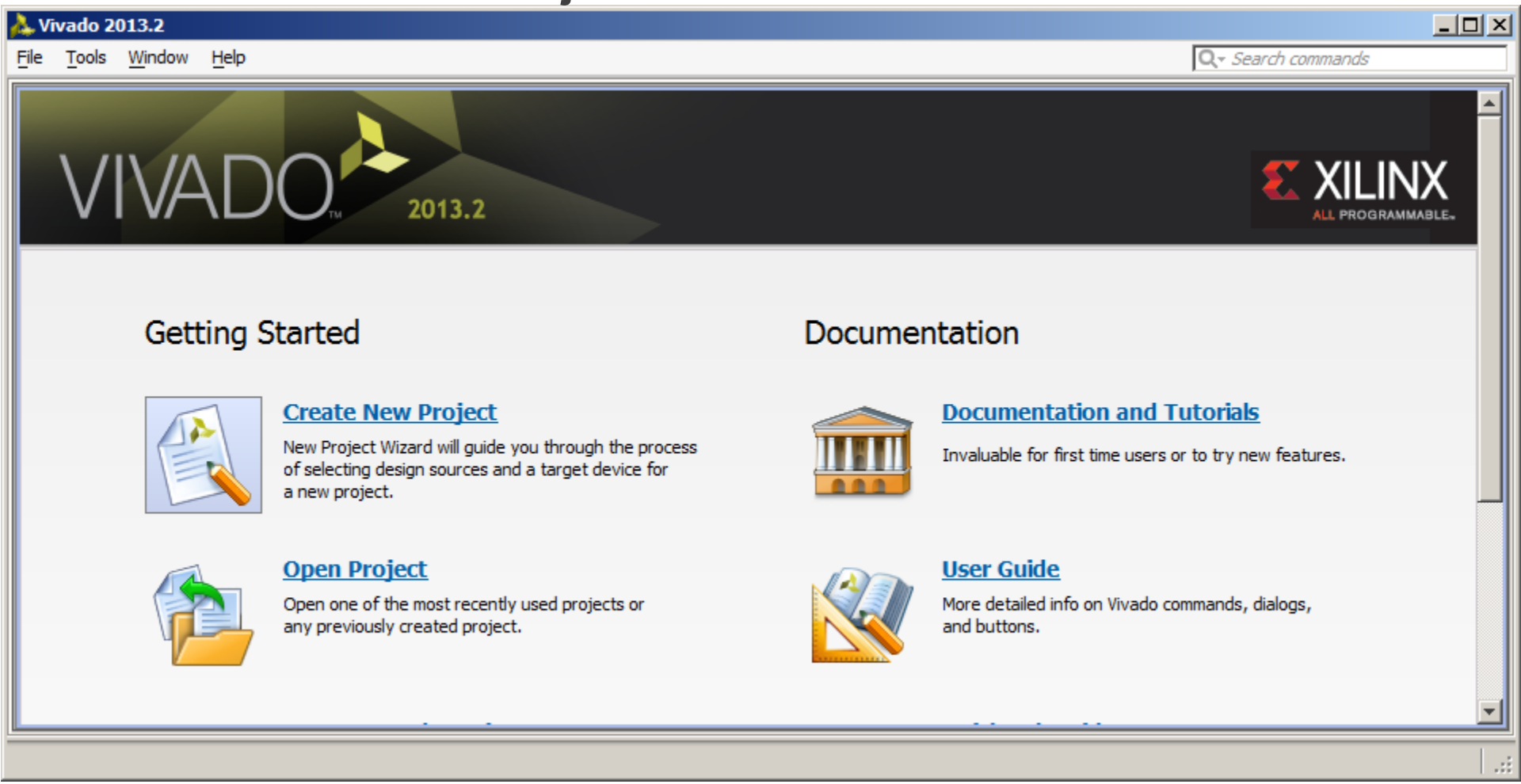
Note: Presentation applies to the KC705

Generate MIG Example Design

- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2013.2 → Vivado

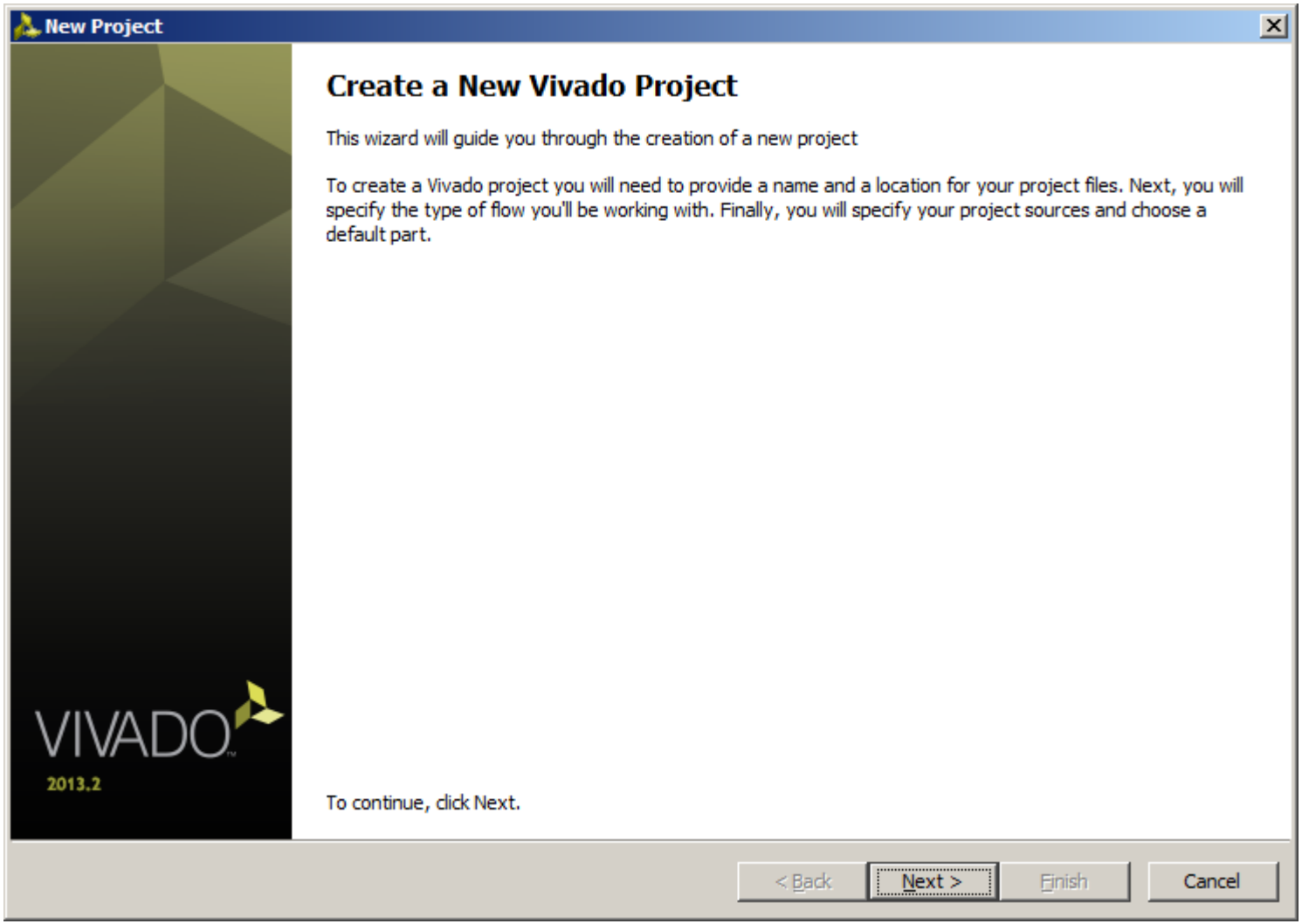
- Select Create New Project



Note: Presentation applies to the KC705

Generate MIG Example Design

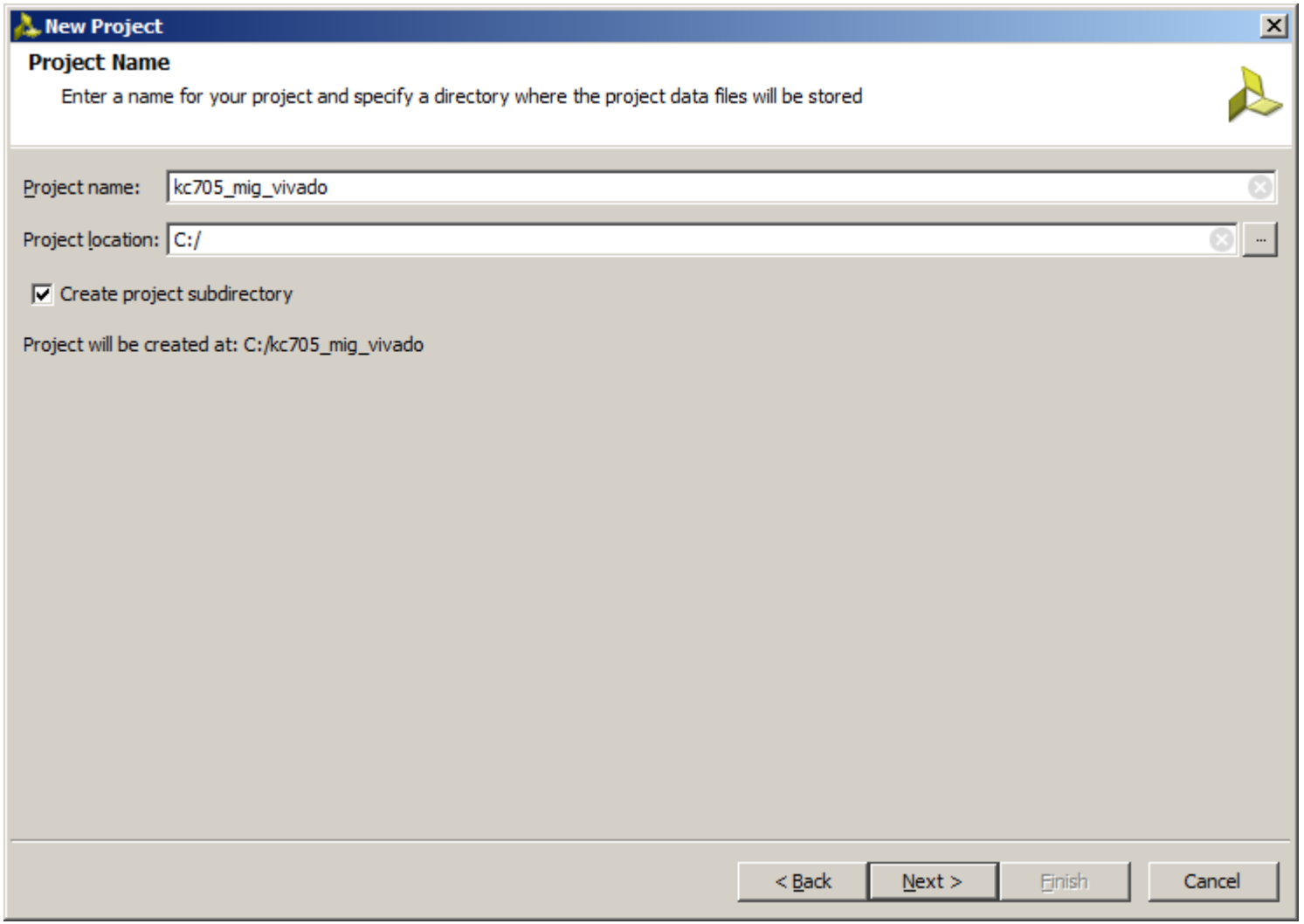
- Click Next



Note: Presentation applies to the KC705

Generate MIG Example Design

- **Set the Project name and location to kc705_mig_vivado and C:**
  - Check **Create Project Subdirectory**

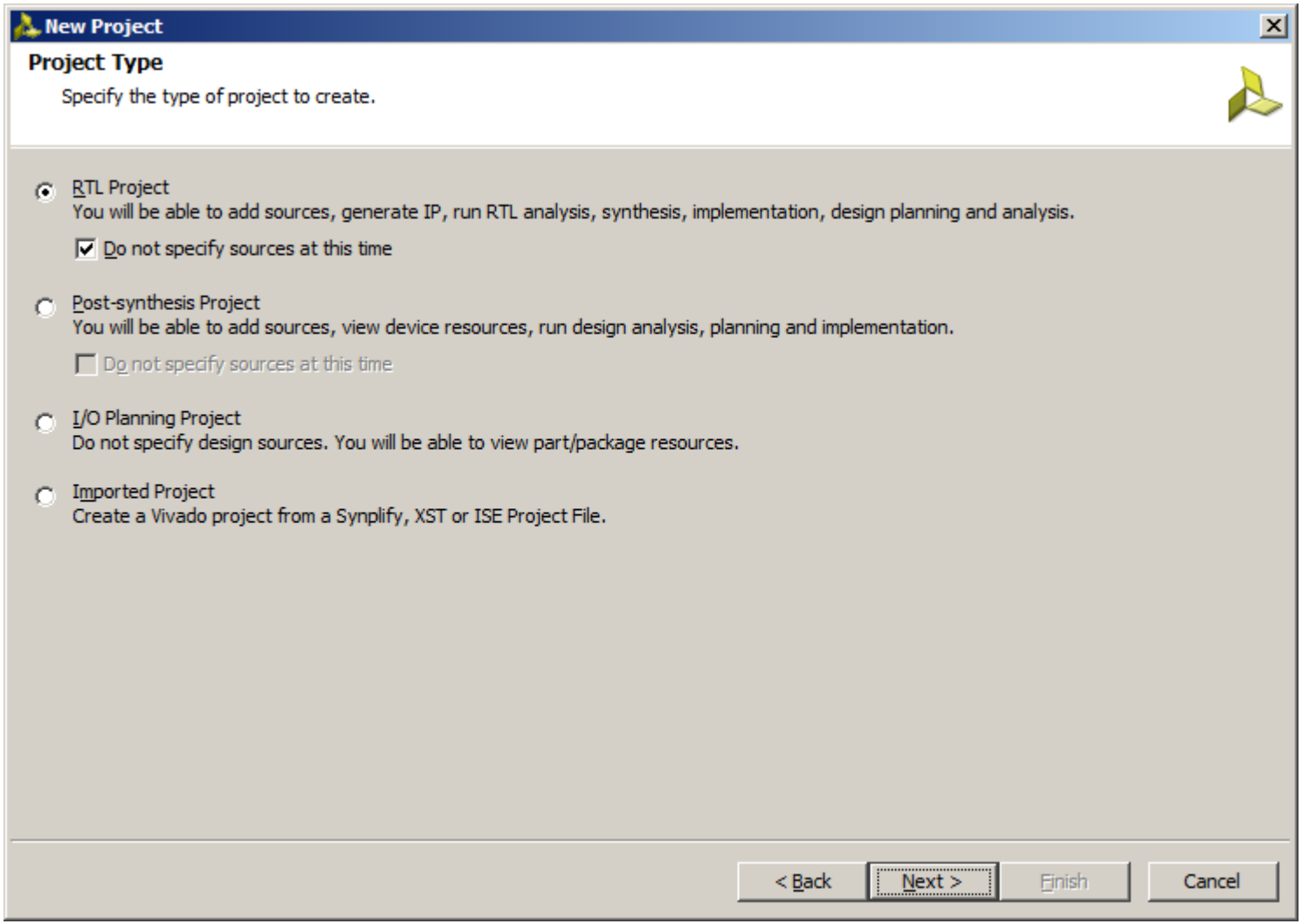


Note: Presentation applies to the KC705

Generate MIG Example Design

Select RTL Project

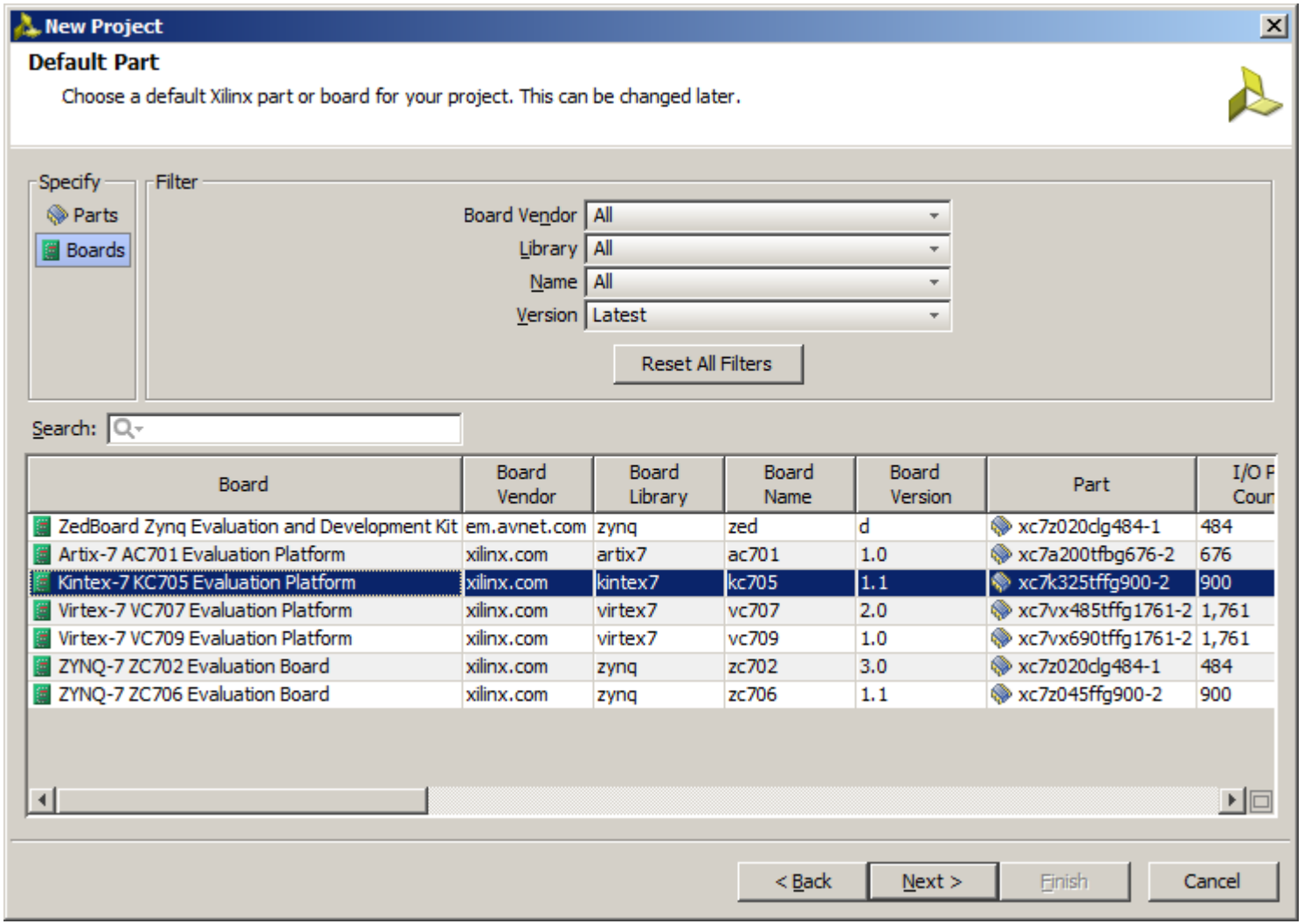
- Select **Do not specify sources at this time**



Note: Presentation applies to the KC705

Generate MIG Example Design

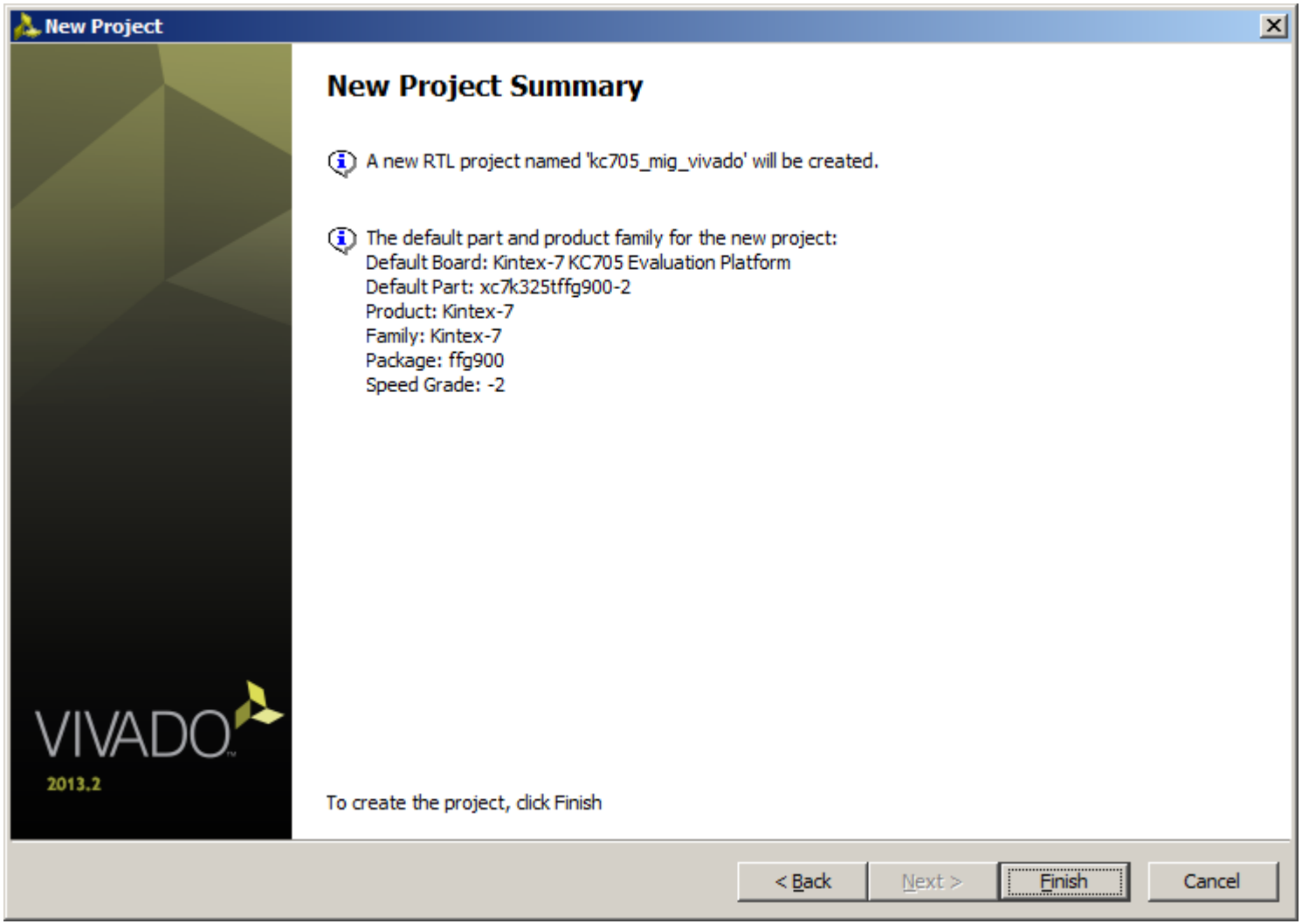
Select the KC705 Board



Note: Presentation applies to the KC705

Generate MIG Example Design

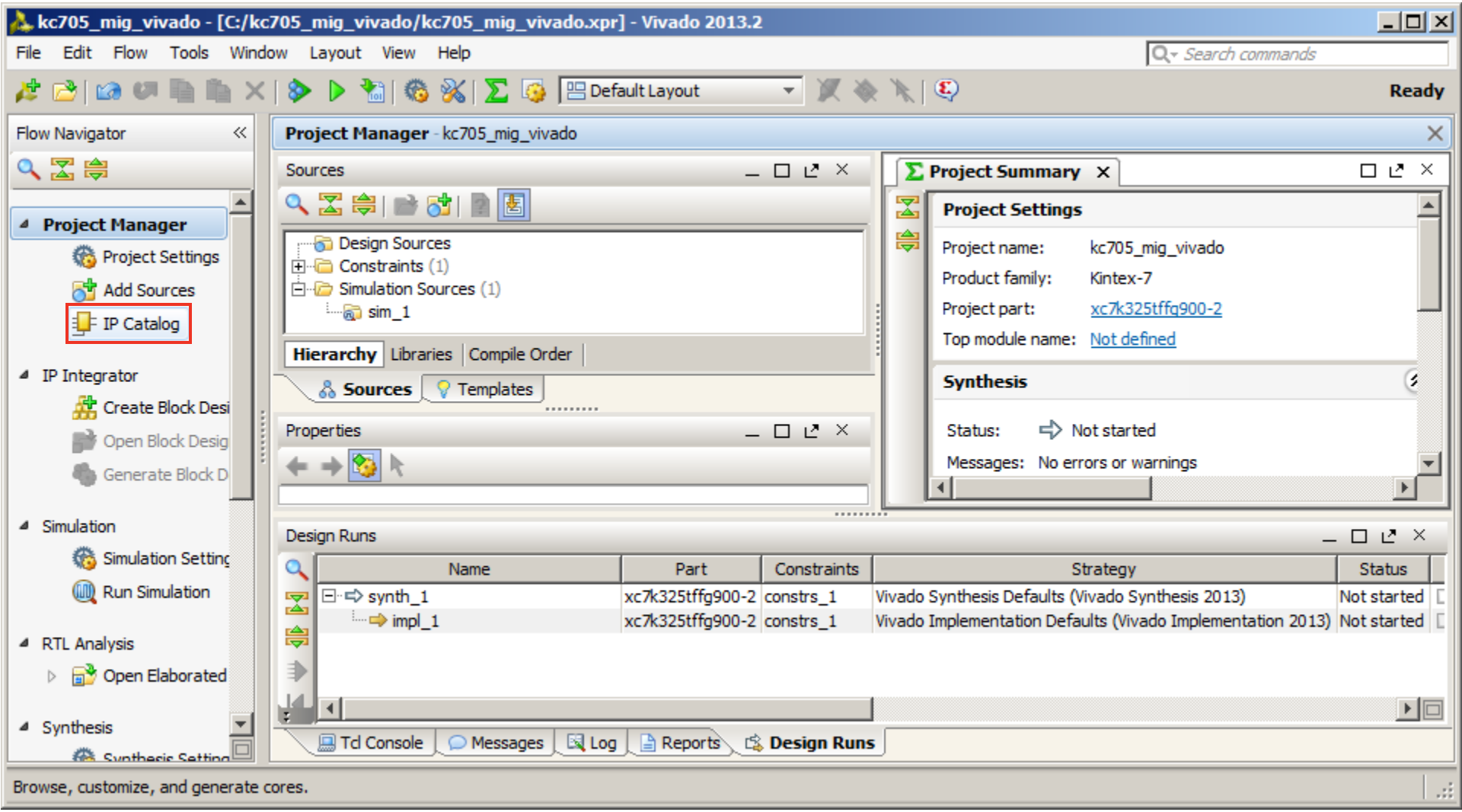
- Click Finish



Note: Presentation applies to the KC705

Generate MIG Example Design

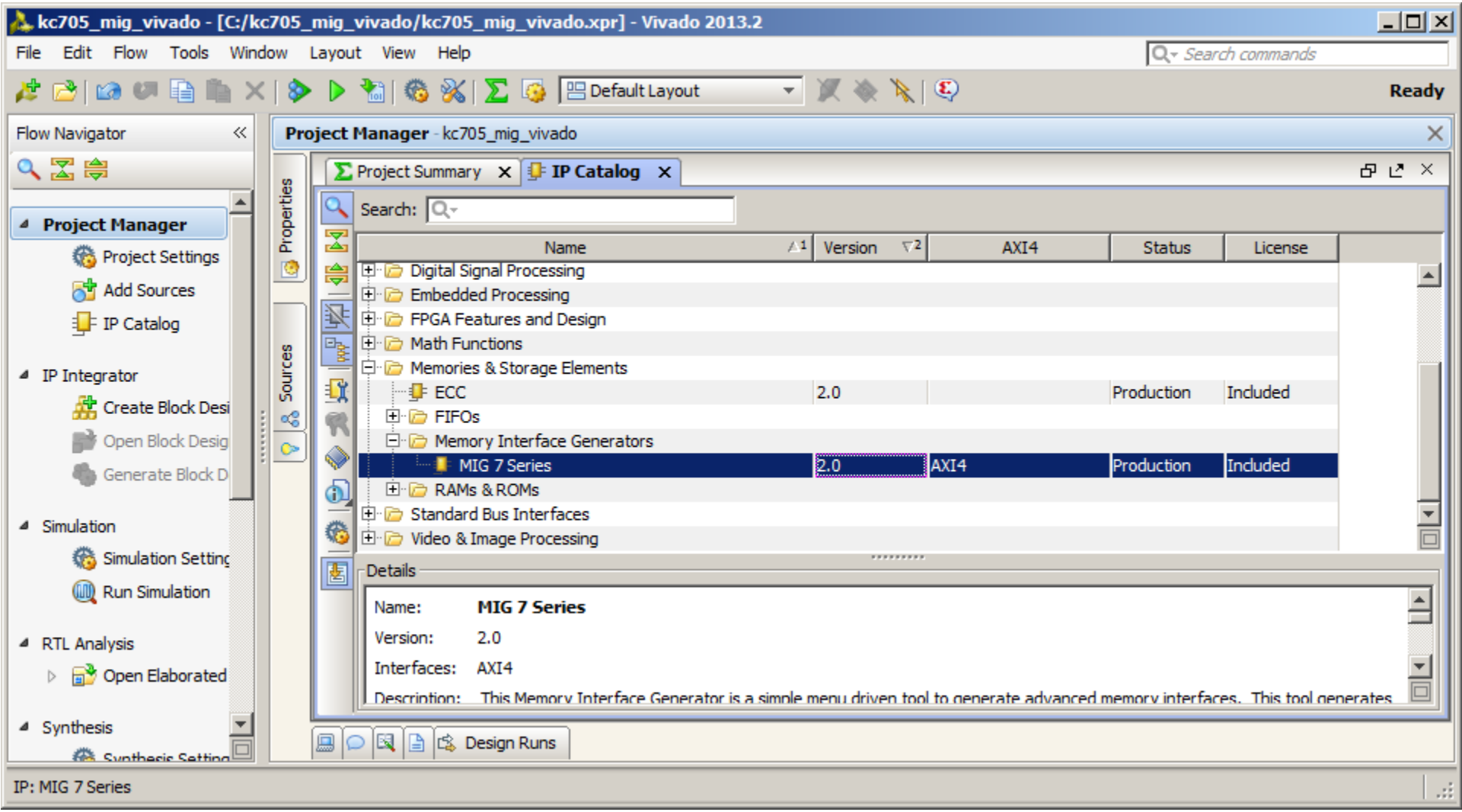
- Click on IP Catalog



Note: Presentation applies to the KC705

Generate MIG Example Design

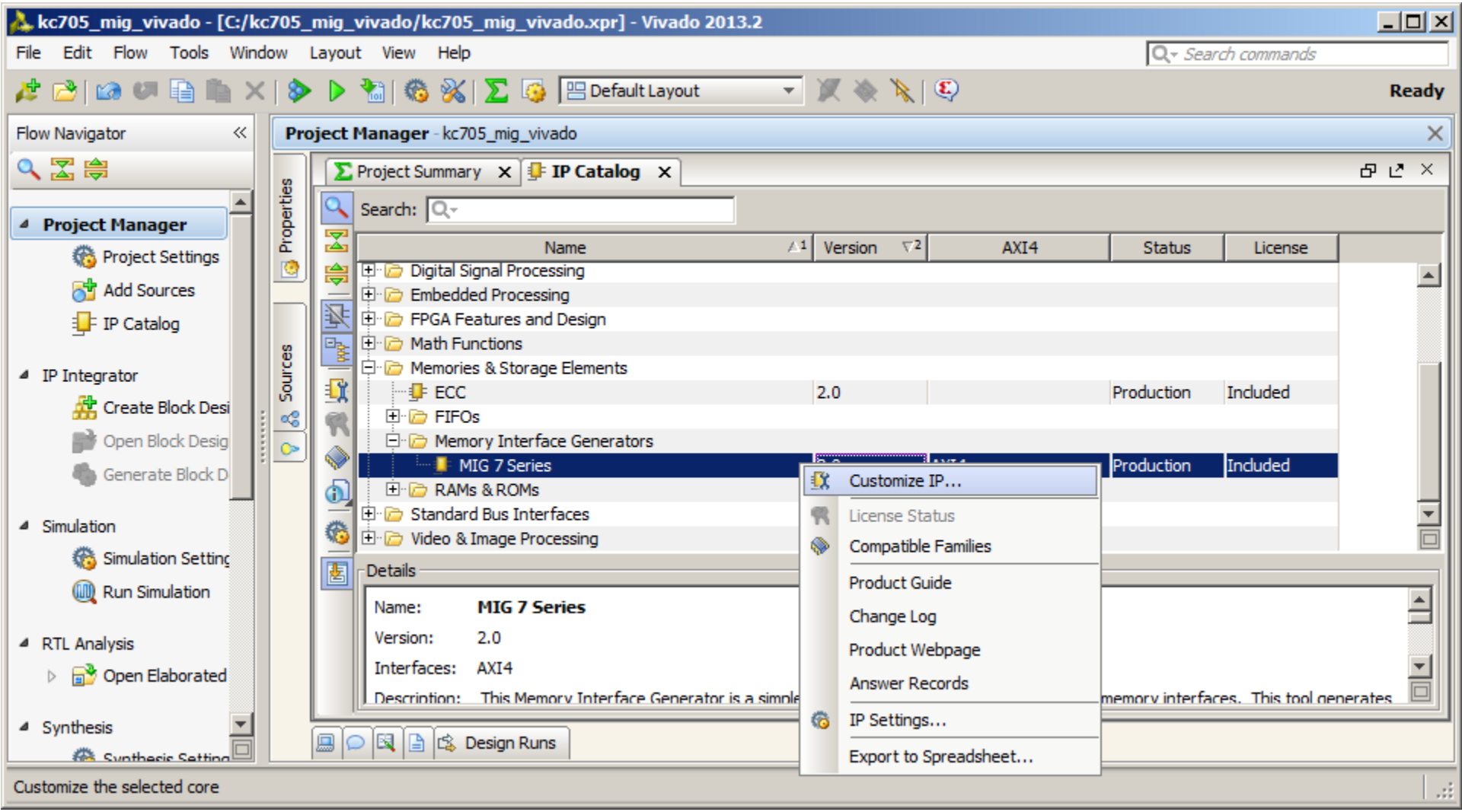
- Select MIG 7 Series, 2.0 under Memory Interface Generators



Note: Presentation applies to the KC705

Generate MIG Example Design

- Right click on MIG 7 Series Version
  - Select **Customize IP**



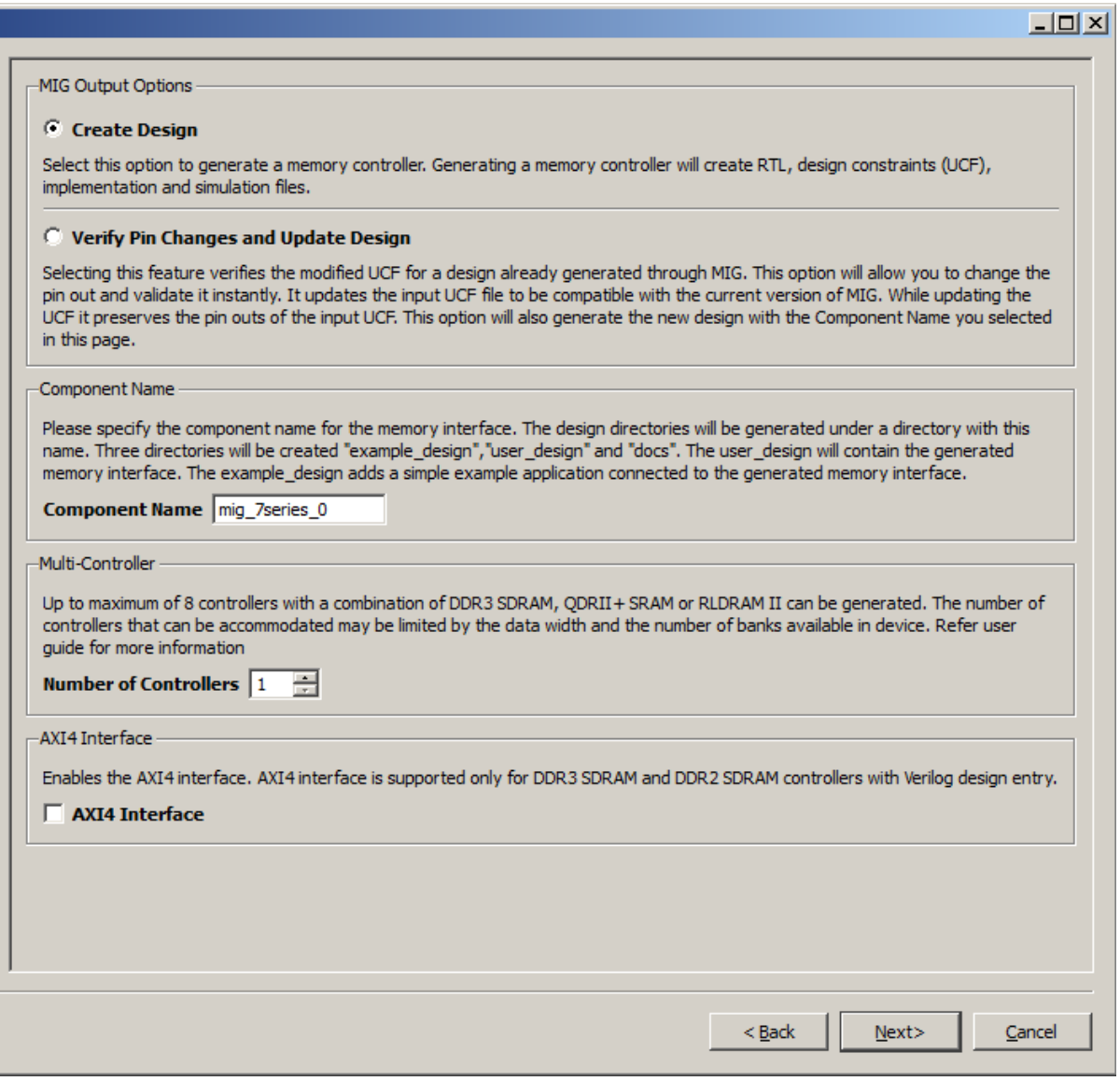
Note: Presentation applies to the KC705

Generate MIG Example Design

- Leave this page as is
  - Click Next

Note: Presentation applies to the KC705

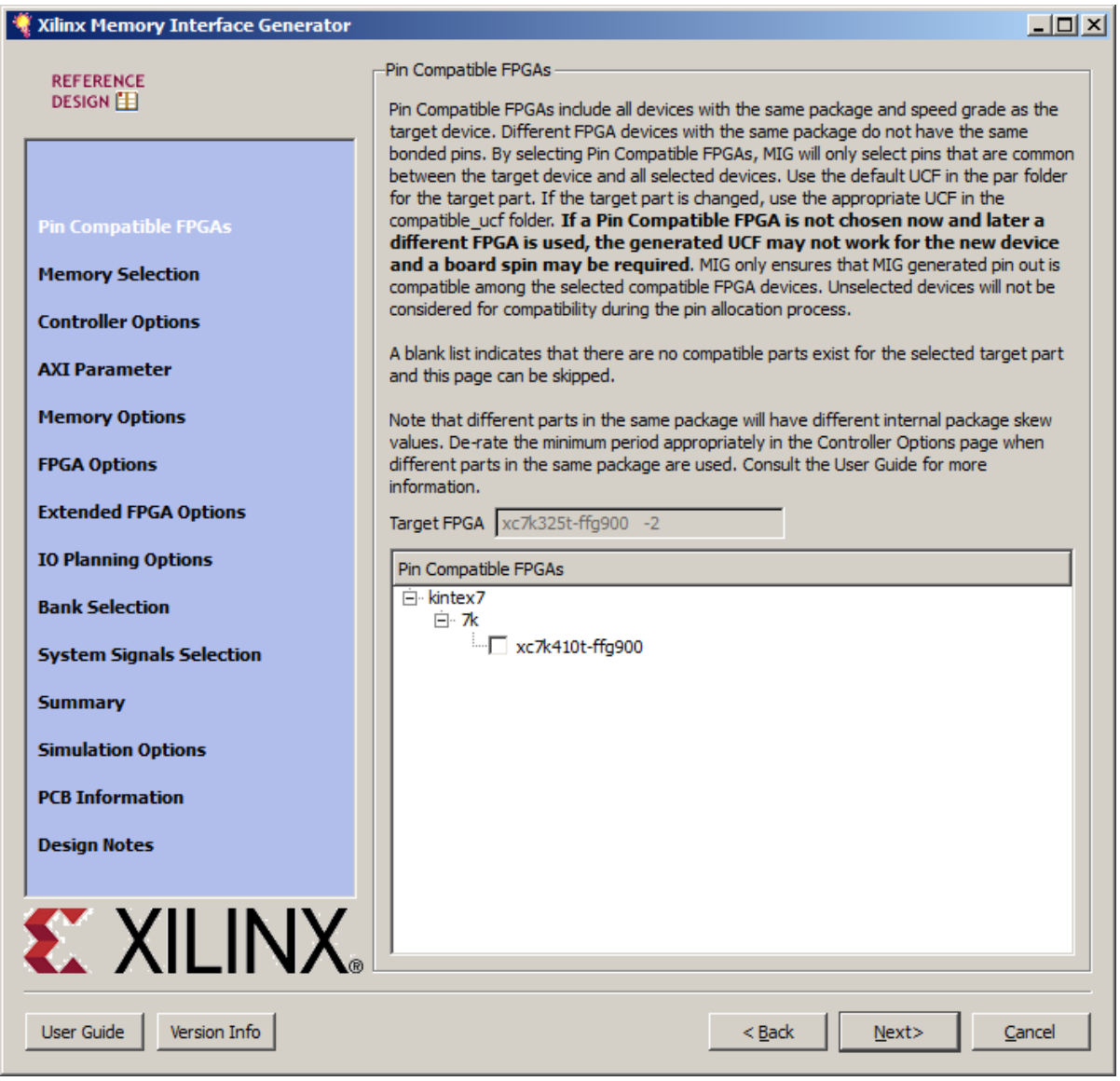
Generate MIG Example Design



- Leave this page as is
  - Click Next

Note: Presentation applies to the KC705

Generate MIG Example Design



- Leave this page as is
  - Click Next

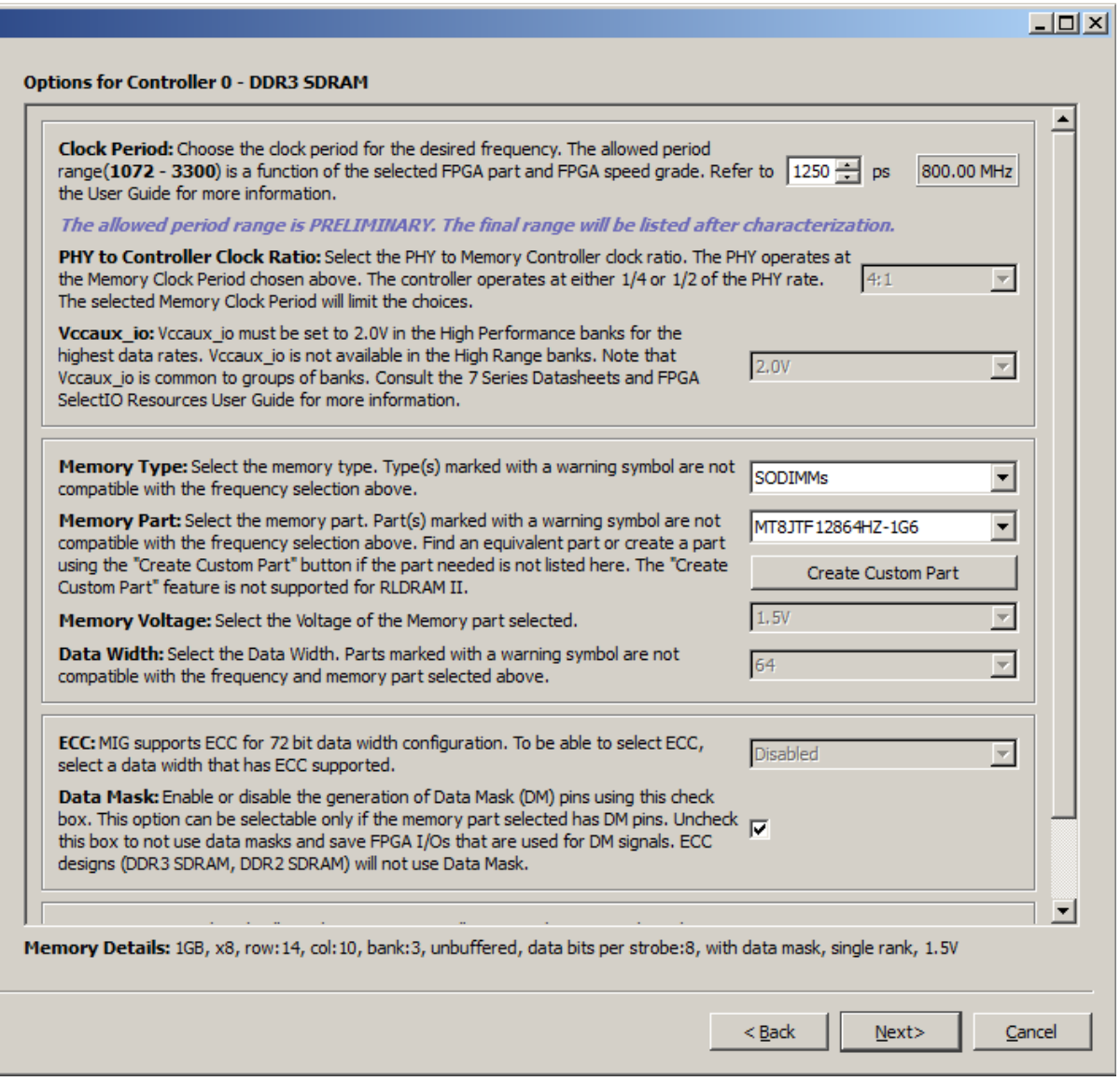
Note: Presentation applies to the KC705

Generate MIG Example Design

- **Select Memory Type**
  - DDR3 SDRAM
  - Click Next

Note: Presentation applies to the KC705

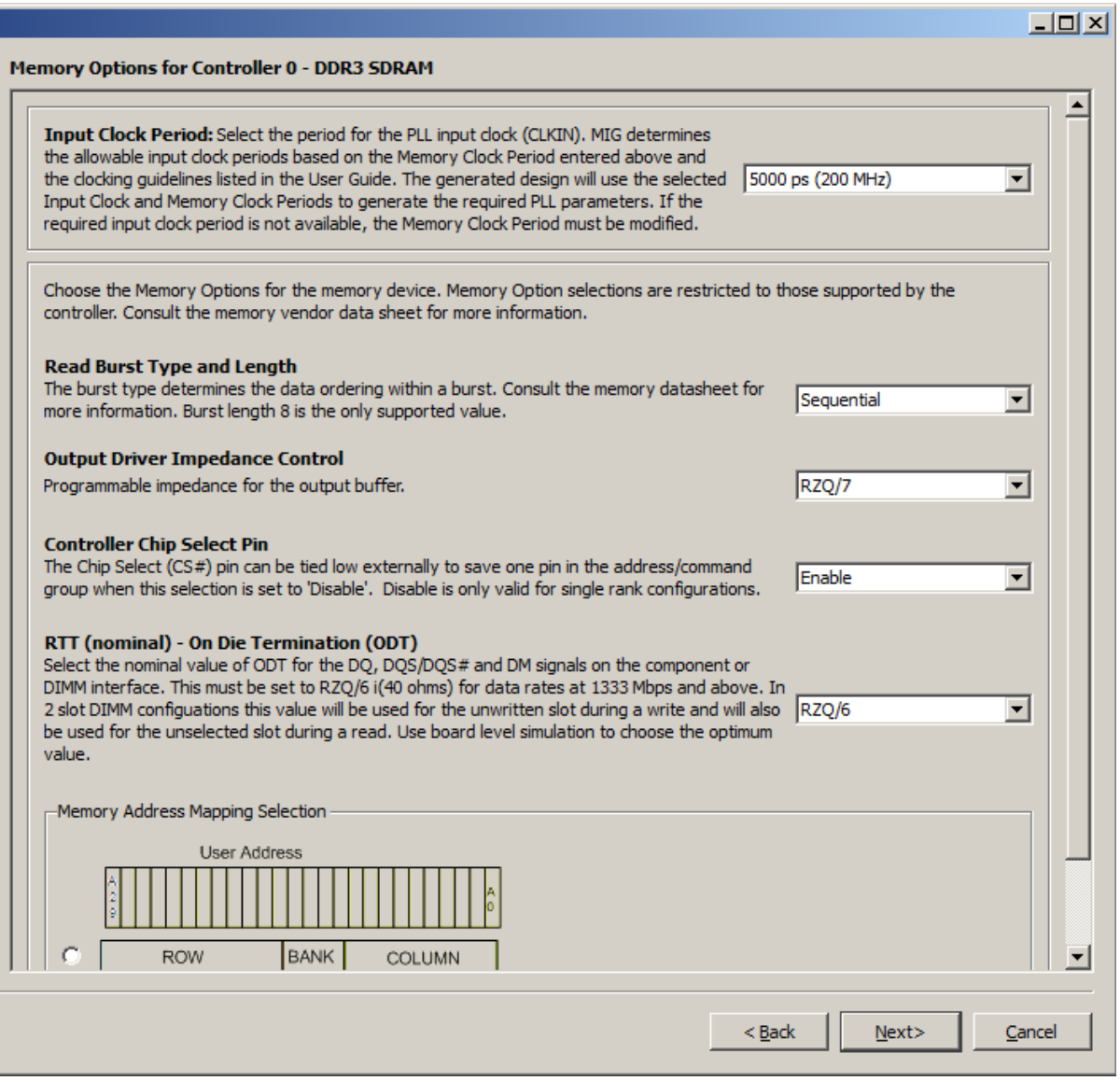
Generate MIG Example Design



- **Select**
  - Clock Period: **1250 ps**
  - Type: **SODIMMs**
  - Part: **MT8JTF12864HZ-1G6**
  - Data Mask: **Checked**
  - Click Next

Note: Presentation applies to the KC705

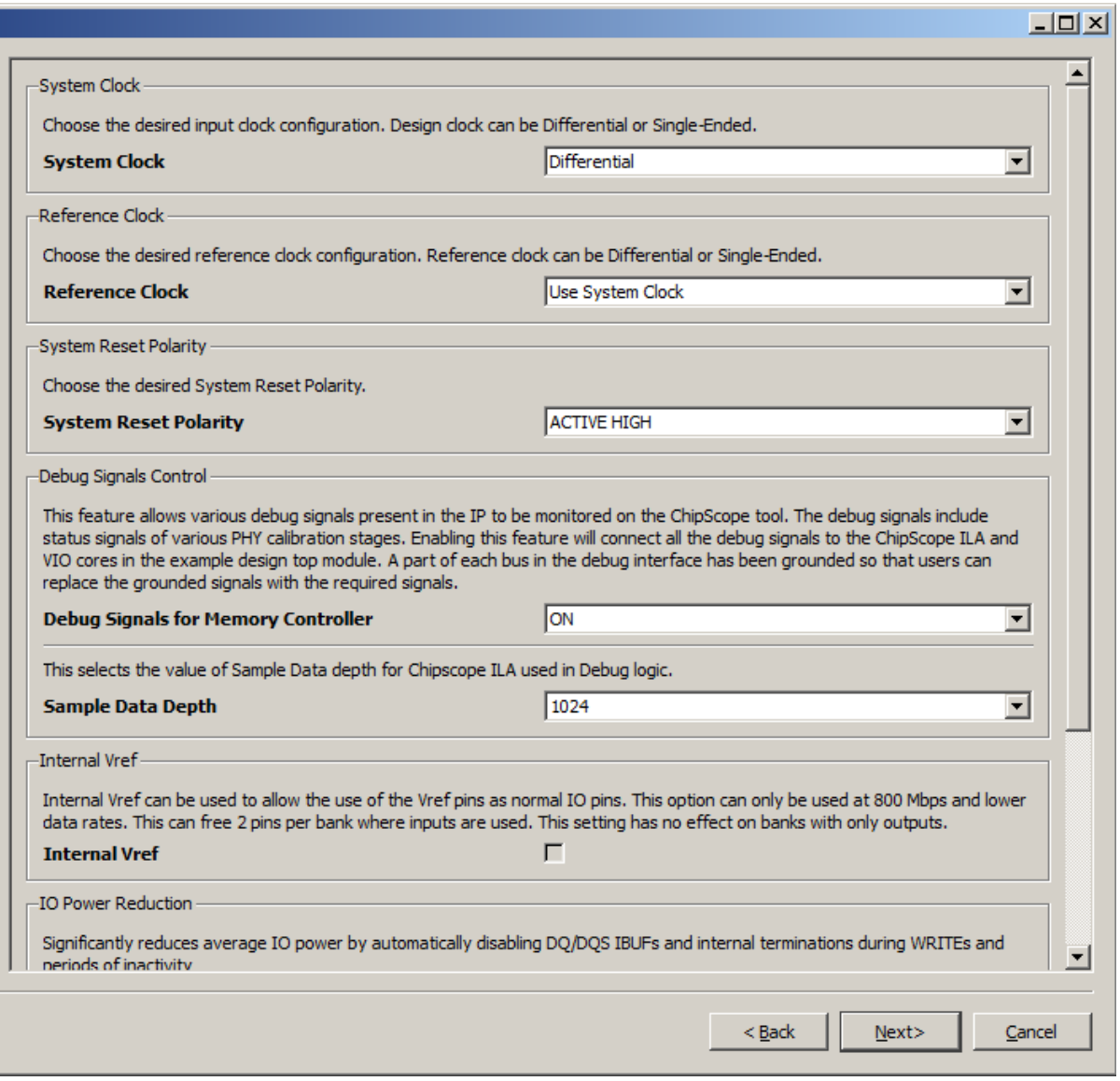
Generate MIG Example Design



- **Select:**
  - Input Clock Period: **5000 ps**
  - RTT: **RZQ/6**
  - Click Next

Note: Presentation applies to the KC705

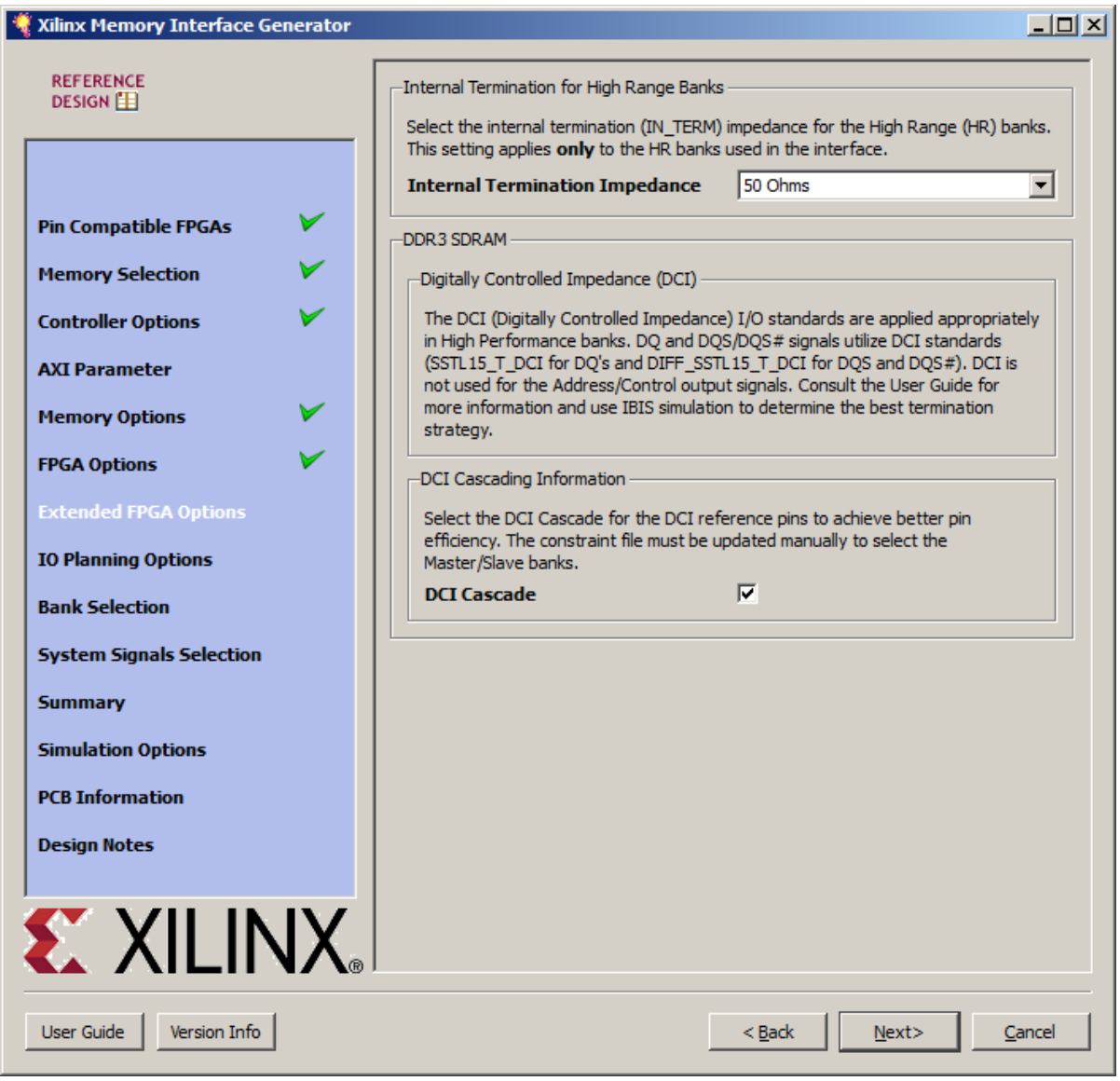
Generate MIG Example Design



- **Select**
  - Reference Clock: **Use System Clock**
  - System Reset: **ACTIVE HIGH**
  - Debug: **ON**
  - Click Next

Note: Presentation applies to the KC705

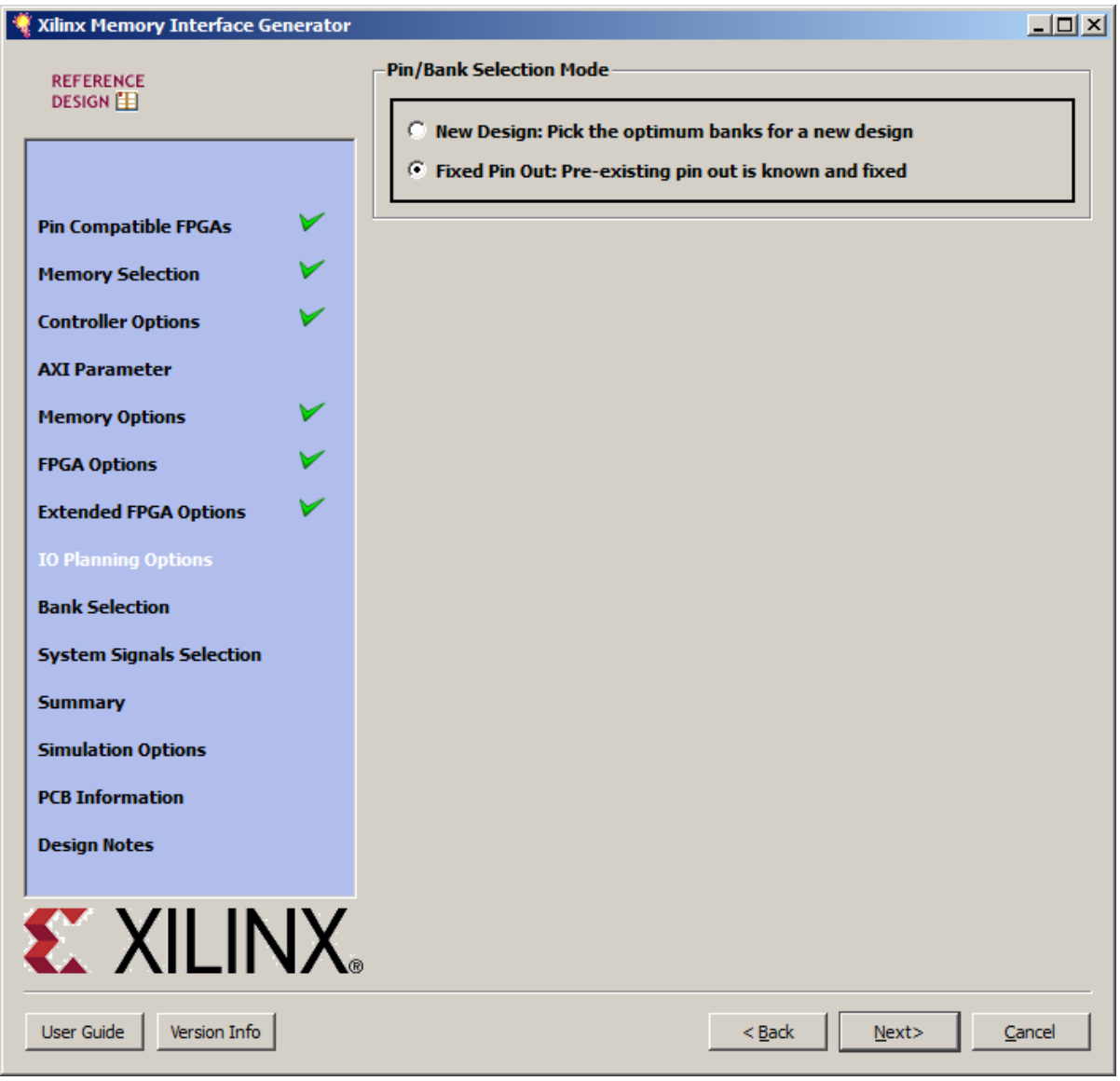
Generate MIG Example Design



- **Select**
  - DCI Cascade: **Checked**
  - Click Next

Note: Presentation applies to the KC705

Generate MIG Example Design

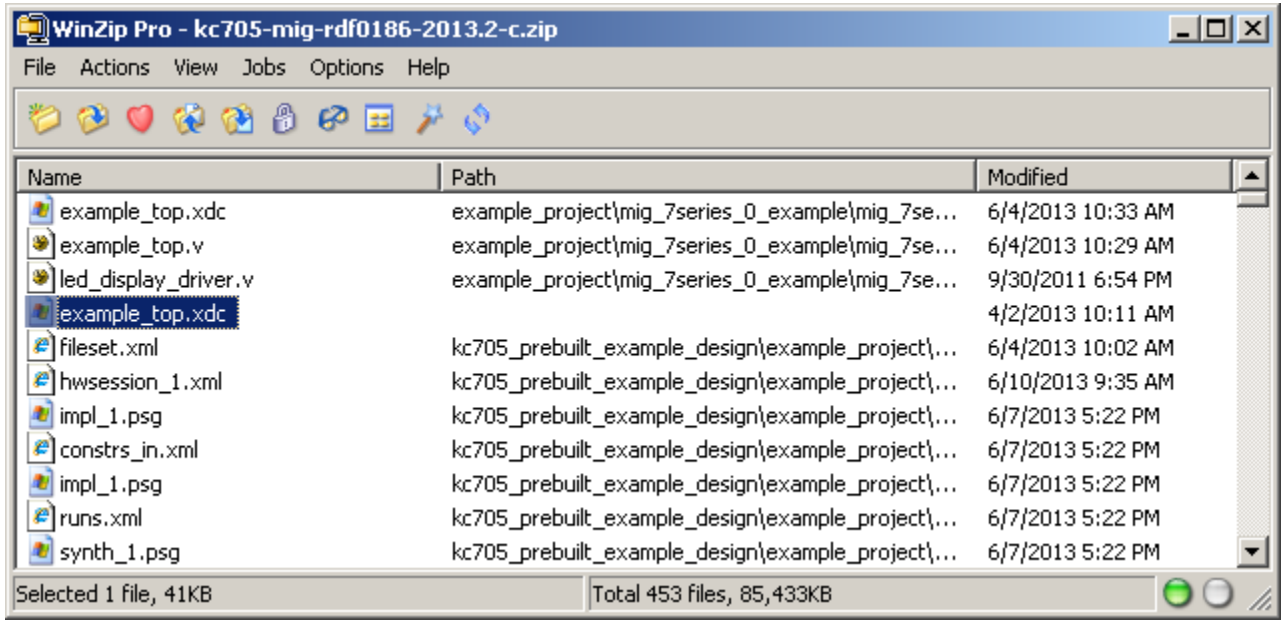


- **Select Fixed Pin Out**
  - Click Next

Note: Presentation applies to the KC705

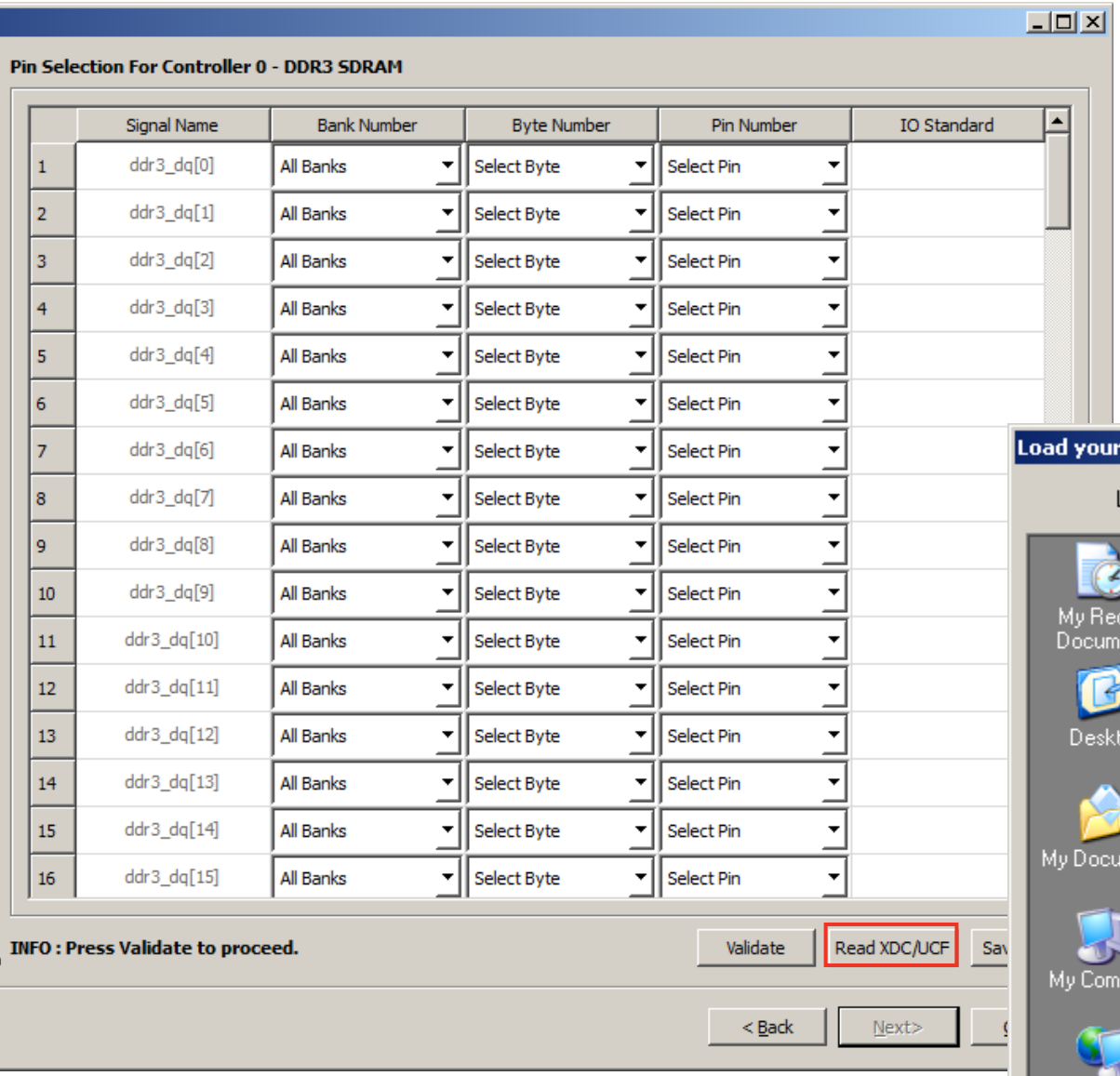
Modifications to Example Design

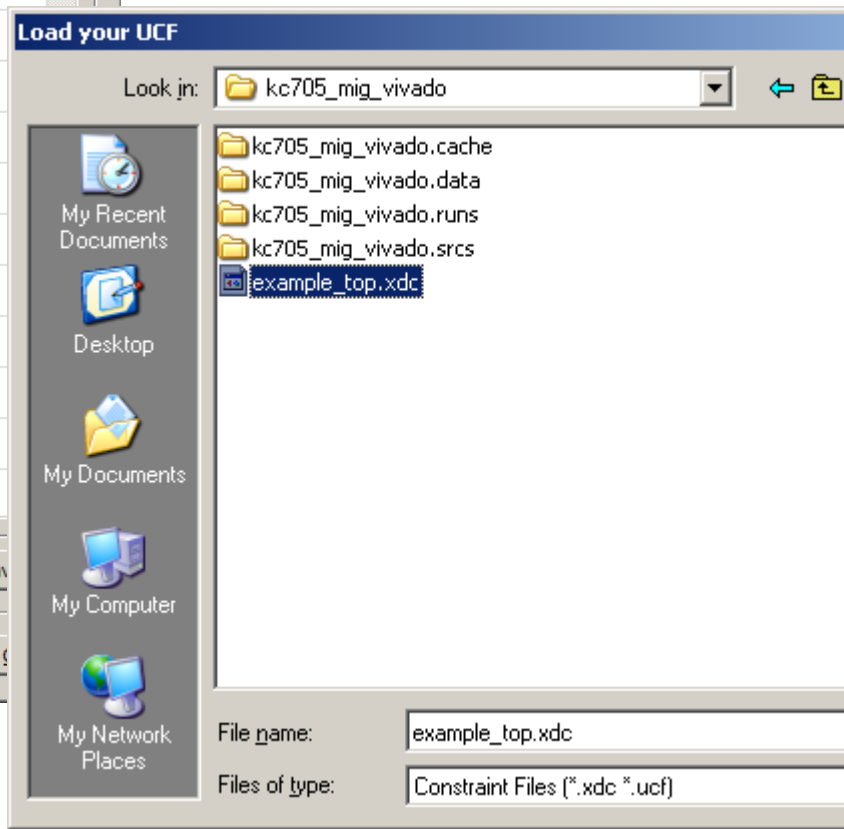
- **Open the KC705 MIG Vivado Design Files (2013.2 C)**
  - Available through http://www.xilinx.com/kc705
  - Extract the file, "**example_top.xdc**" *only* to C:\kc705_mig_vivado
  - Contains the constraints needed for KC705 MIG design
  - This zip file will be needed later in the presentation



Note: Presentation applies to the KC705

Generate MIG Example Design

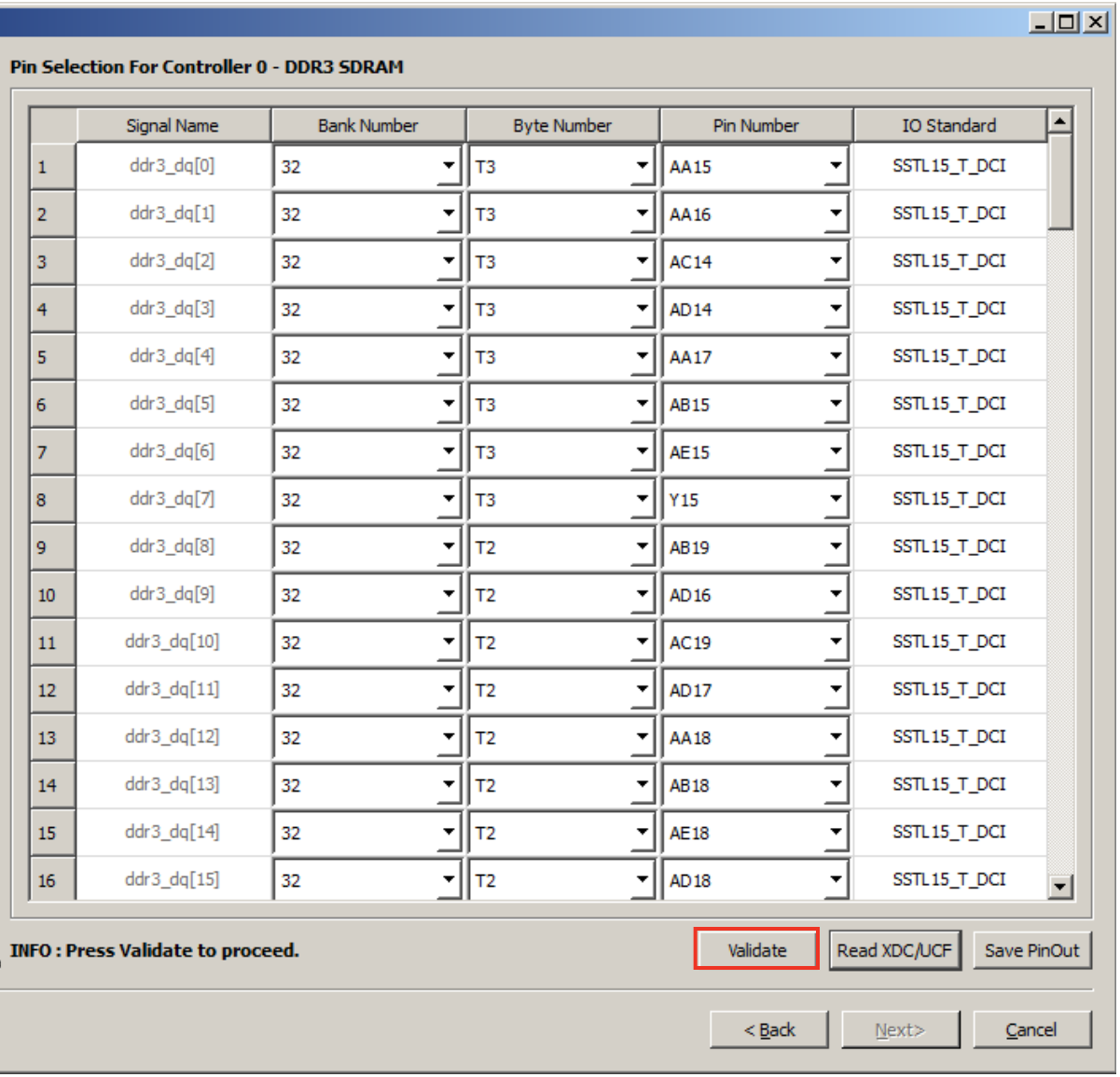




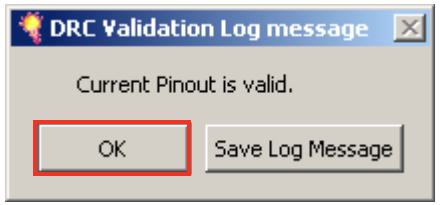
- **Select Read XDC/UCF**
  - Open the file: example_top.xdc

Note: Presentation applies to the KC705

Generate MIG Example Design

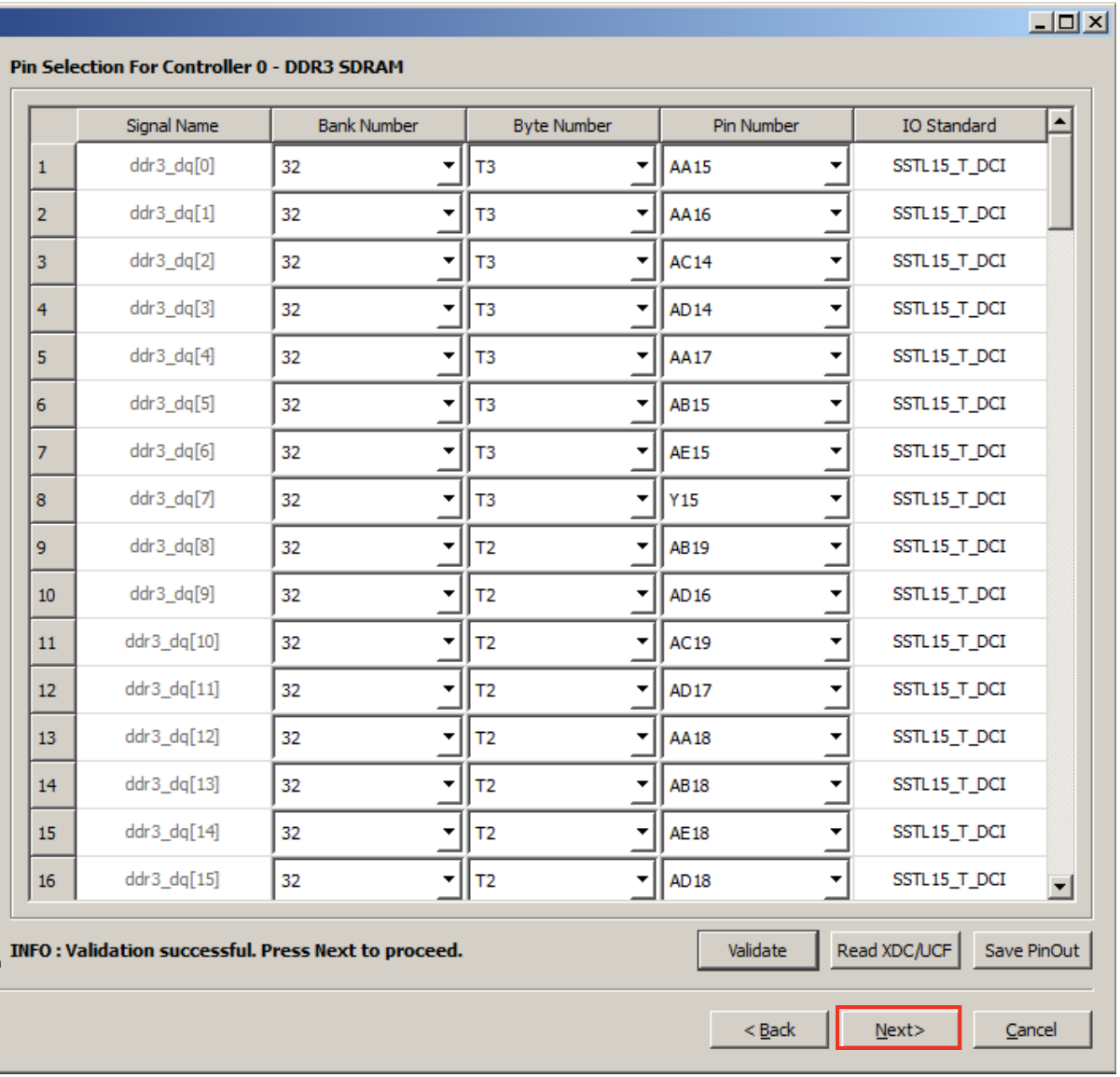


- Once it finishes reading in the XDC, click Validate
  - Click OK



Note: Presentation applies to the KC705

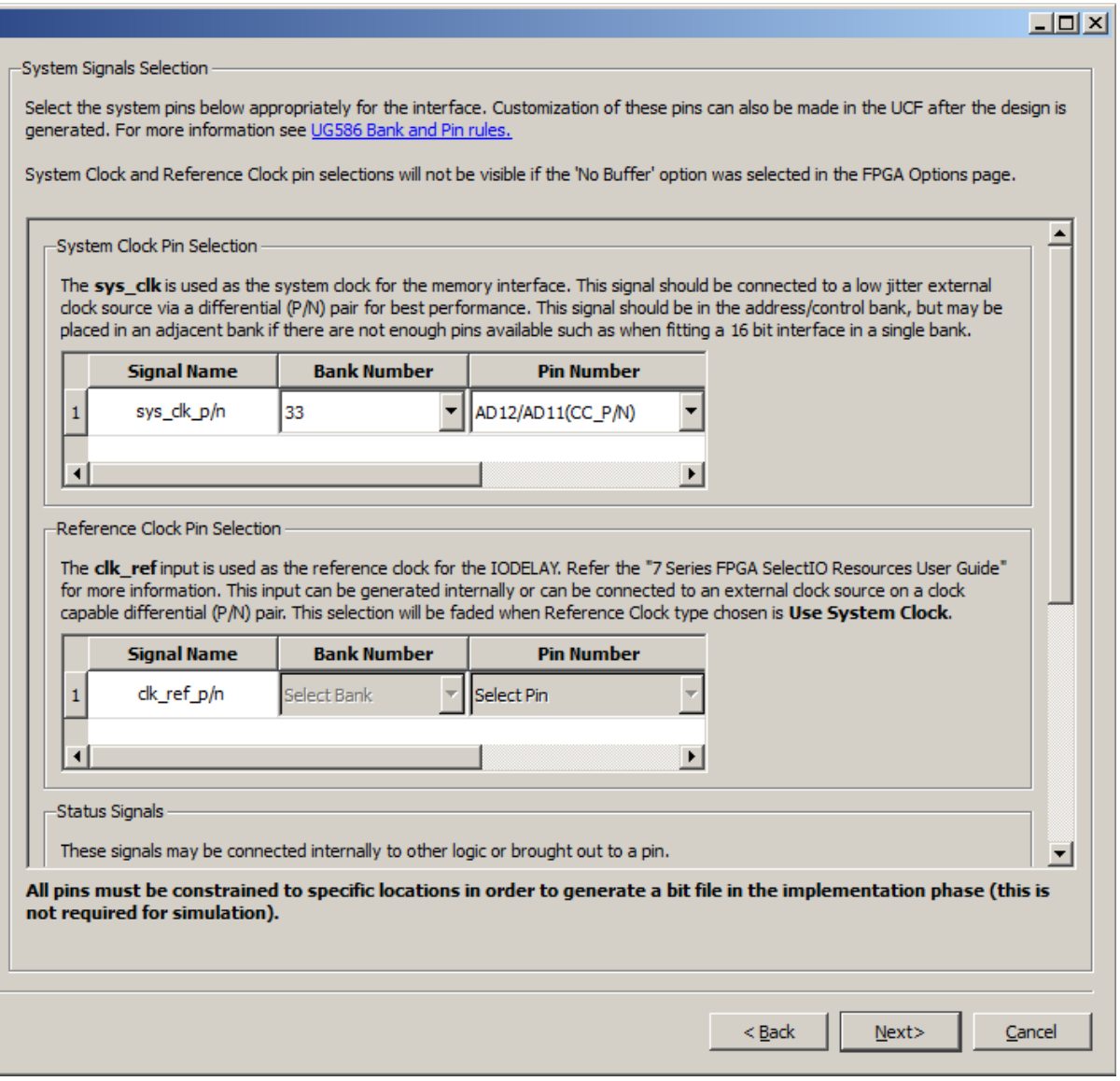
Generate MIG Example Design



- **The Next button is enabled once the pinout is validated.**
  - Click Next

Note: Presentation applies to the KC705

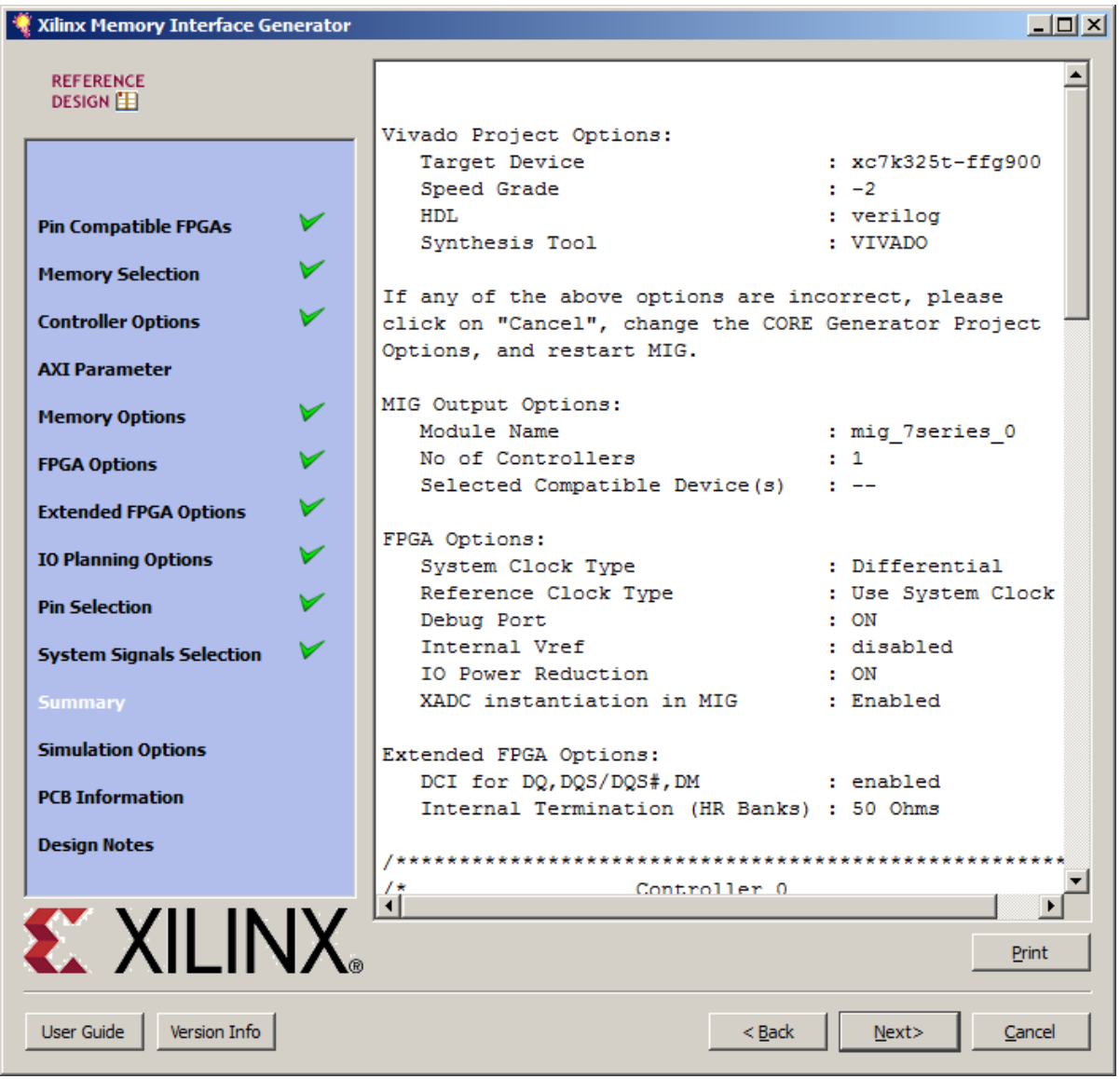
Generate MIG Example Design



- **Leave this page as is**
  - Click Next

Note: Presentation applies to the KC705

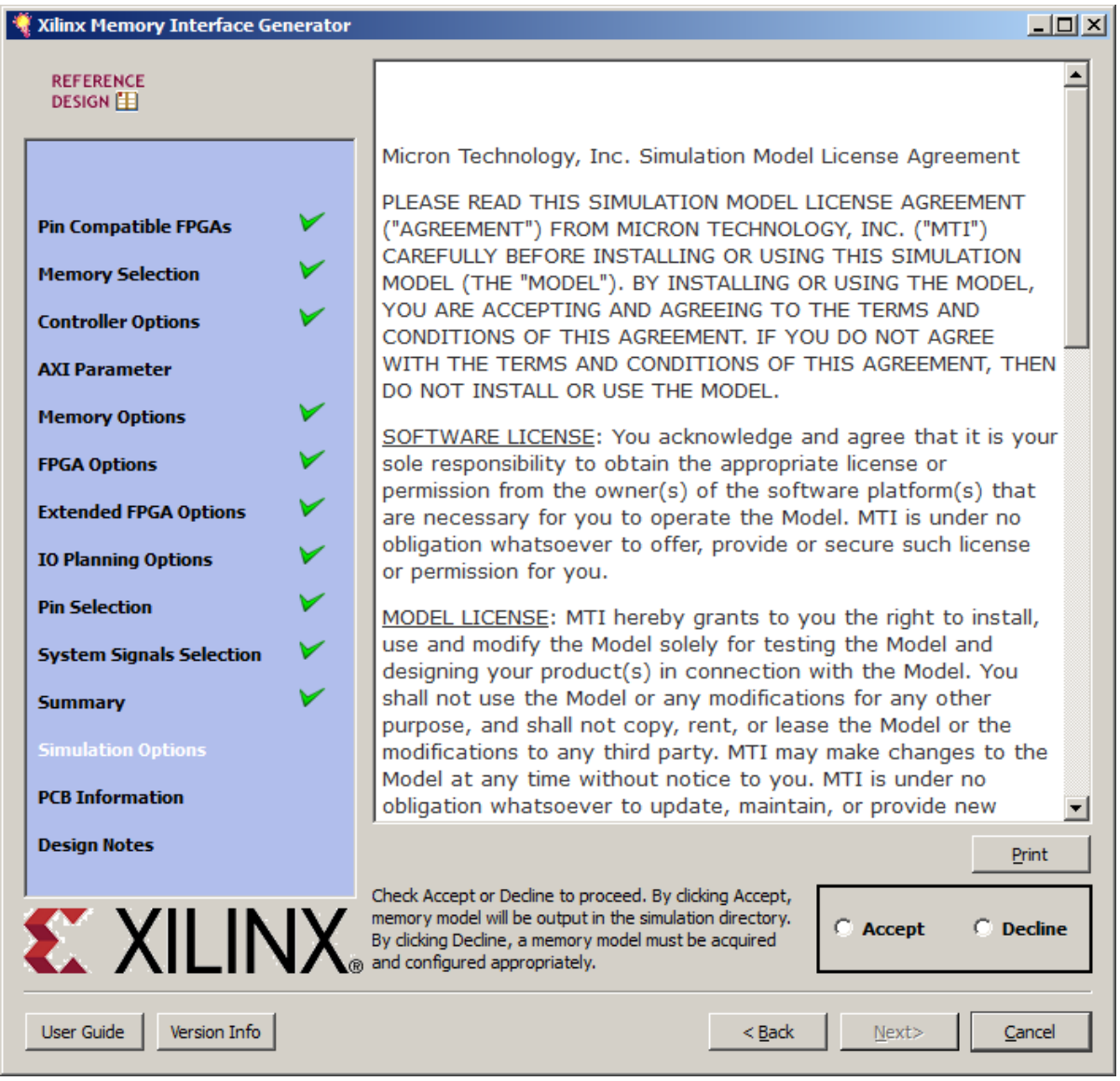
Generate MIG Example Design



- Leave this page as is
  - Click Next

Note: Presentation applies to the KC705

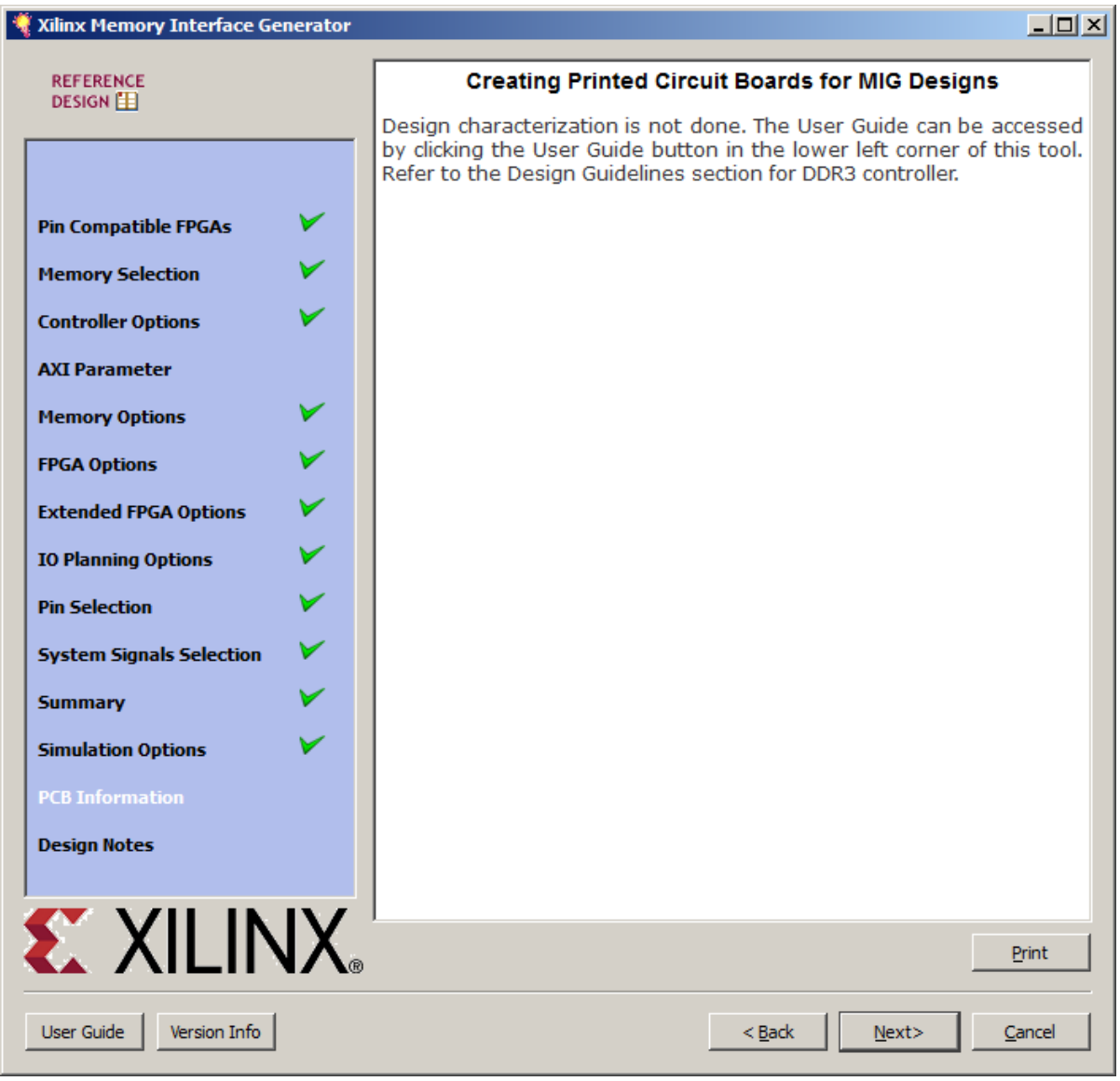
Generate MIG Example Design



- **Accept Simulation license, if desired**
  - Otherwise, Decline license
  - Click Next

Note: Presentation applies to the KC705

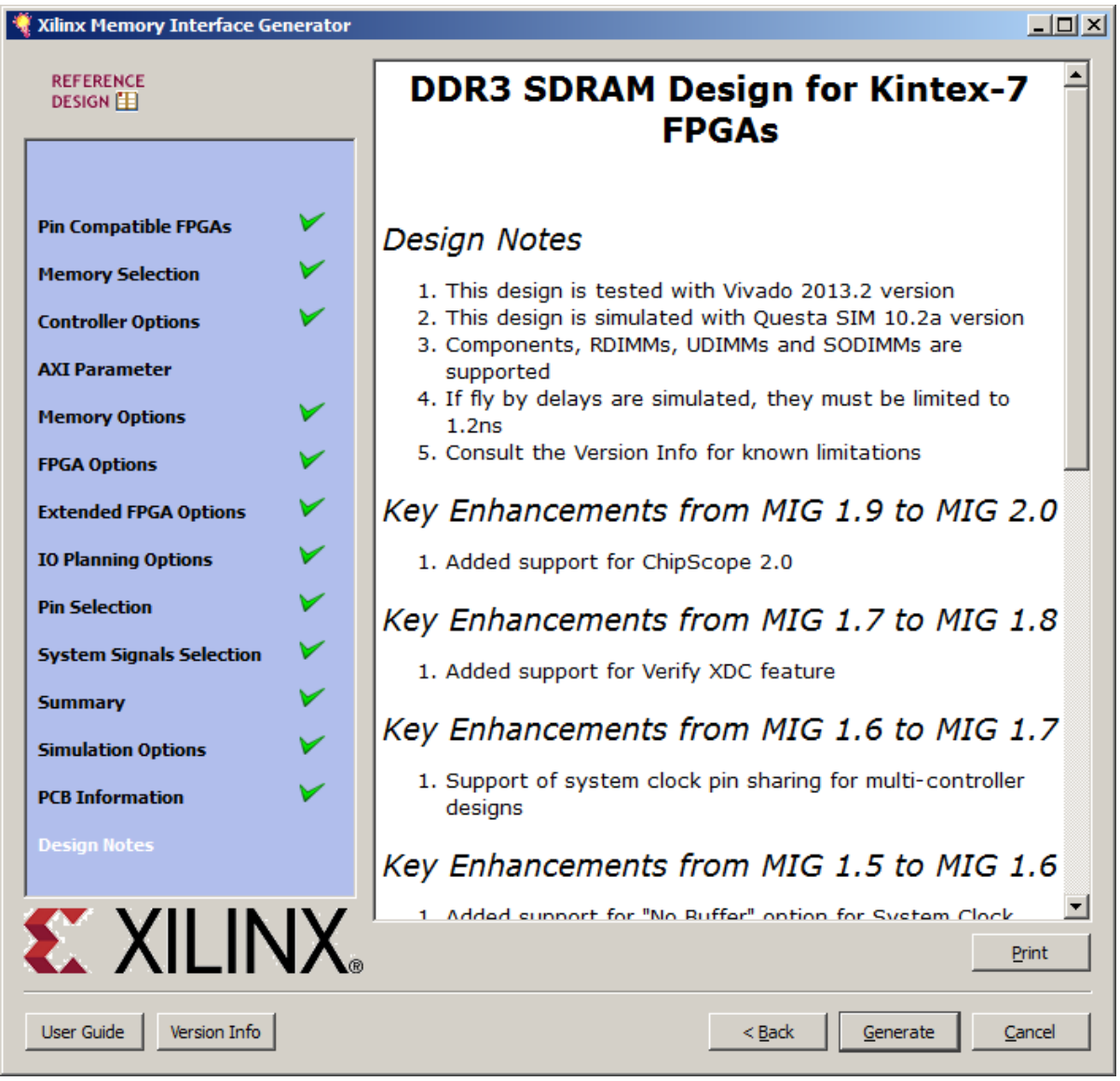
Generate MIG Example Design



- Leave this page as is
  - Click Next

Note: Presentation applies to the KC705

Generate MIG Example Design

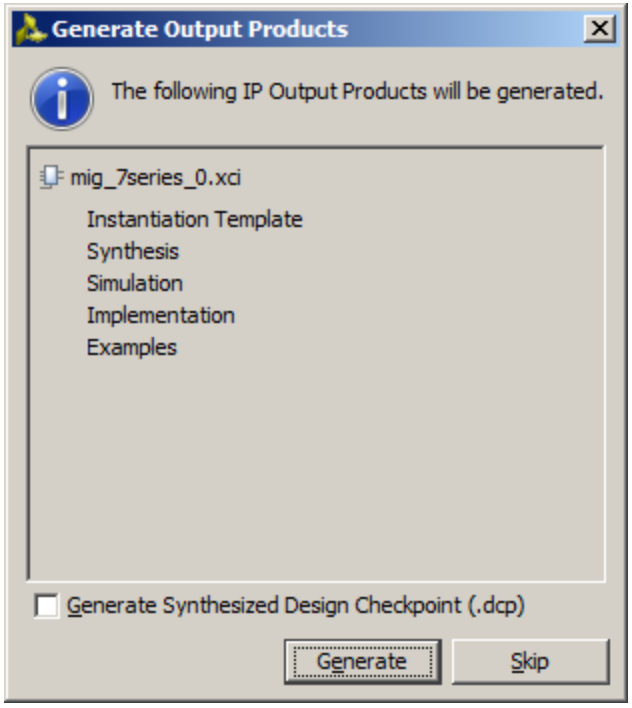


- Click Generate

Note: Presentation applies to the KC705

Generate MIG Example Design

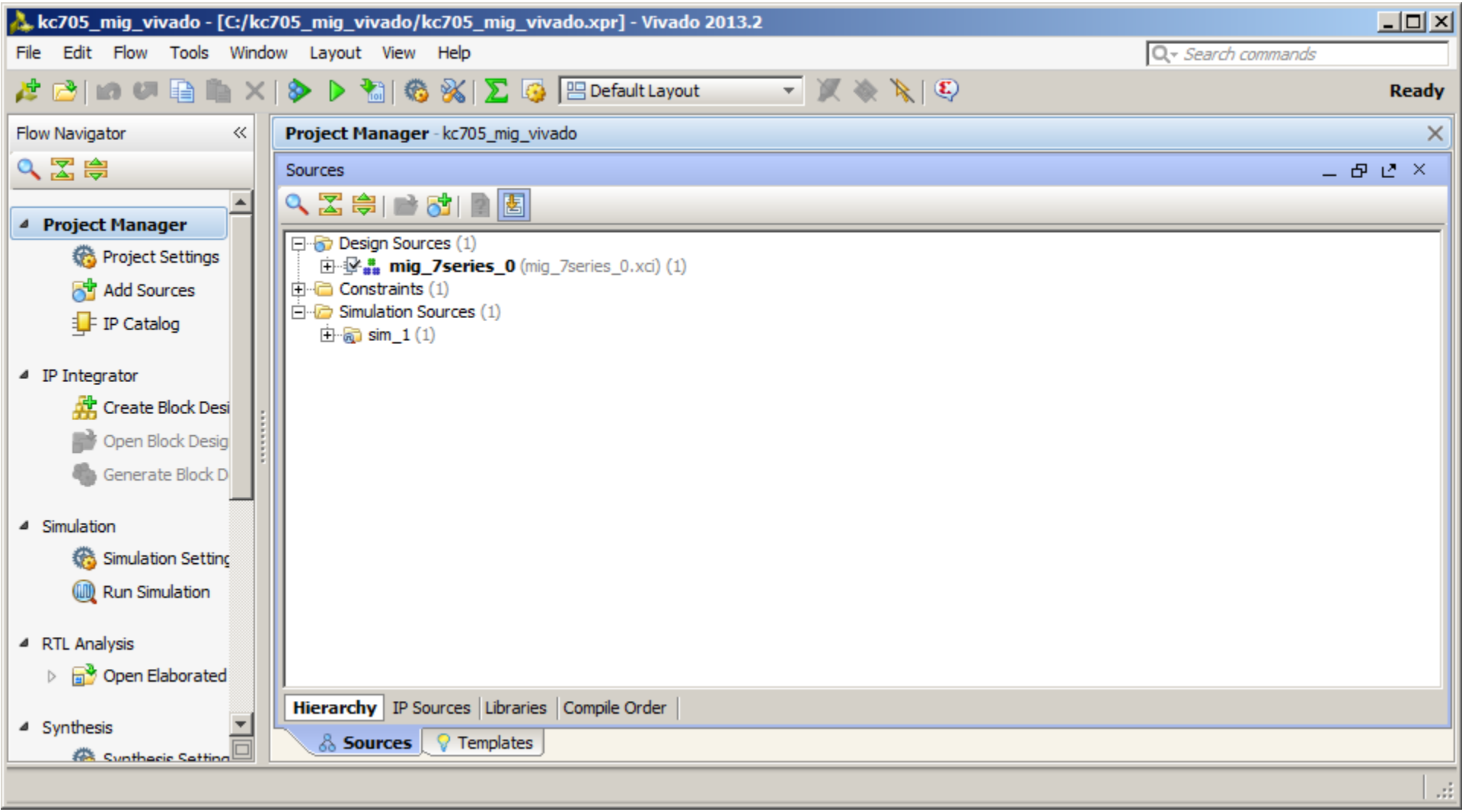
- Click Generate



Note: Presentation applies to the KC705

Generate MIG Example Design

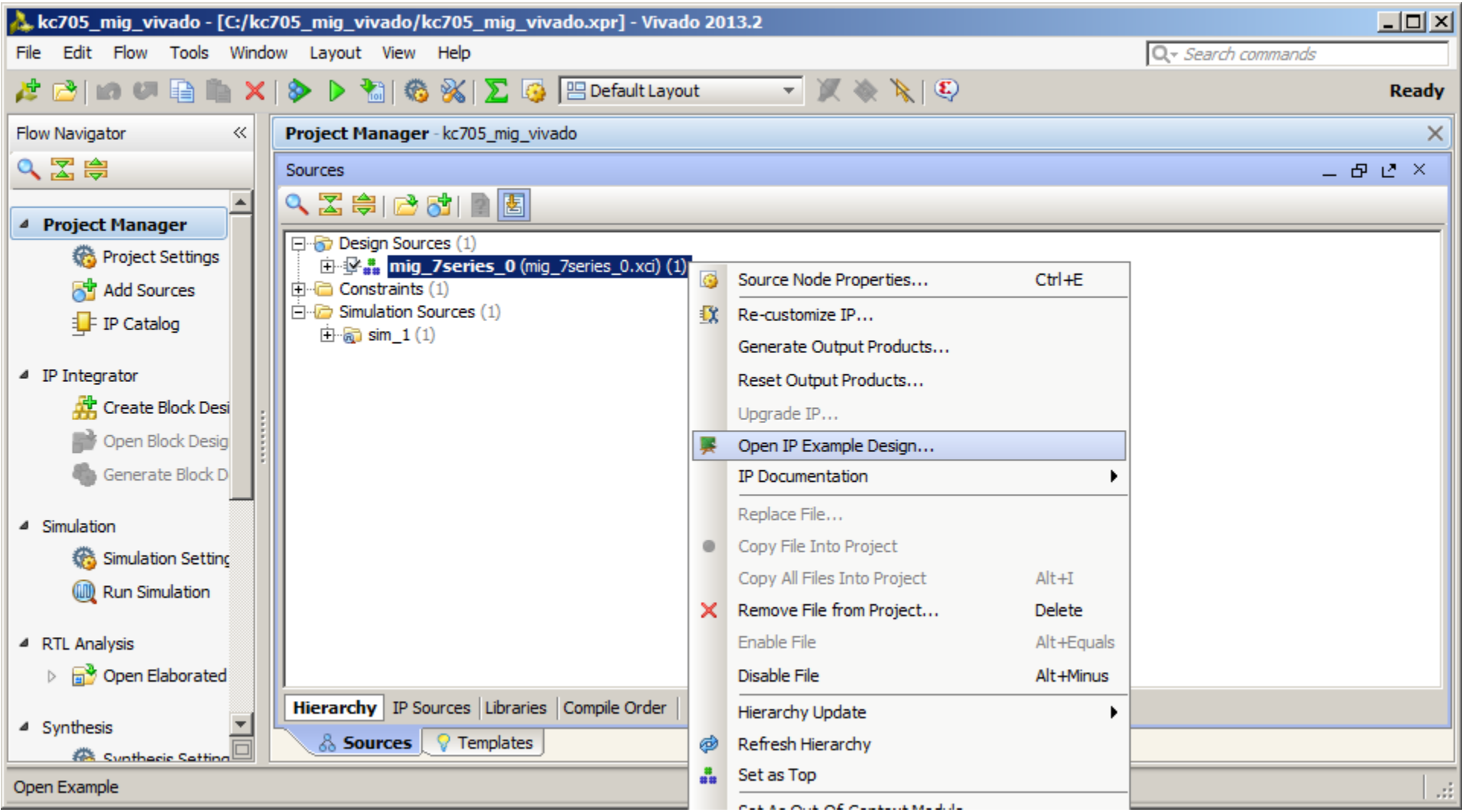
- MIG design appears in Design Sources



Note: Presentation applies to the KC705

Compile Example Design

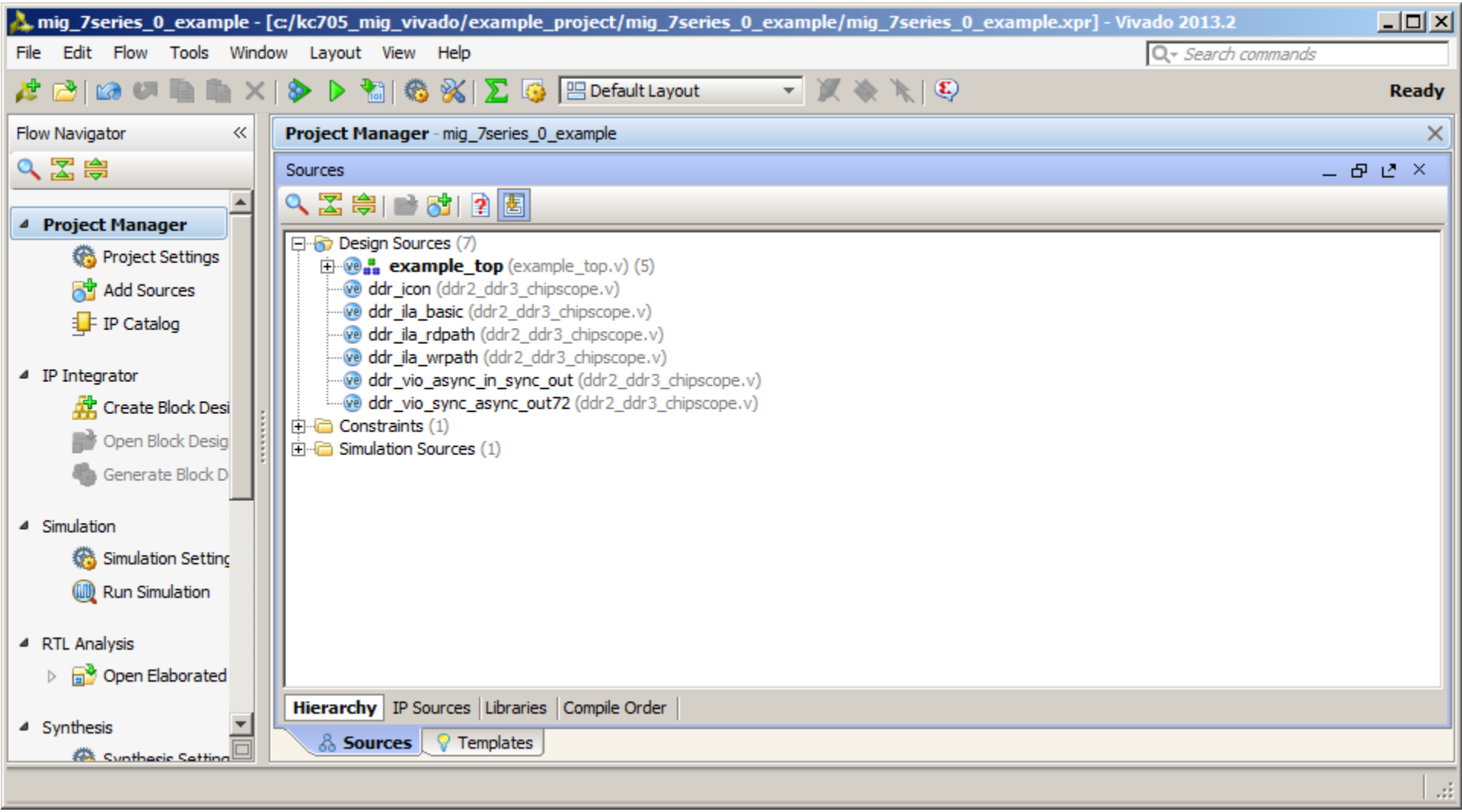
- Right click on mig_7series_0 and select Open IP Example Design…



Note: Presentation applies to the KC705

Compile Example Design

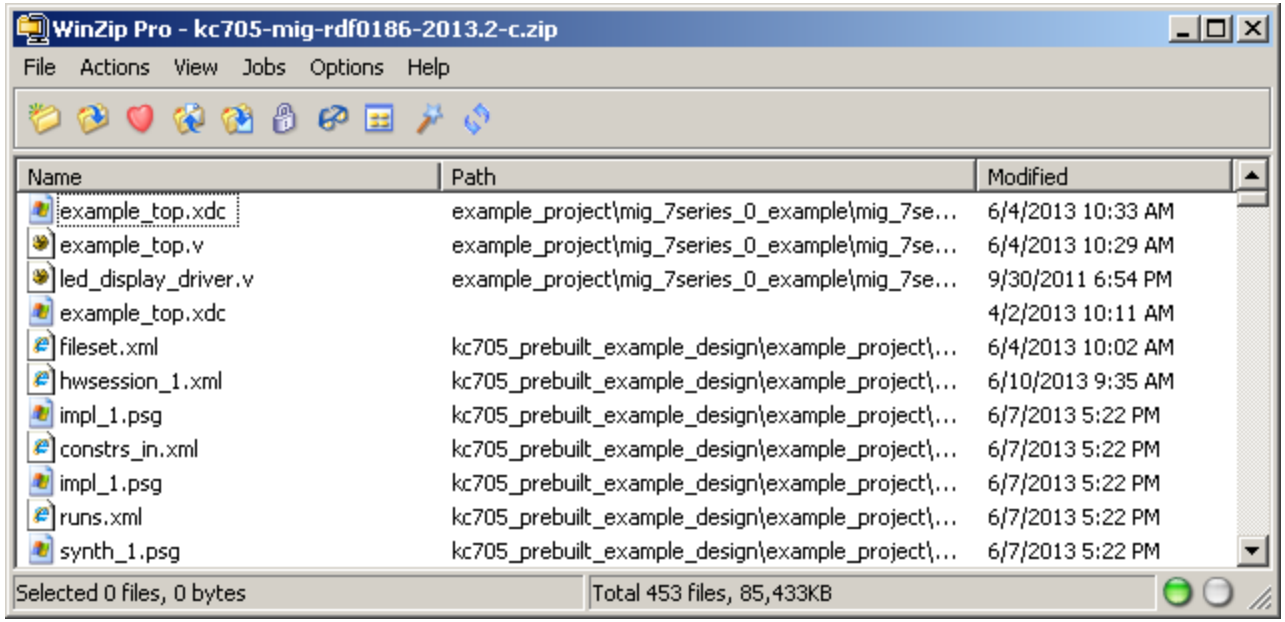
- A new project is created under <design path>/example_project



Note: The original project window can be closed

Modifications to Example Design

- **Unzip the KC705 MIG Vivado Design Files (2013.2 C) to your C:\kc705_mig_vivado directory**
  - Contains several changes needed to support Kintex-7 devices with MIG
  - Do this **after** creating the Example Design; changes only affect the Example Design



Note: Presentation applies to the KC705

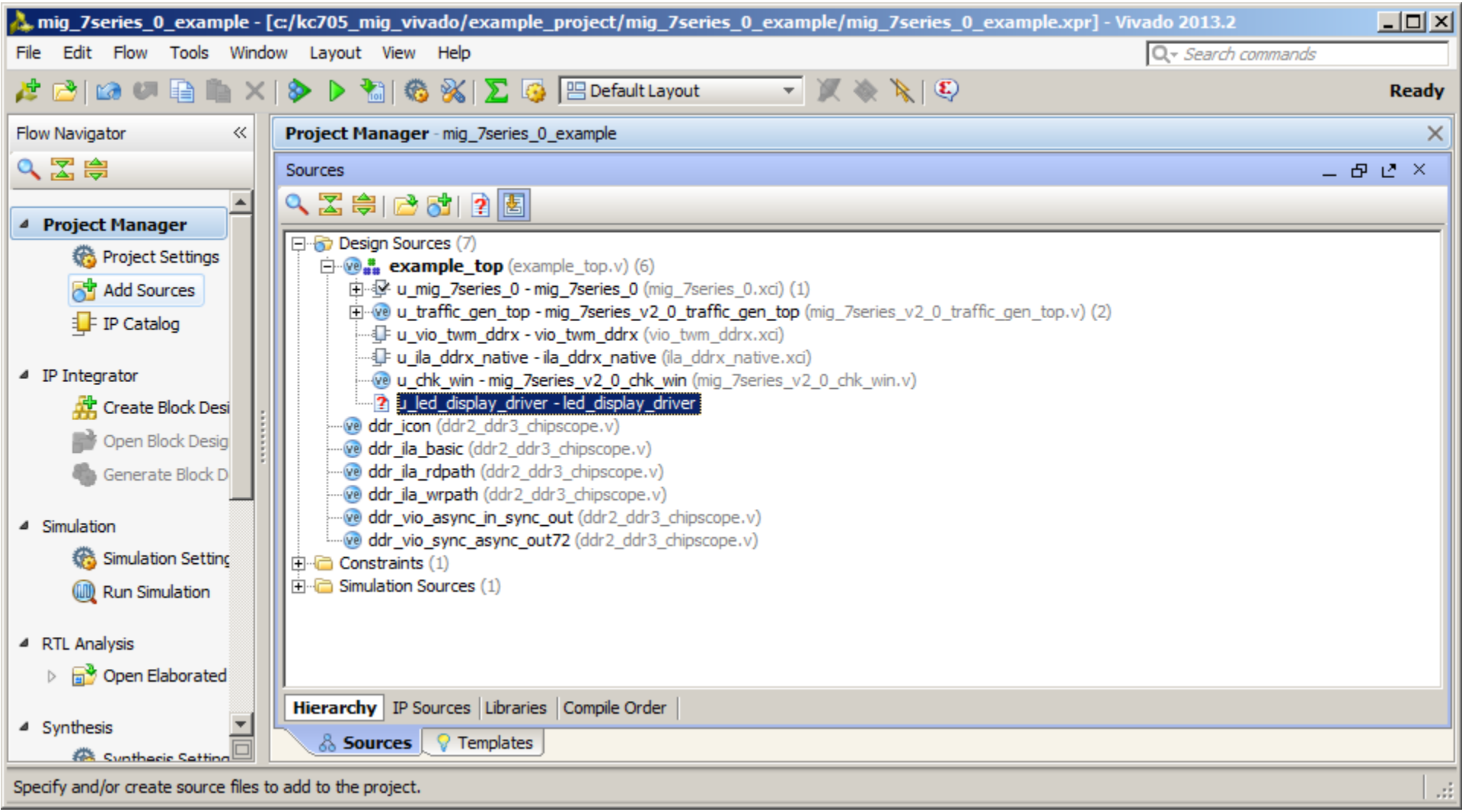
Modifications to Example Design

- **Modifications to the example design**
  - Added RTL and XDC modifications to drive LEDs
  - Added DCI Cascade constraints to XDC; for more information on using the DCI Cascade constraints for 7 Series refer to UG899

Note: Presentation applies to the KC705

Modifications to Example Design

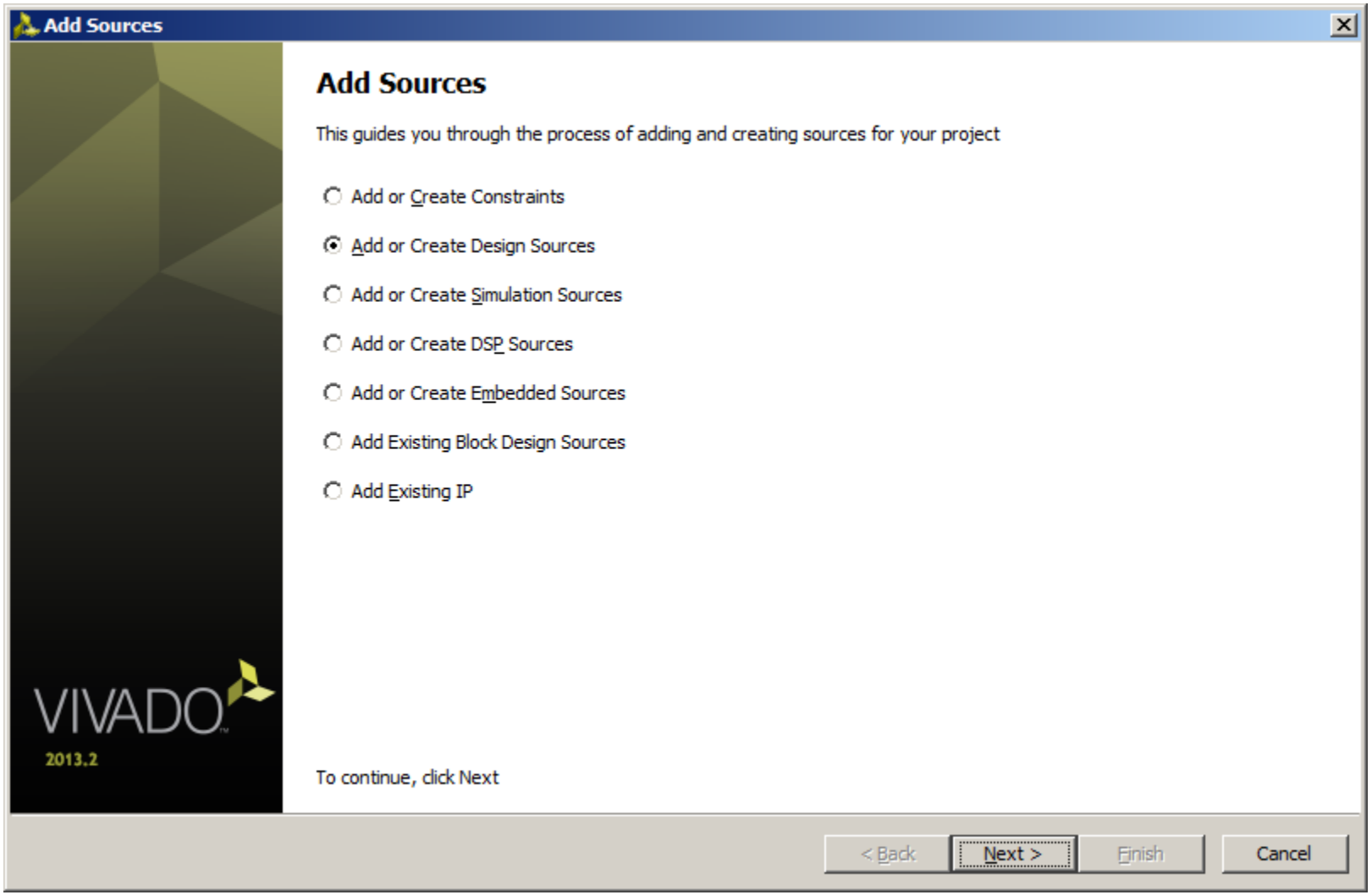
- The LED Display driver RTL file needs to be added manually
- Click on Add Sources



Note: Presentation applies to the KC705

Modifications to Example Design

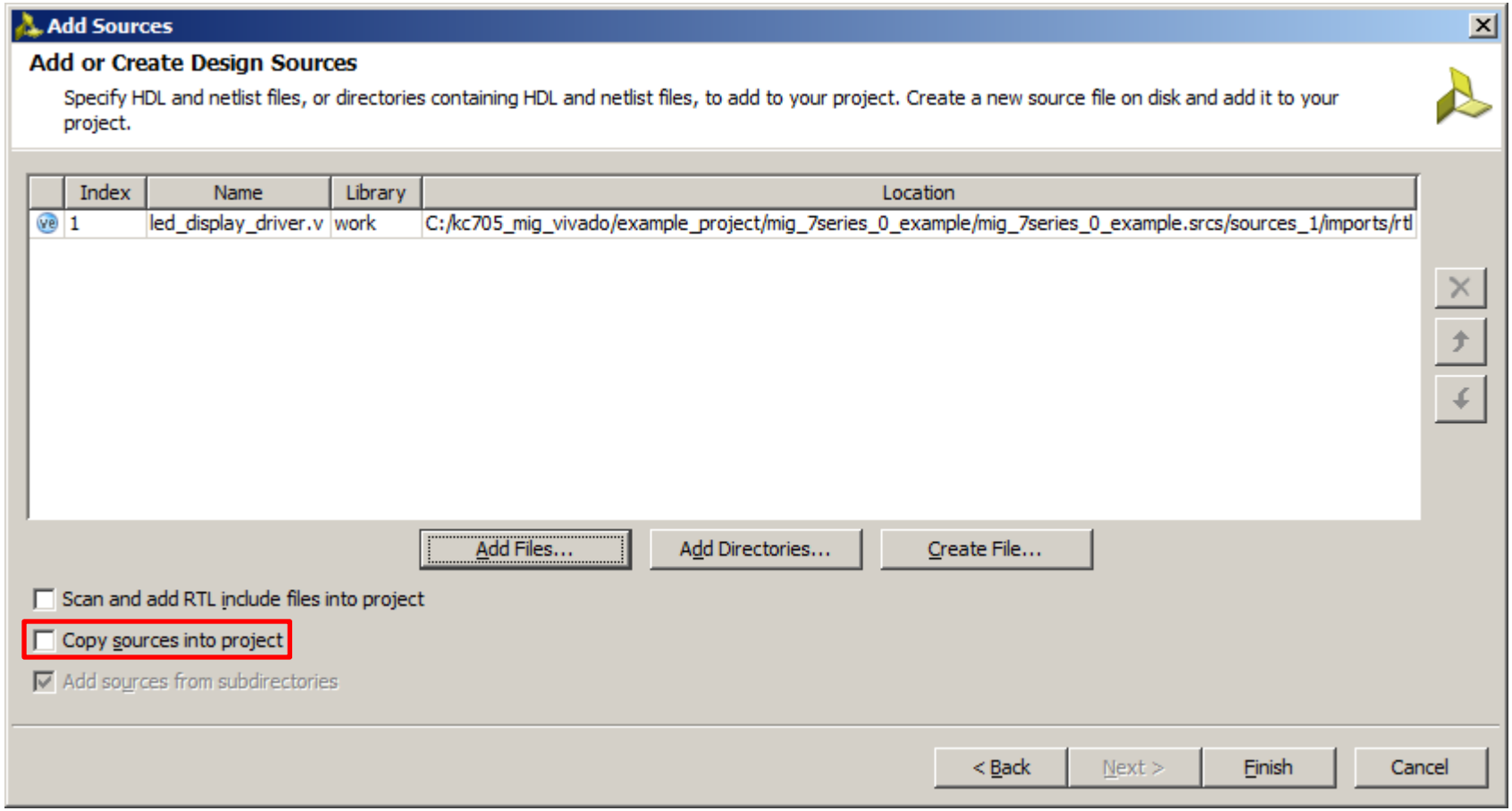
- Select Add or Create Design Sources and click Next



Note: Presentation applies to the KC705

Modifications to Example Design

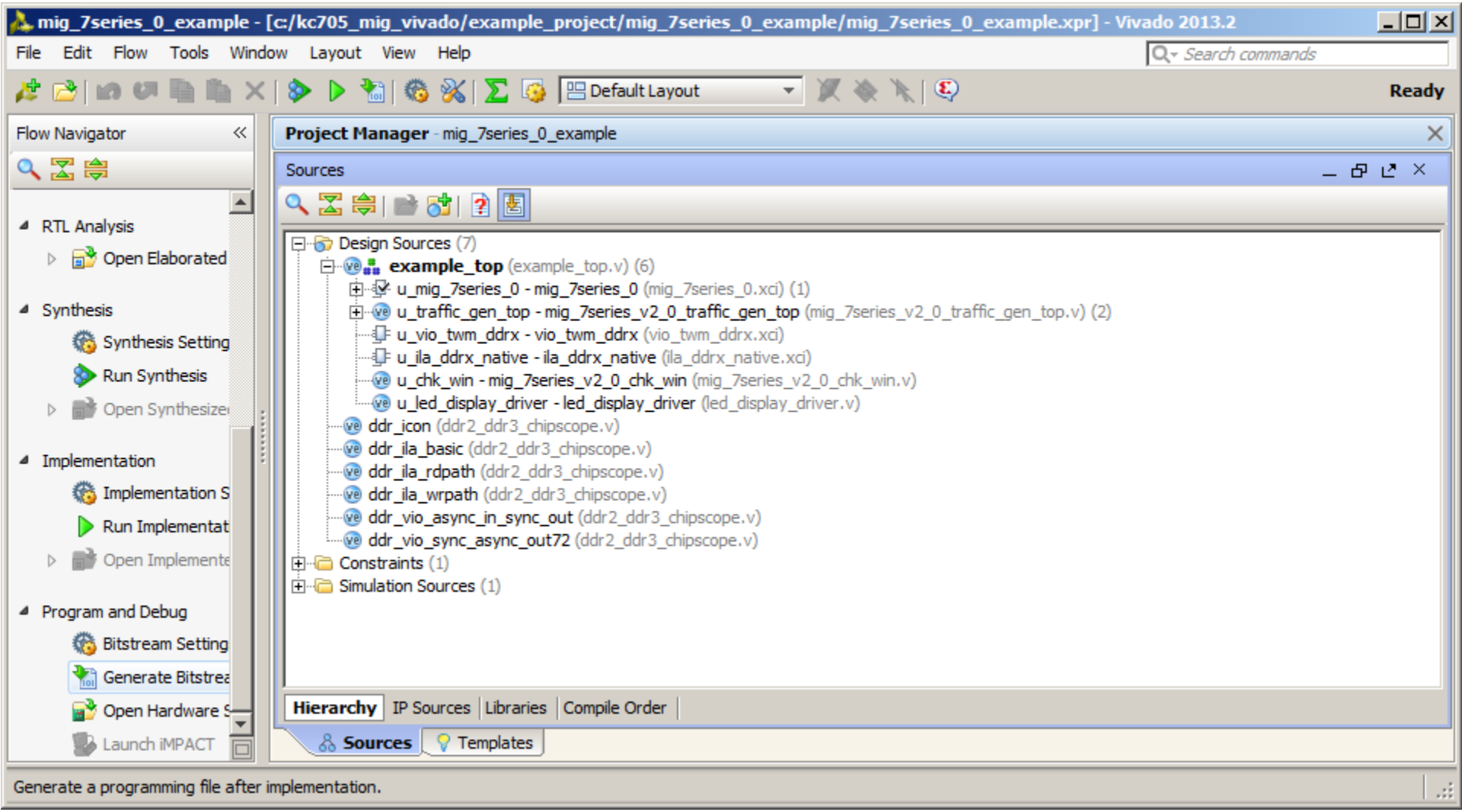
- Add led_display_driver.v from the example project
- Make sure Copy sources into project is deselected
- Click Finish



Note: Presentation applies to the KC705

Compile Example Design

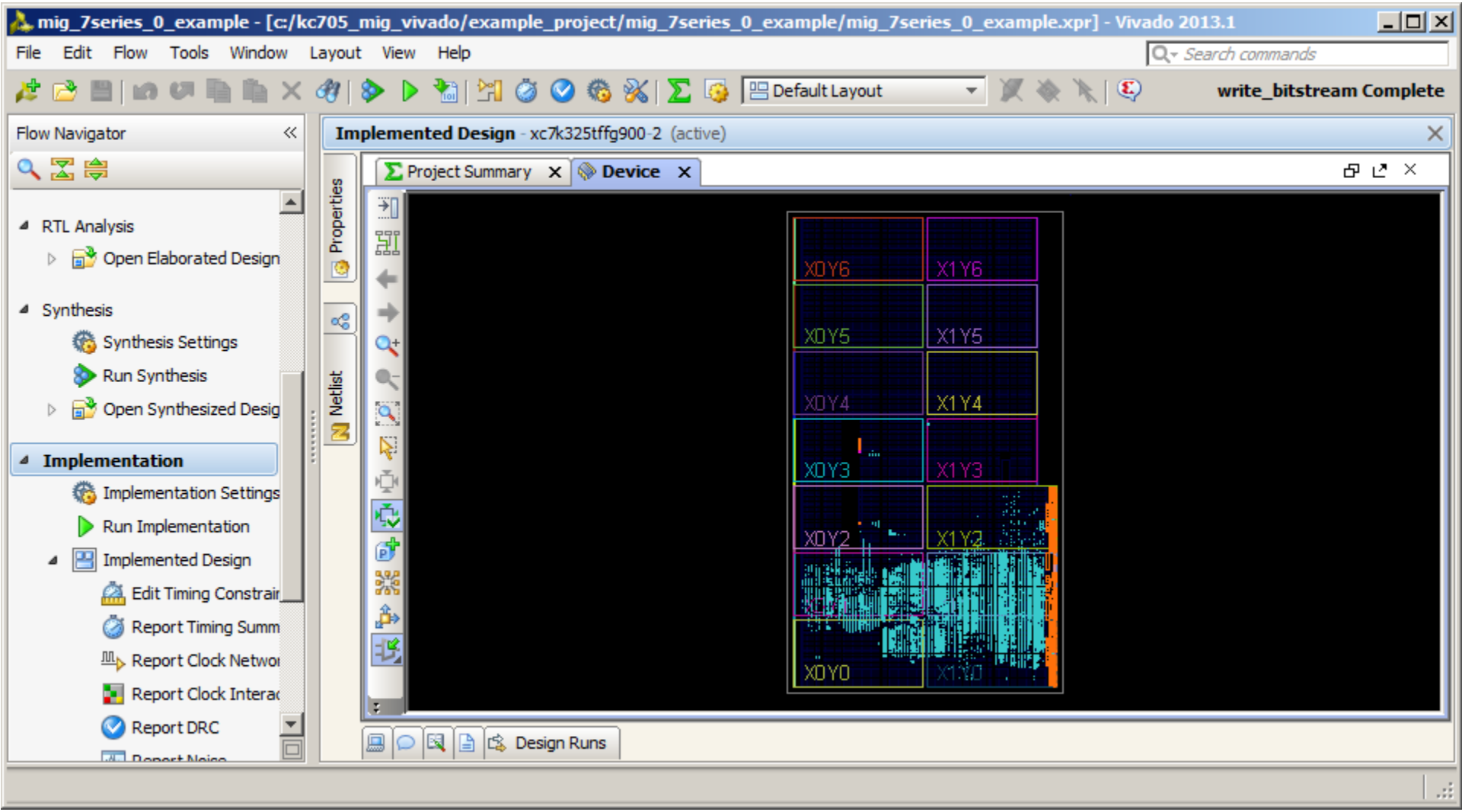
- Click on Generate Bitstream



Note: Presentation applies to the KC705

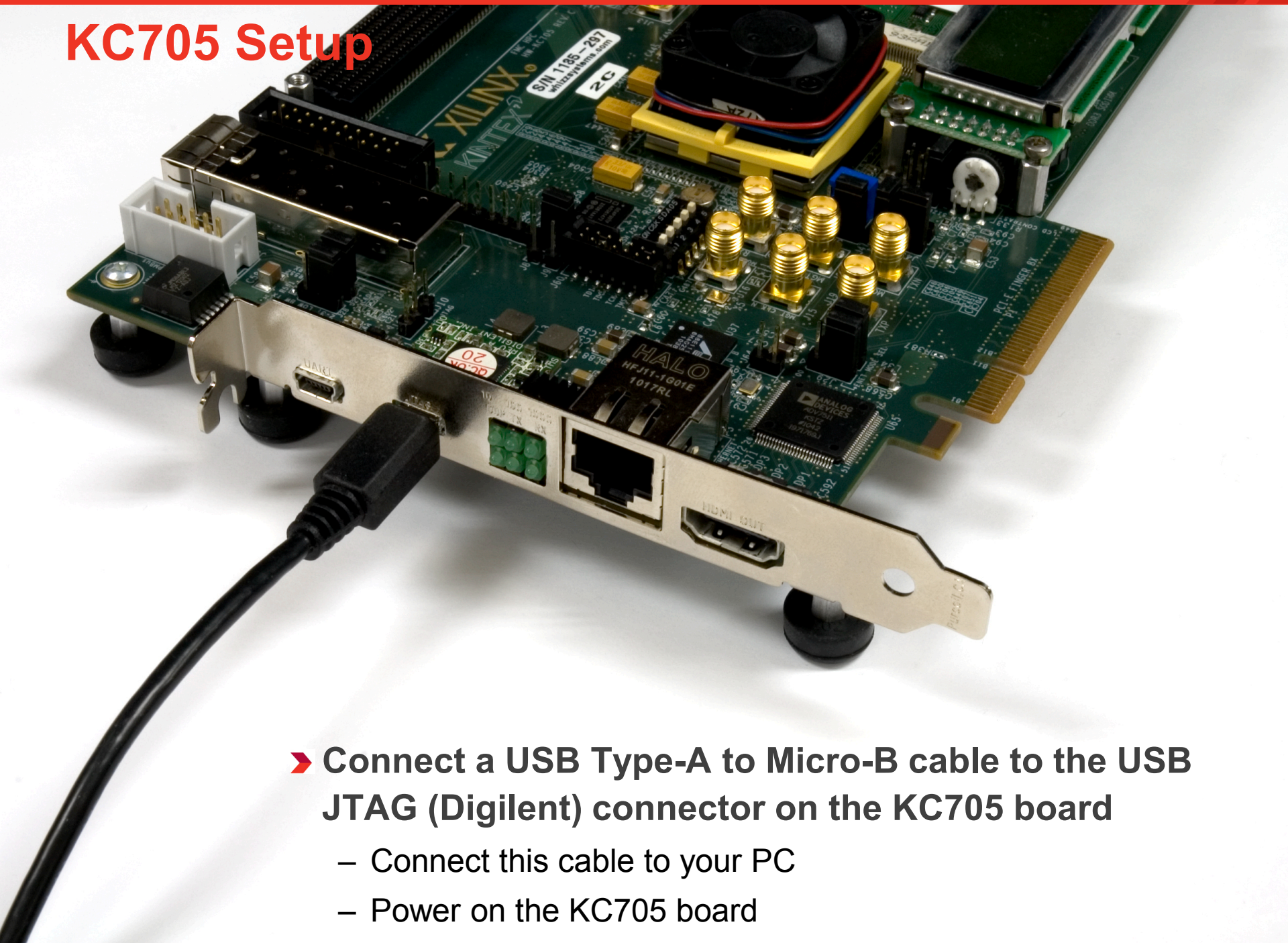
Compile Example Design

- Open and view the implemented design



Note: Presentation applies to the KC705

KC705 Setup



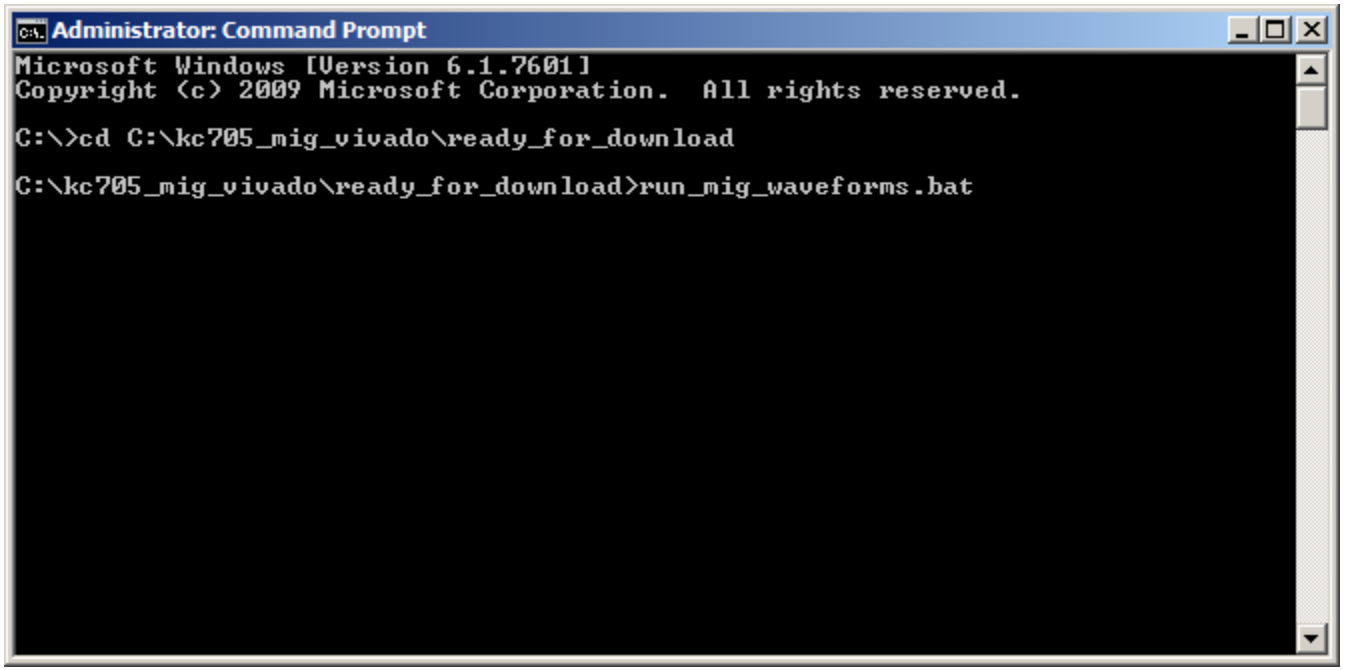
- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
  - Connect this cable to your PC
  - Power on the KC705 board

Run MIG Example Design

- From a Command Prompt, type:

  cd C:\kc705_mig_vivado\ready_for_download

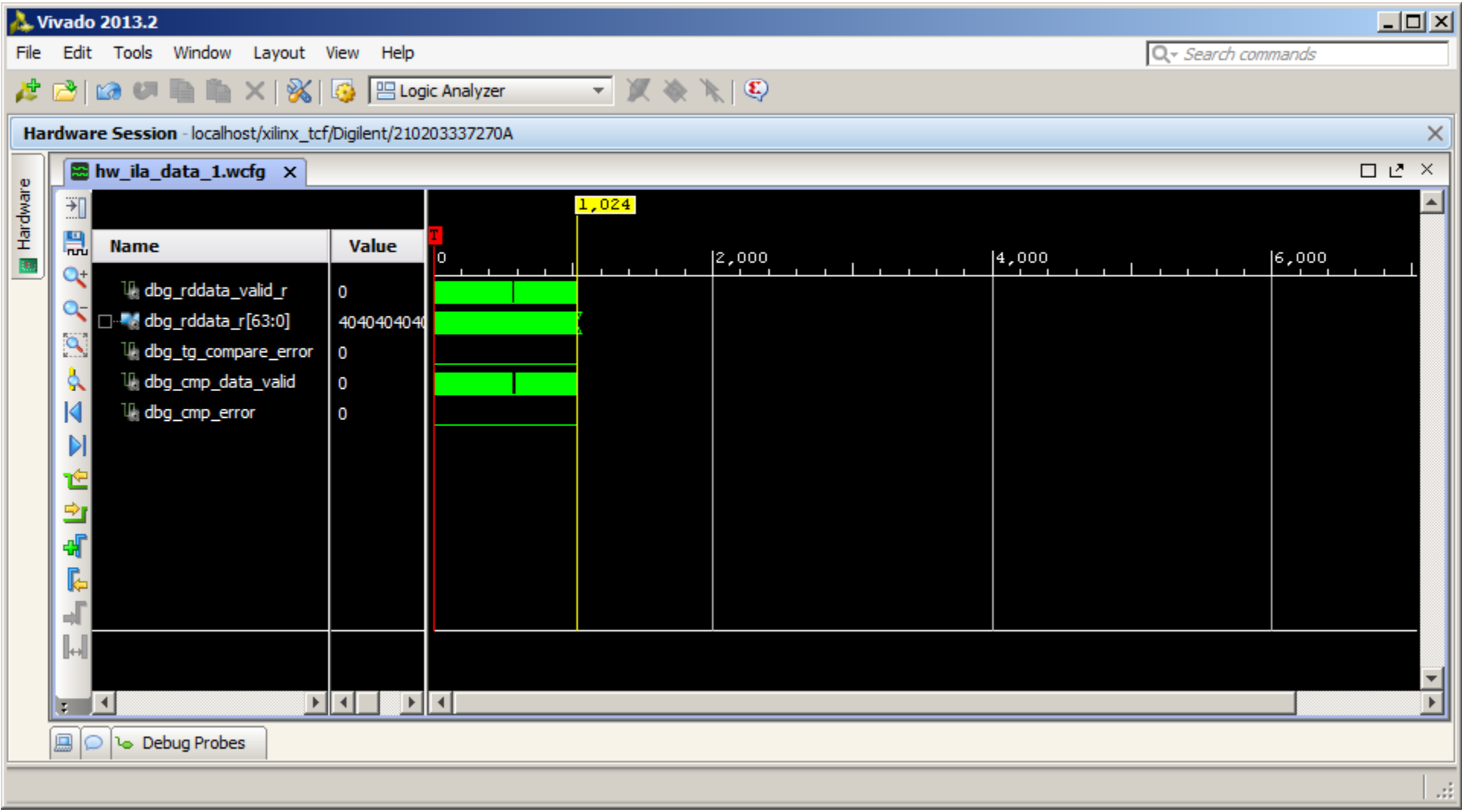
  run_mig_waveforms.bat



Note: Presentation applies to the KC705

Run MIG Example Design

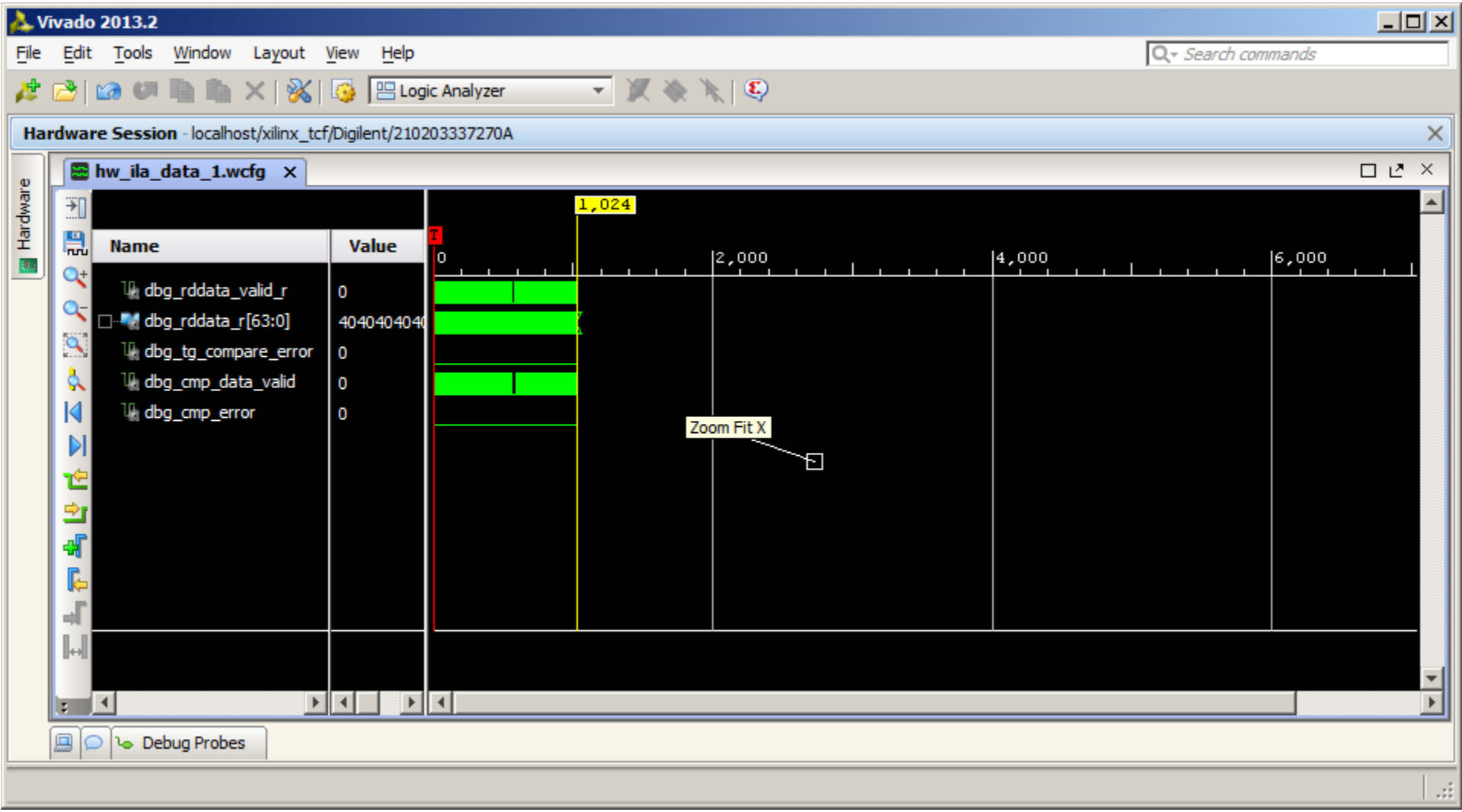
- Under Tcl script control, Vivado opens, loads the bitstream and generates a MIG waveform



Note: Set layout to Logic Analyzer layout to see waveform

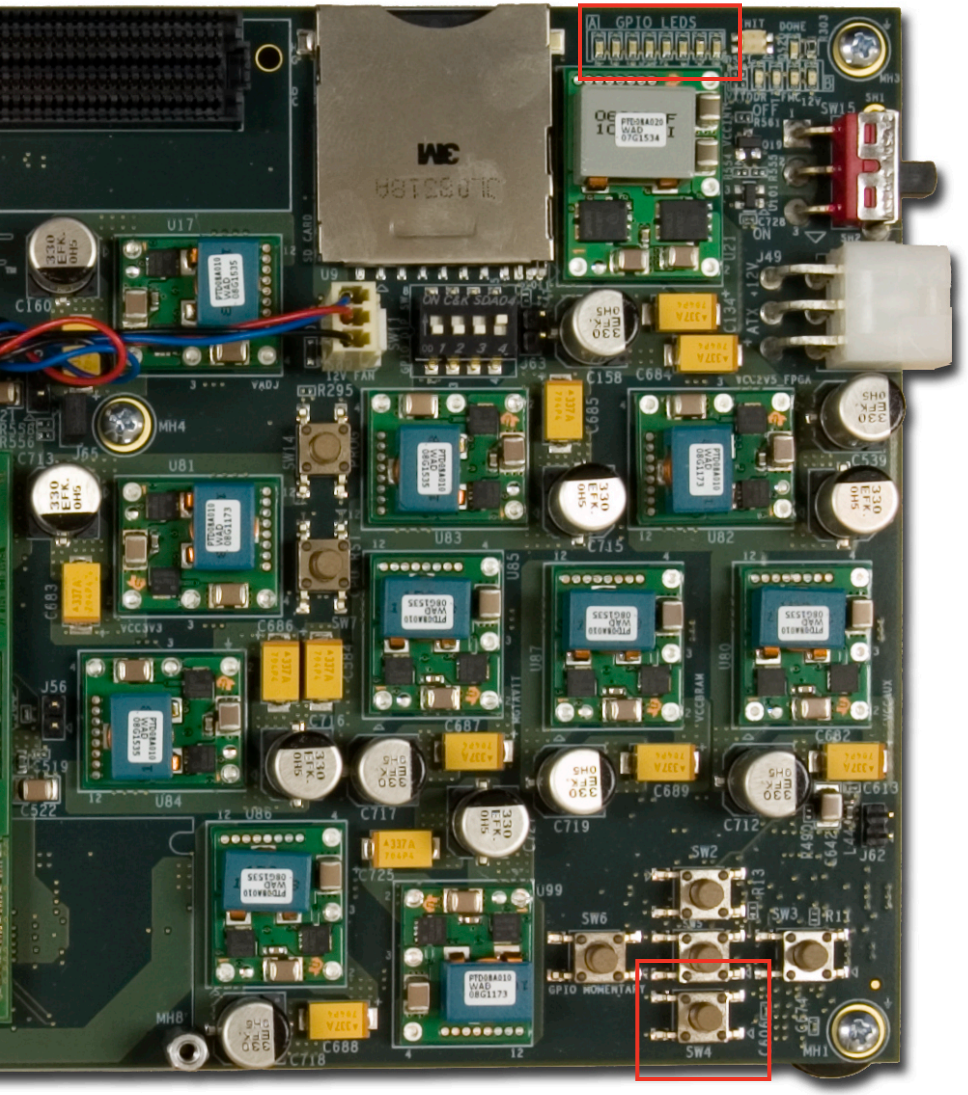
Run MIG Example Design

- Click and drag to the left to expand the waveform



Note: Presentation applies to the KC705

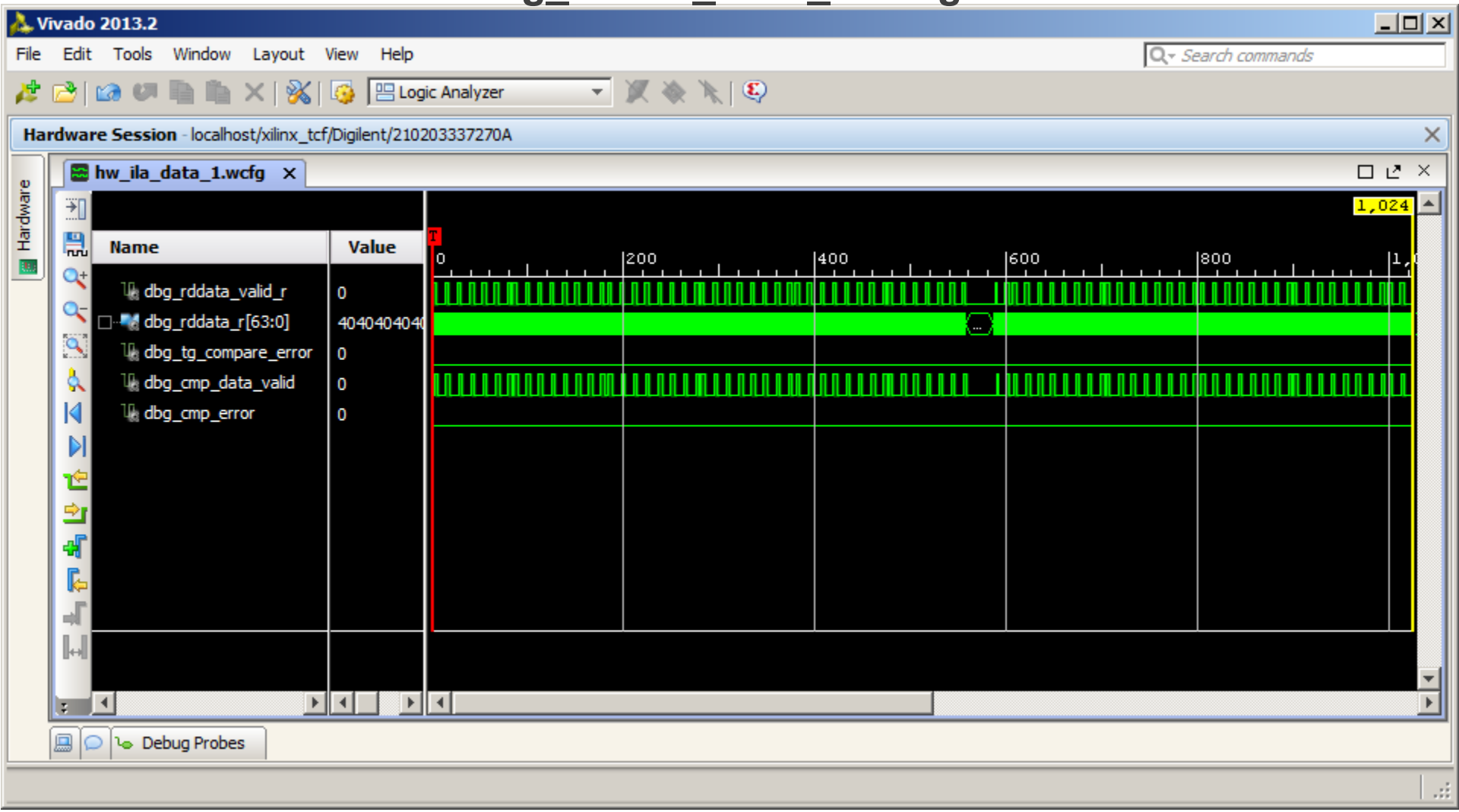
Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “South” button, SW4, is the reset

Run MIG Example Design

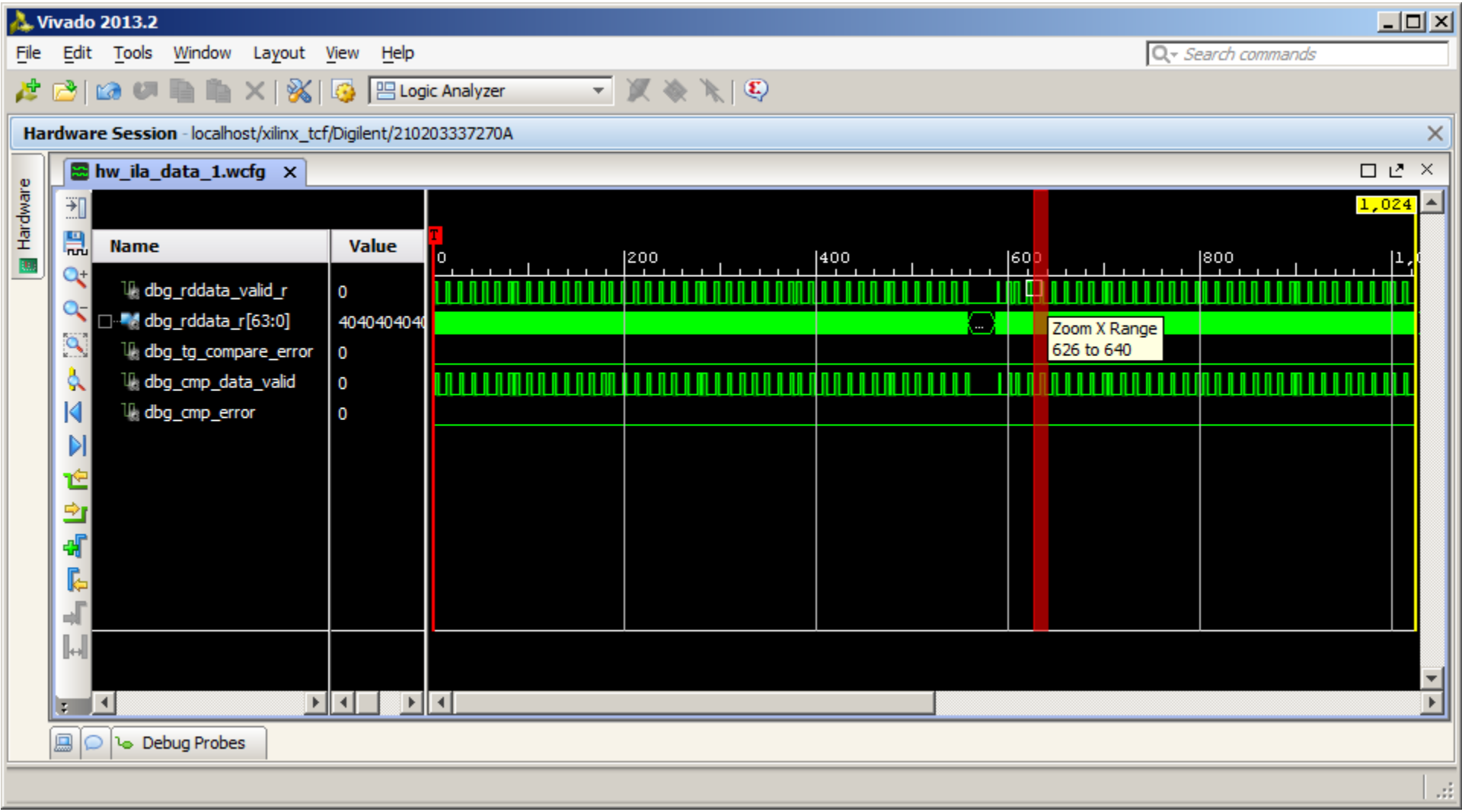
- View waveforms
- Data is valid when dbg_rddata_valid_r is high



Note: Presentation applies to the KC705

Run MIG Example Design

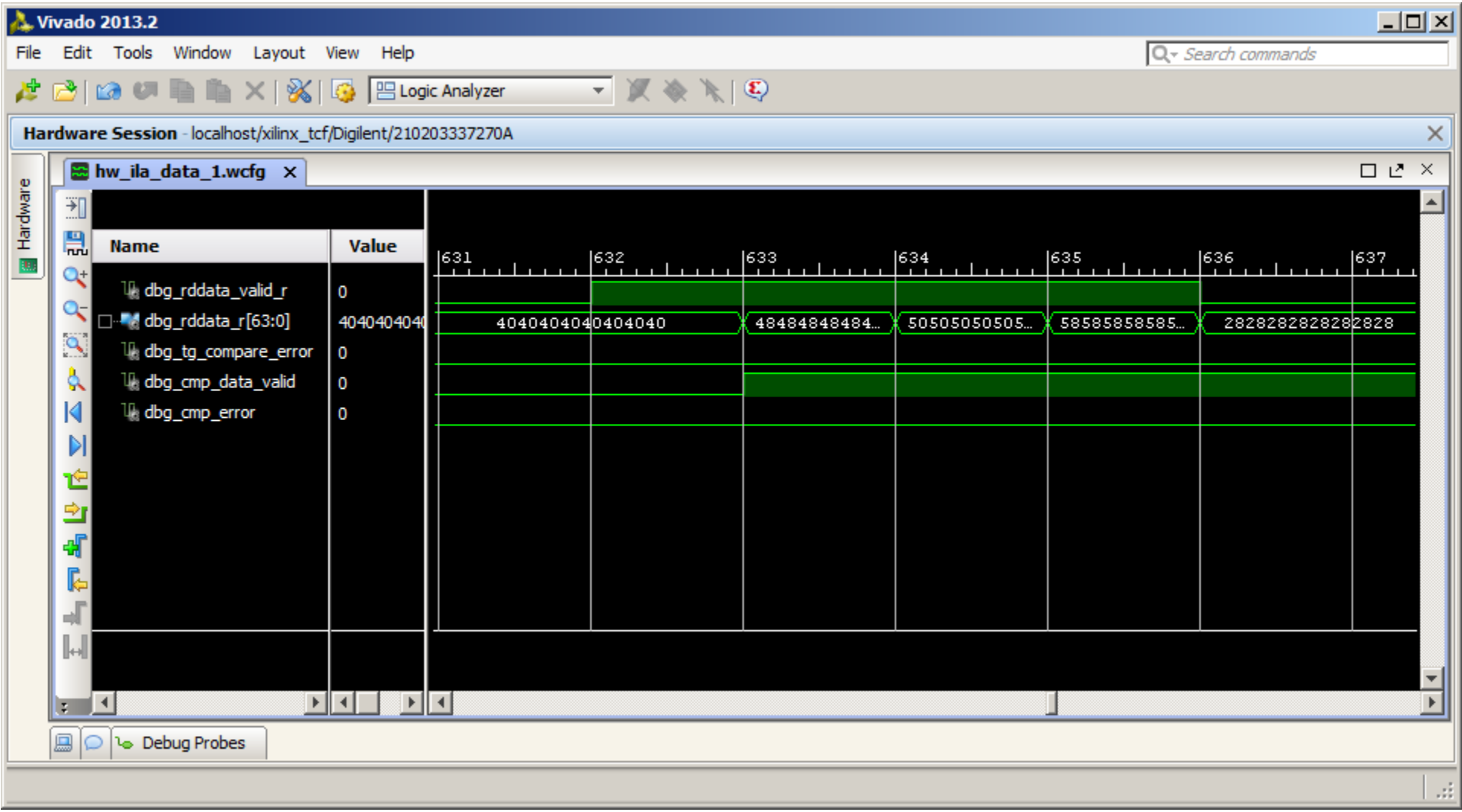
- Click and drag to the right to zoom in



Note: Presentation applies to the KC705

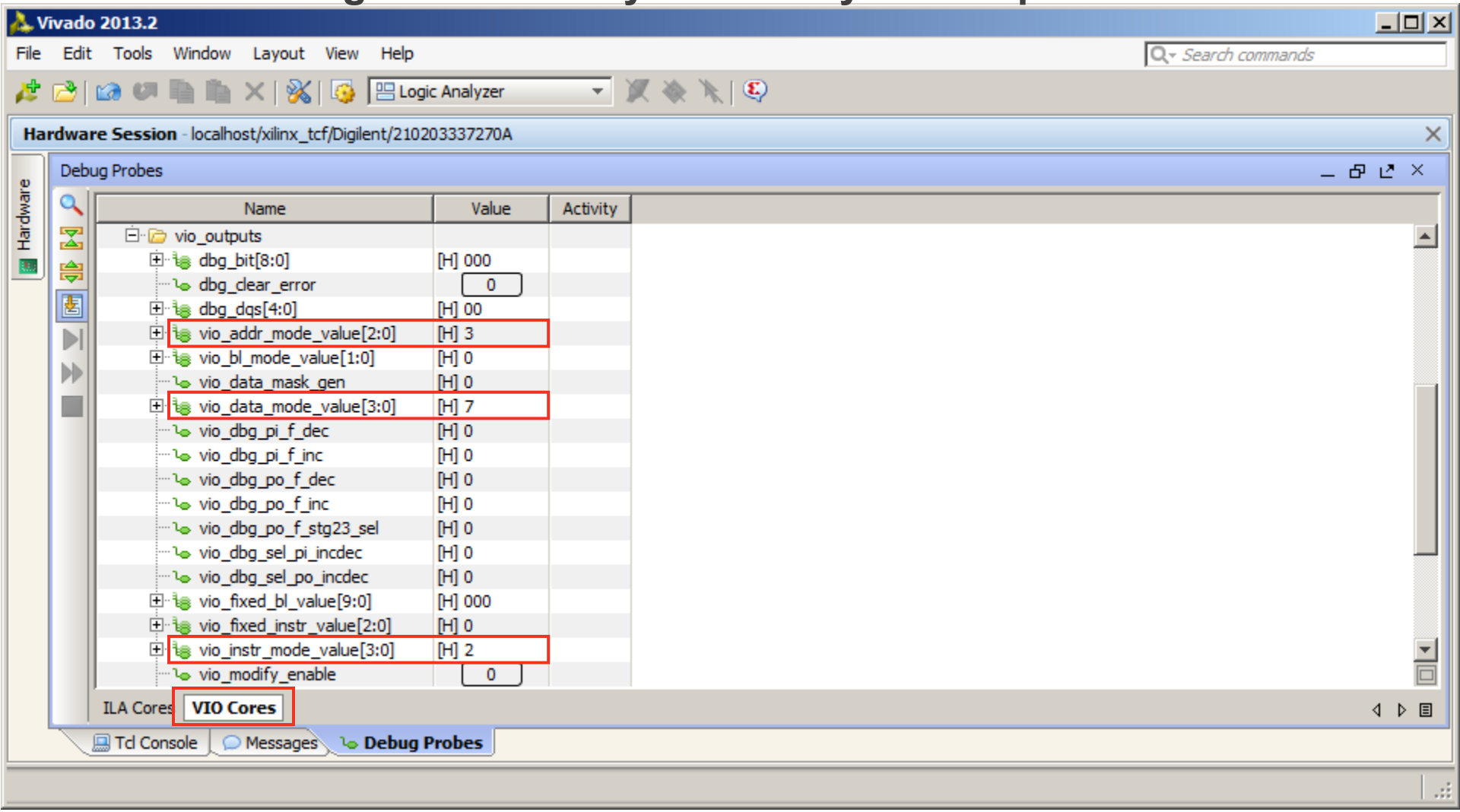
Run MIG Example Design

- View waveform details



Adjust Data Pattern using VIO Console

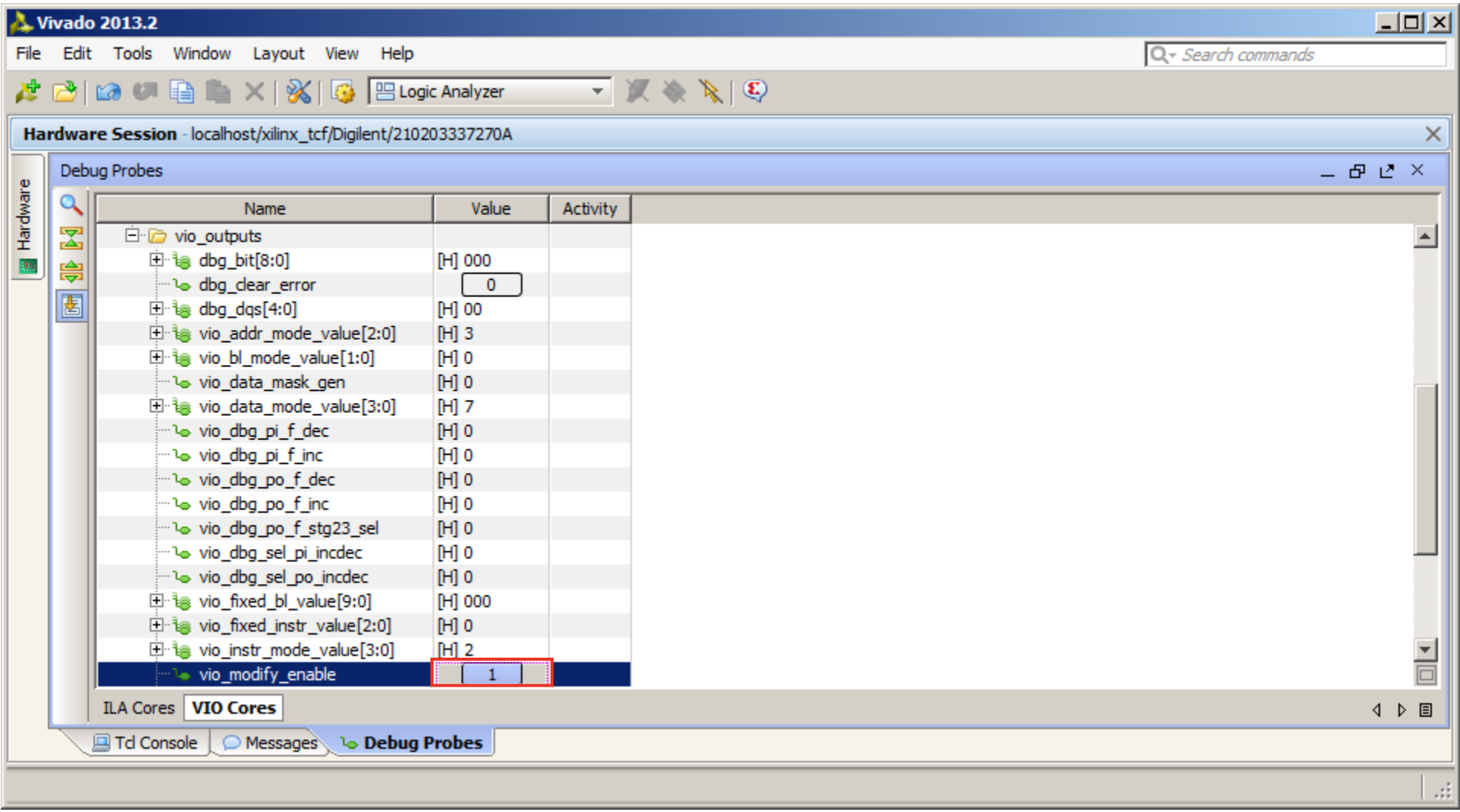
- Under the Debug Probes, view the vio_outputs of the VIO Cores
- PRBS settings were already entered by the script but not activated



Note: Presentation applies to the KC705

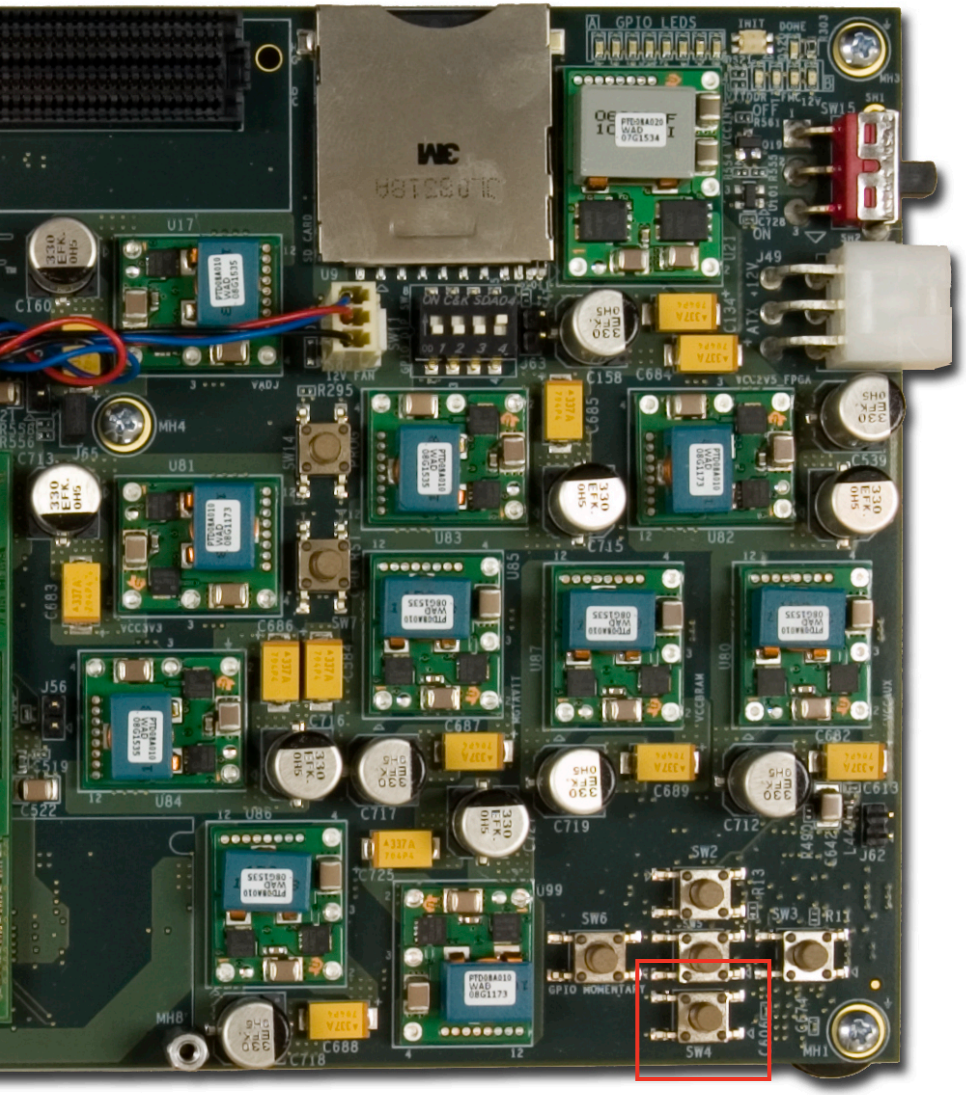
Adjust Data Pattern using VIO Console

- Toggle the vio_modify_enable button to “1”



Note: Presentation applies to the KC705

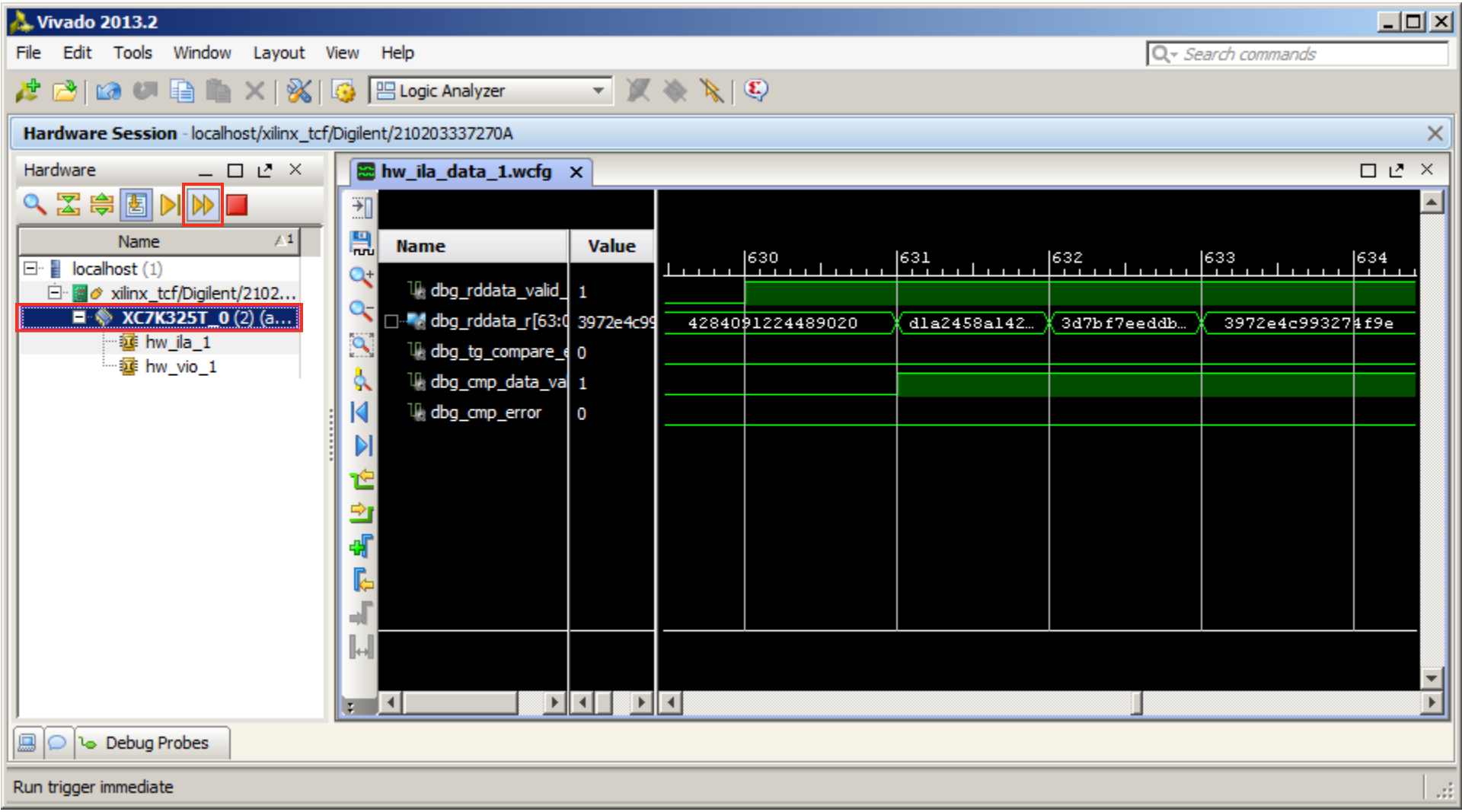
Run MIG Example Design



- Press and release the CPU RESET switch, SW4, after each change to vio_modify_enable or vio_data_mode_value

Adjust Data Pattern using VIO Console

- Select the XC7K325T_0 device and click Run Trigger Immediately
- View PRBS data



Note: Presentation applies to the KC705

References

References

- **Kintex-7 Memory**
  - 7 Series FPGAs Memory Interface Solutions User Guide – UG586
    - http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v2_0/ug586_7Series_MIS.pdf
- **Vivado Programming and Debugging**
  - Vivado Design Suite Programming and Debugging User Guide
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_2/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

- **Kintex-7**
  - Kintex-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm
- **KC705 Documentation**
  - Kintex-7 FPGA KC705 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm
  - KC705 Getting Started Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf
  - KC705 User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf