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KC705 MIG Design Creation with Vivado

July 2013

XTP196

Revision History

Date	Version	Description
07/30/13	5.1	Added missing files to RDF0186.
06/19/13	5.0	Recompiled for 2013.2
04/03/13	4.0	Recompiled for 2013.1. AR53420 fixed. Added AR55531.
02/22/13	3.1	Added AR53420.
12/18/12	3.0	Recompiled for 2012.4. Added AR53392.
10/23/12	2.0	Recompiled for 2012.3. Added AR52368.
07/25/12	1.0	Regenerated for 14.2. Added Vivado Flow. Added AR50886.

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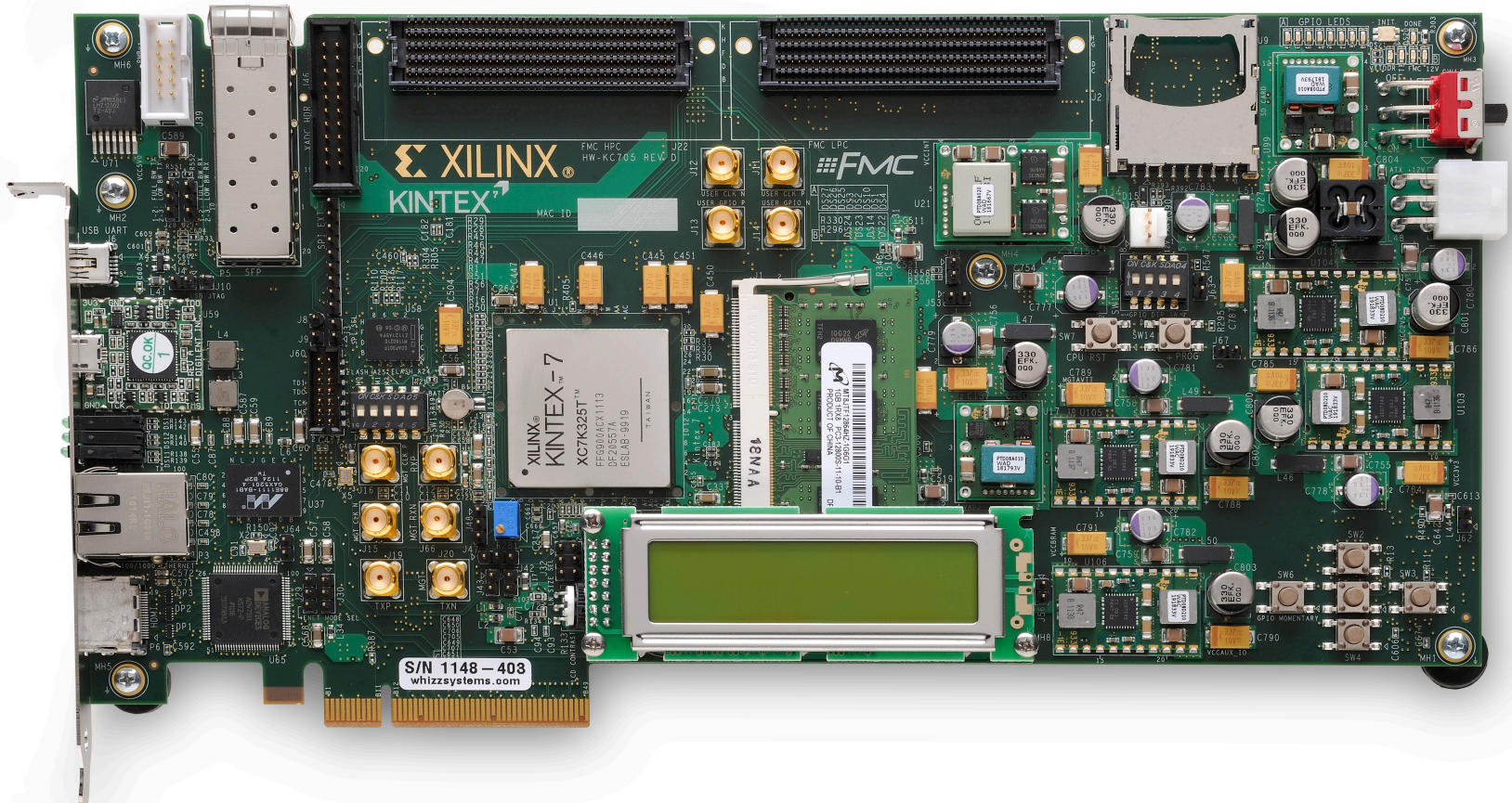
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Overview

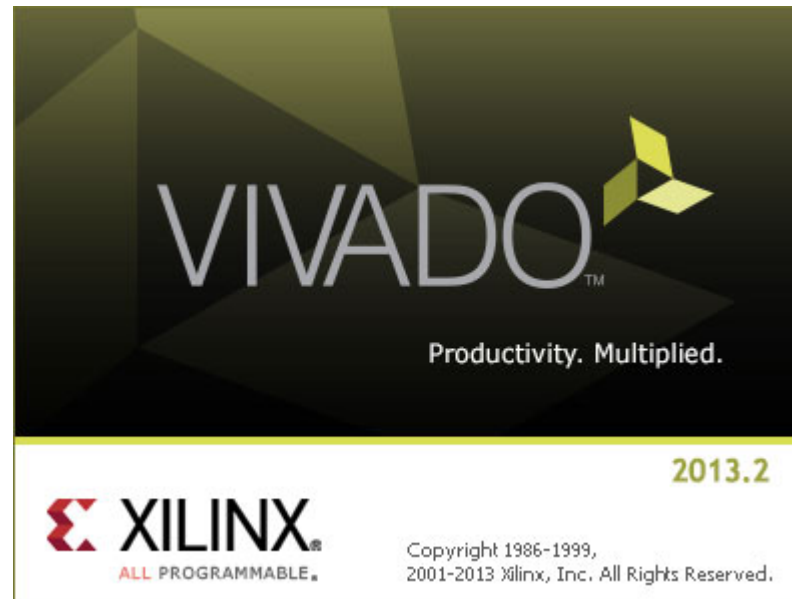
- **KC705 Board**
- **KC705 Setup**
- **Generate MIG Example Design**
- **Modifications to Example Design**
- **Compile Example Design**
- **Run MIG Example Design**
- **References**

Xilinx KC705 Board



Vivado Software Requirements

➤ Xilinx Vivado Design Suite 2013.2, Design Edition

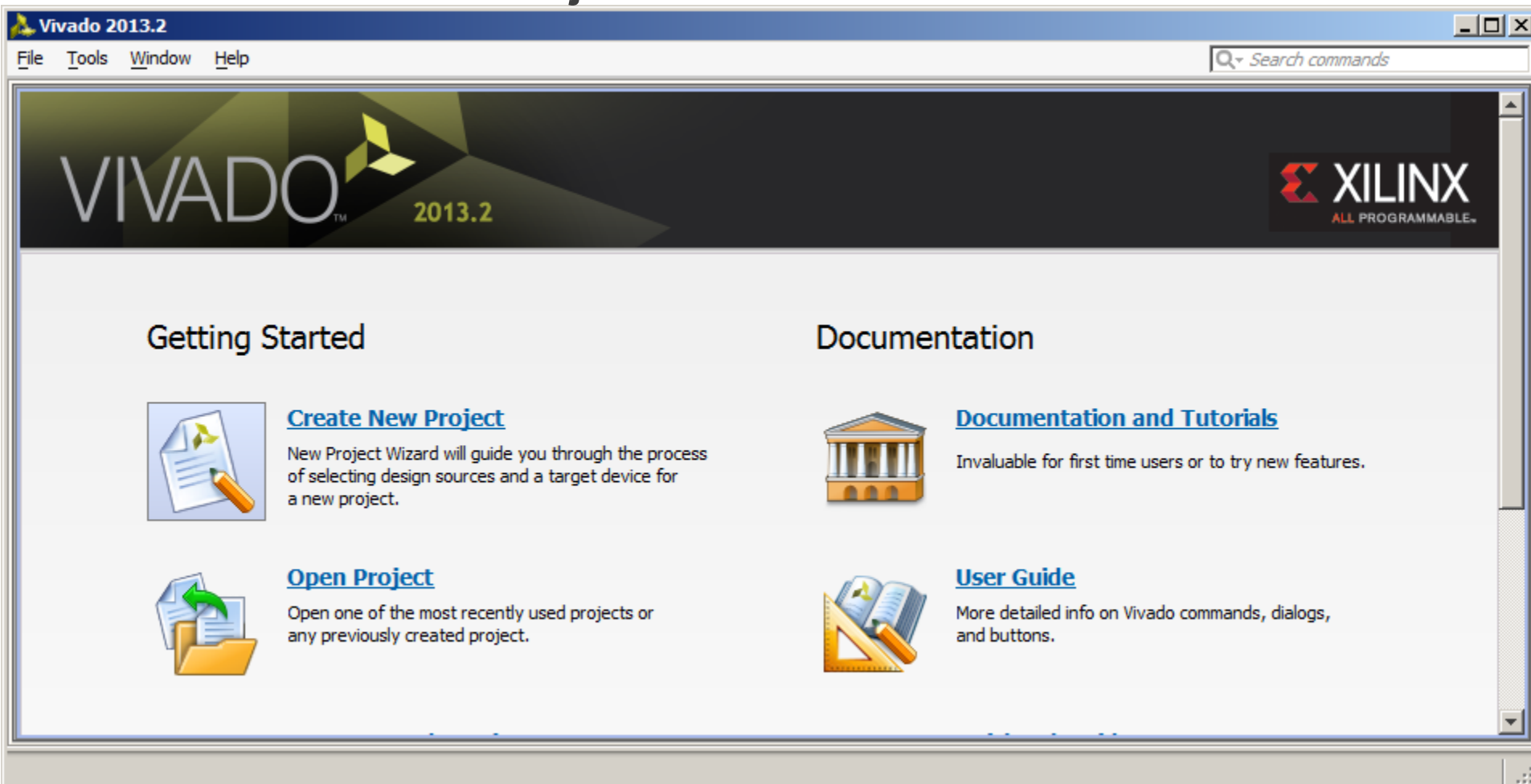


Generate MIG Example Design

➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2013.2 → Vivado

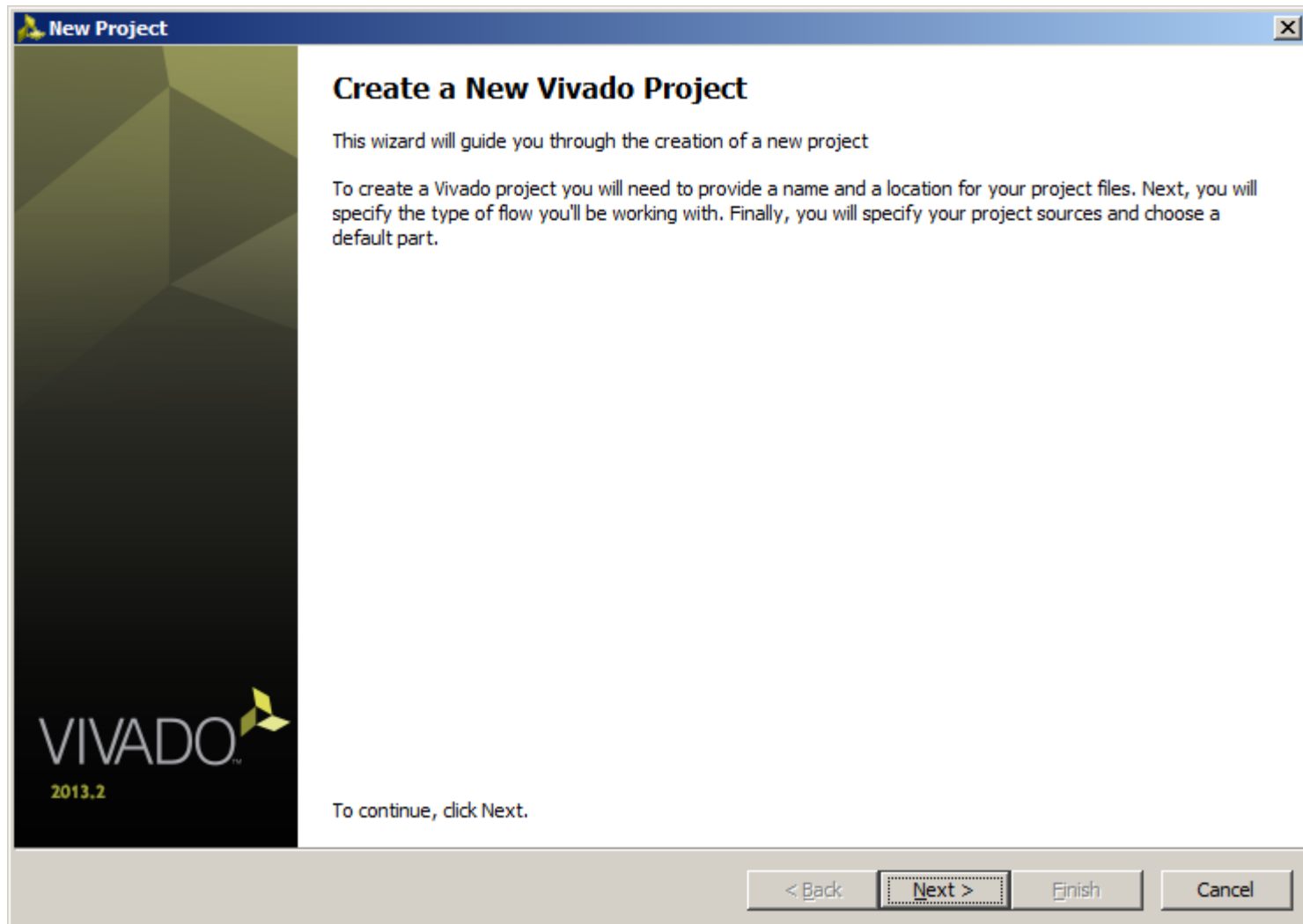
➤ Select Create New Project



Note: Presentation applies to the KC705

Generate MIG Example Design

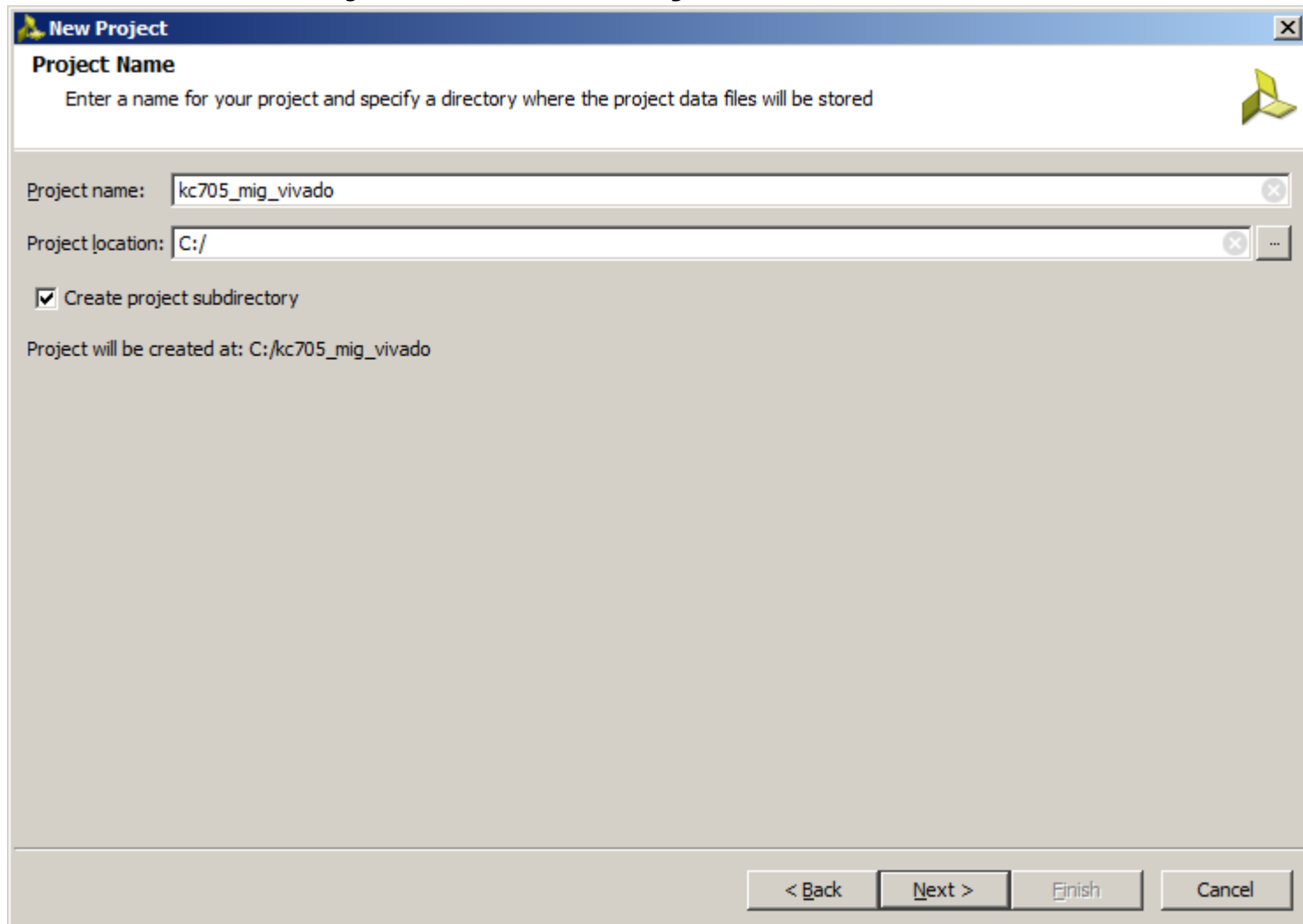
➤ Click Next



Note: Presentation applies to the KC705

Generate MIG Example Design

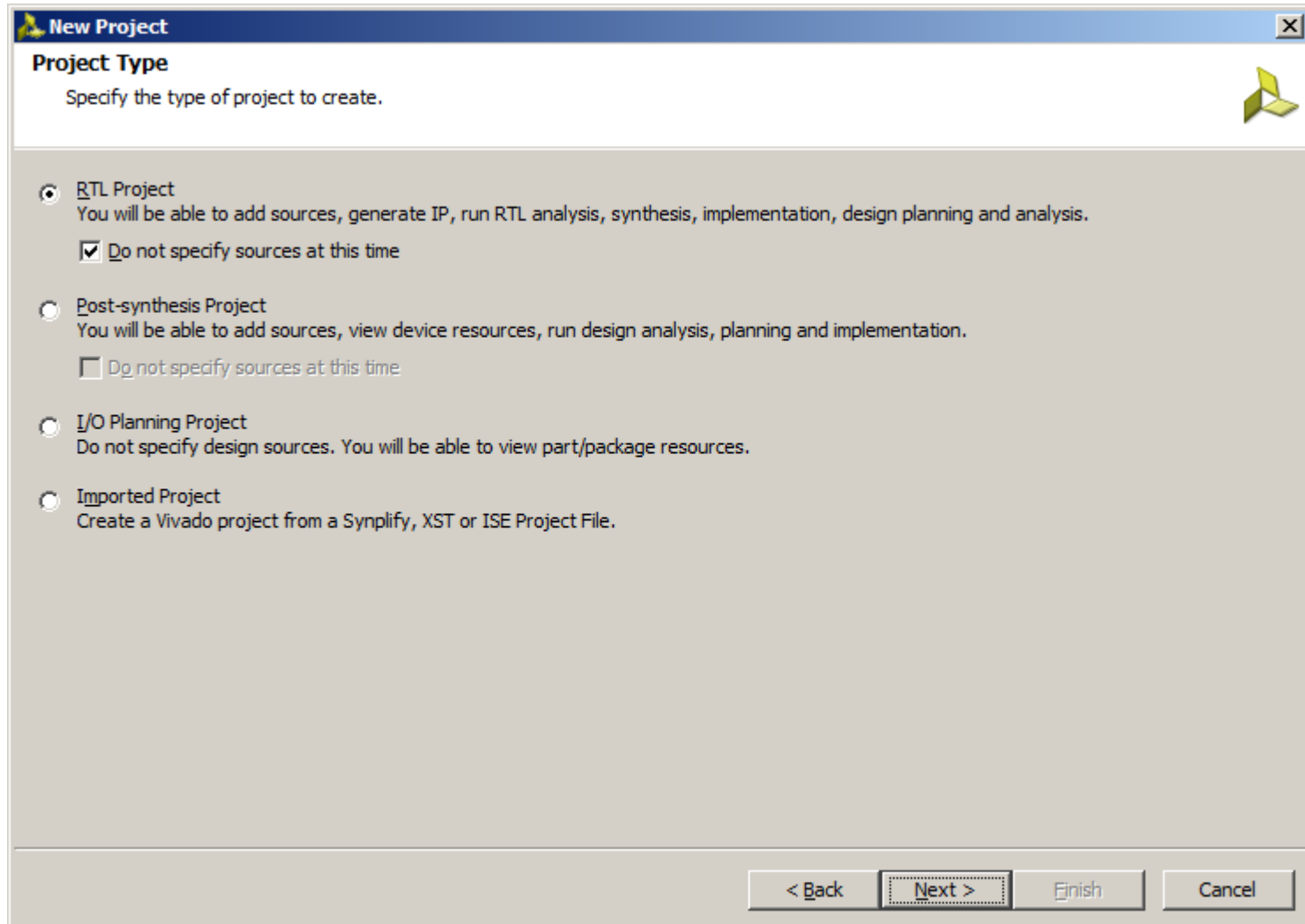
- Set the Project name and location to `kc705_mig_vivado` and `C:\`
 - Check **Create Project Subdirectory**



Generate MIG Example Design

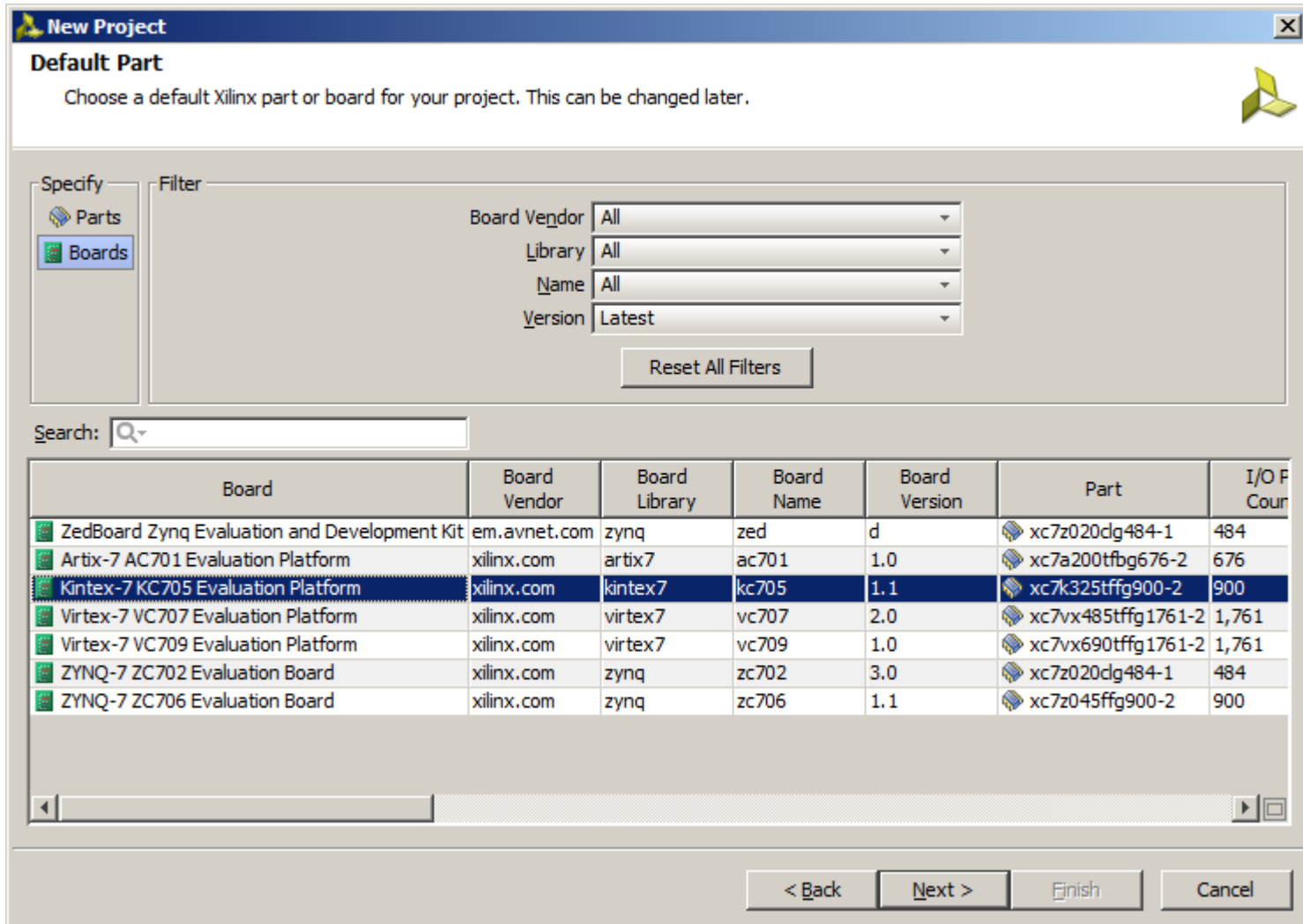
➤ Select RTL Project

- Select **Do not specify sources at this time**



Generate MIG Example Design

➤ Select the KC705 Board



New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Specify: **Boards**

Filter:

Board Vendor: All
Library: All
Name: All
Version: Latest

Reset All Filters

Search:

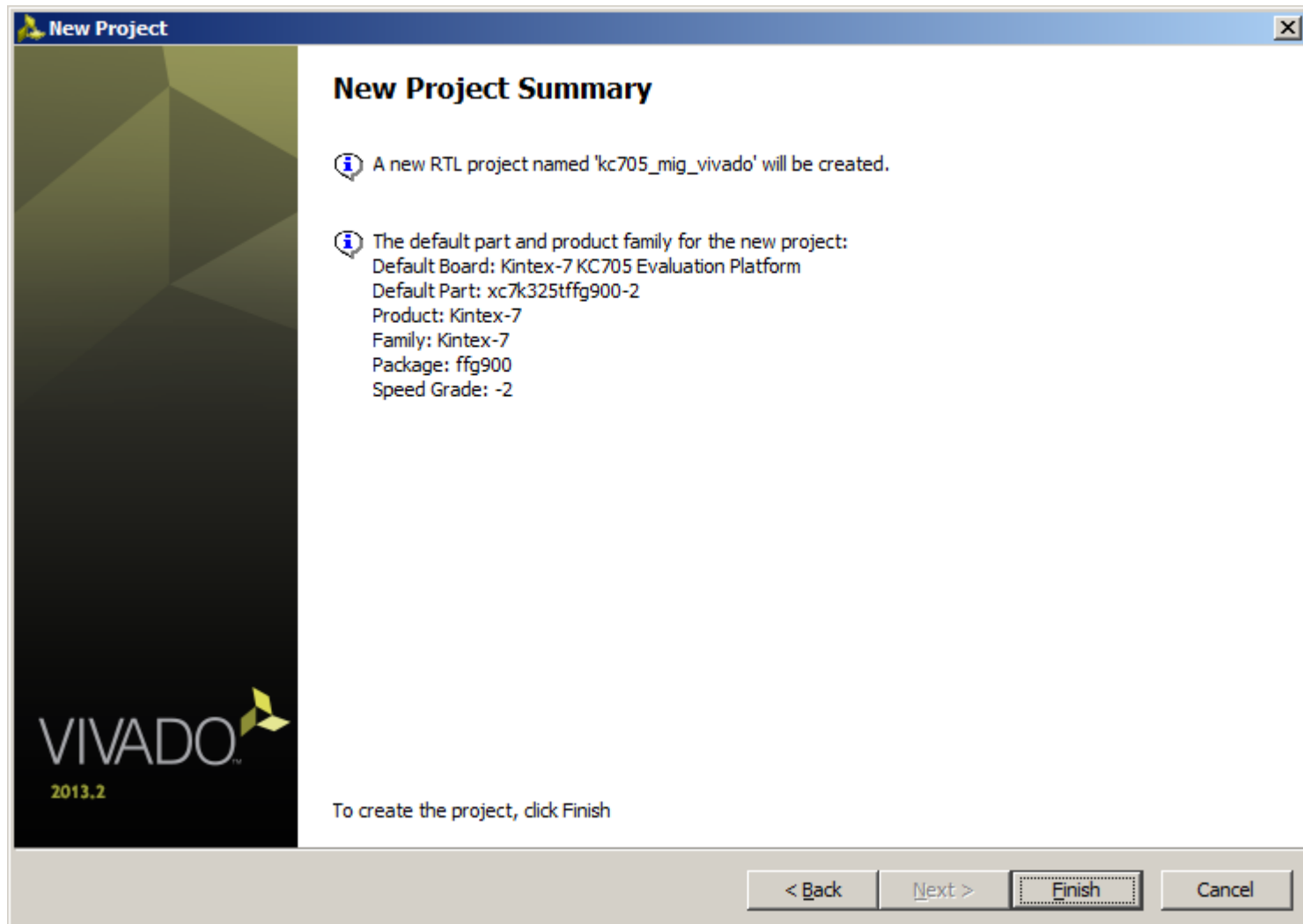
Board	Board Vendor	Board Library	Board Name	Board Version	Part	I/O P Cour
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	zynq	zed	d	xc7z020dkg484-1	484
Artix-7 AC701 Evaluation Platform	xilinx.com	artix7	ac701	1.0	xc7a200tffg676-2	676
Kintex-7 KC705 Evaluation Platform	xilinx.com	kintex7	kc705	1.1	xc7k325tffg900-2	900
Virtex-7 VC707 Evaluation Platform	xilinx.com	virtex7	vc707	2.0	xc7vx485tffg1761-2	1,761
Virtex-7 VC709 Evaluation Platform	xilinx.com	virtex7	vc709	1.0	xc7vx690tffg1761-2	1,761
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	zynq	zc702	3.0	xc7z020dkg484-1	484
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	zynq	zc706	1.1	xc7z045ffg900-2	900

< Back Next > Finish Cancel

Note: Presentation applies to the KC705

Generate MIG Example Design

➤ Click Finish



Note: Presentation applies to the KC705

Generate MIG Example Design

➤ Click on IP Catalog

The screenshot shows the Vivado 2013.2 IDE interface. The main window is titled "kc705_mig_vivado - [C:/kc705_mig_vivado/kc705_mig_vivado.xpr] - Vivado 2013.2". The "Project Manager" window is open, showing the "Sources" tab with a tree view containing "Design Sources", "Constraints (1)", and "Simulation Sources (1)". The "IP Catalog" icon is highlighted with a red box. The "Project Summary" window is also open, showing "Project Settings" and "Synthesis" sections. The "Design Runs" window is open at the bottom, showing a table of design runs.

Name	Part	Constraints	Strategy	Status
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2013)	Not started
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2013)	Not started

Note: Presentation applies to the KC705

Generate MIG Example Design

➤ Select MIG 7 Series, 2.0 under Memory Interface Generators

The screenshot shows the Vivado 2013.2 IP Catalog window. The 'Project Manager' tab is active, displaying a list of IP blocks. The 'Memory Interface Generators' folder is expanded, and the 'MIG 7 Series' block is selected. The 'Details' pane shows the following information:

Name	Version	AXI4	Status	License
Digital Signal Processing				
Embedded Processing				
FPGA Features and Design				
Math Functions				
Memories & Storage Elements				
ECC	2.0		Production	Included
FIFOs				
Memory Interface Generators				
MIG 7 Series	2.0	AXI4	Production	Included
RAMs & ROMs				
Standard Bus Interfaces				
Video & Image Processing				

Details:

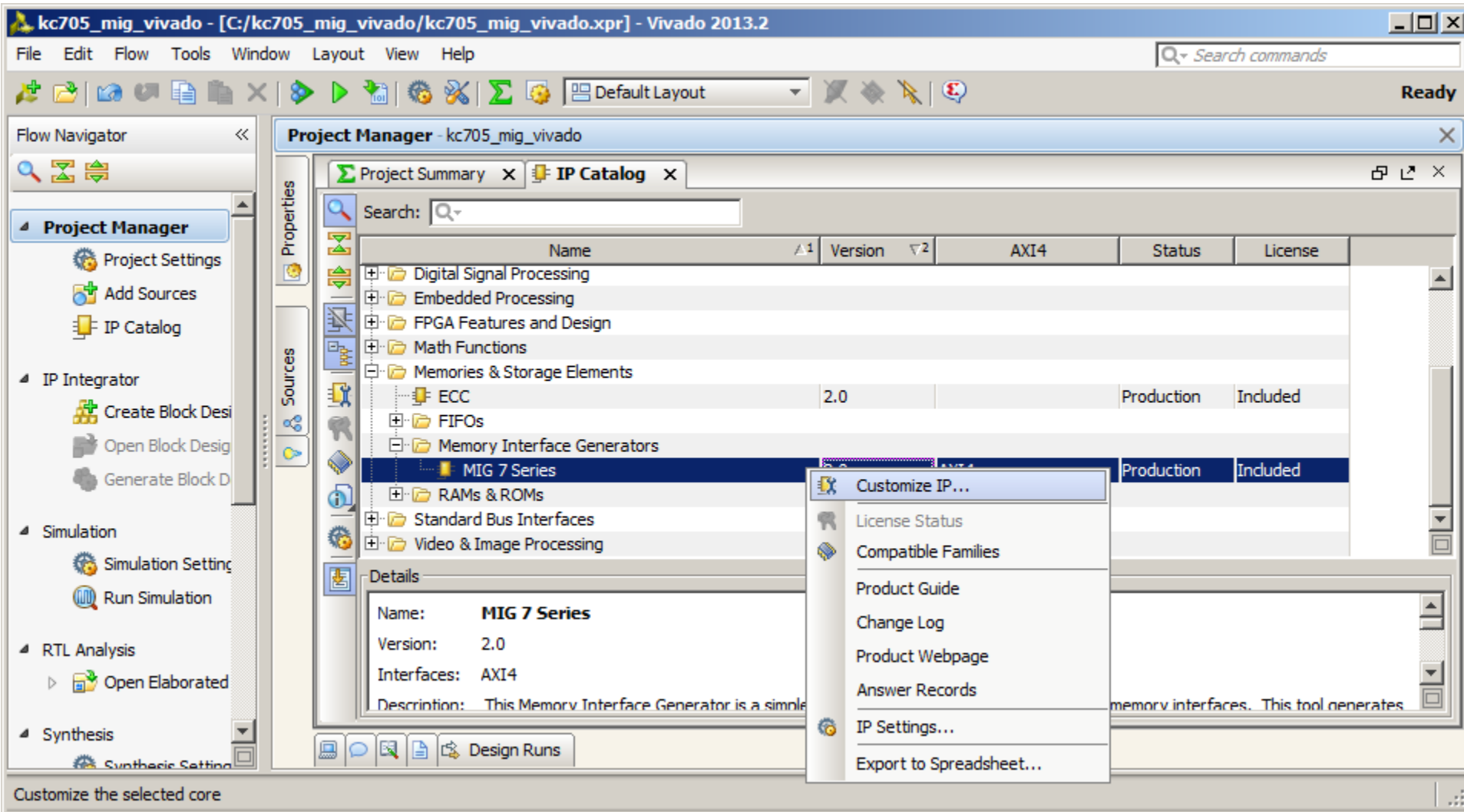
Name: **MIG 7 Series**
Version: 2.0
Interfaces: AXI4
Description: This Memory Interface Generator is a simple menu driven tool to generate advanced memory interfaces. This tool generates

IP: MIG 7 Series

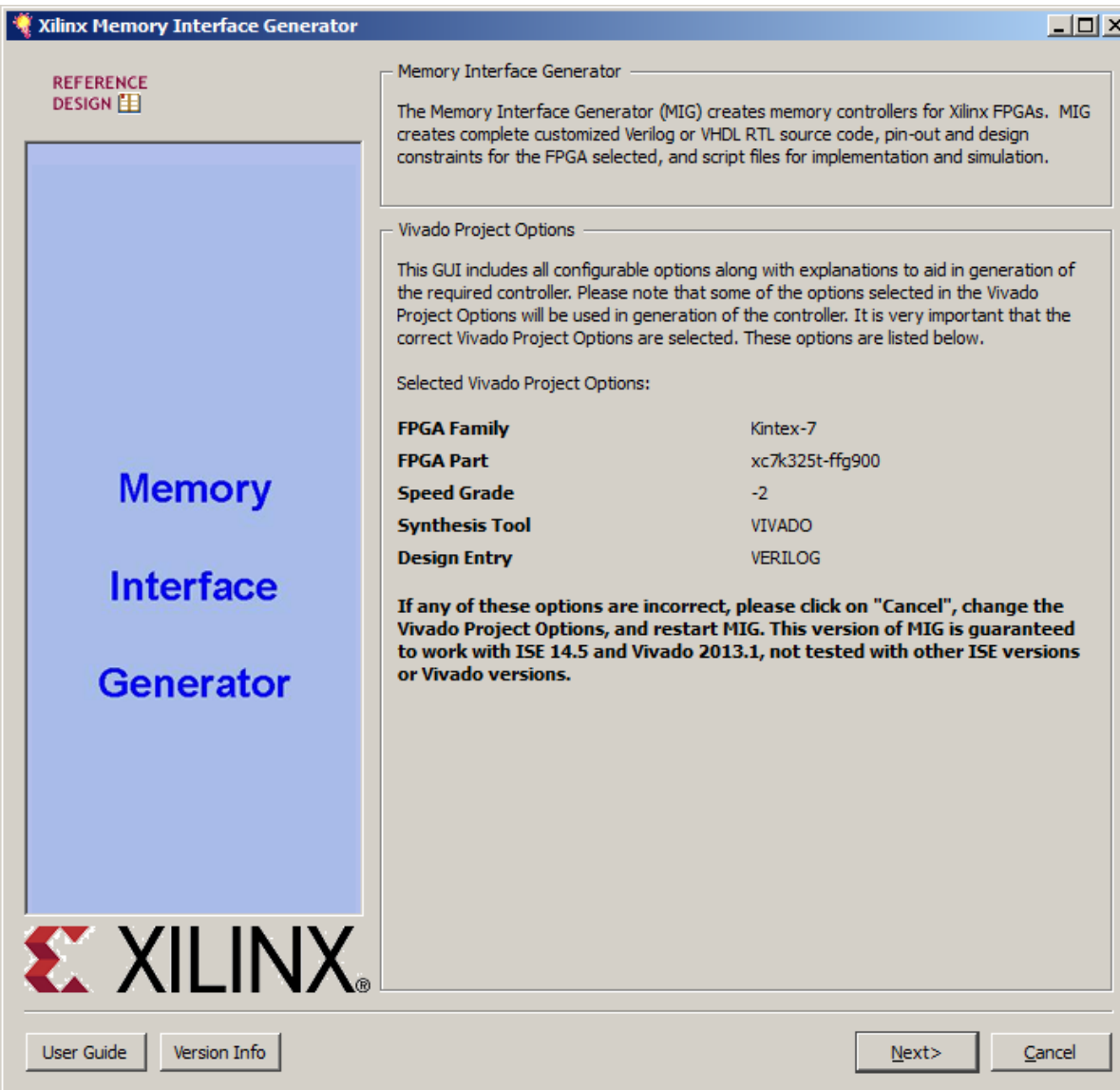
Note: Presentation applies to the KC705

Generate MIG Example Design

- Right click on MIG 7 Series Version
 - Select **Customize IP**



Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

- Leave this page as is
 - Click Next

The screenshot shows a dialog box titled "MIG Output Options" with the following sections:

- MIG Output Options**
 - Create Design**

Select this option to generate a memory controller. Generating a memory controller will create RTL, design constraints (UCF), implementation and simulation files.
 - Verify Pin Changes and Update Design**

Selecting this feature verifies the modified UCF for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input UCF file to be compatible with the current version of MIG. While updating the UCF it preserves the pin outs of the input UCF. This option will also generate the new design with the Component Name you selected in this page.
- Component Name**

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design", "user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.

Component Name
- Multi-Controller**

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDRII+ SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information

Number of Controllers
- AXI4 Interface**

Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.

AXI4 Interface

At the bottom of the dialog box are three buttons: "< Back", "Next >", and "Cancel".

Generate MIG Example Design

- Leave this page as is
 - Click Next

Pin Compatible FPGAs

Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If the target part is changed, use the appropriate UCF in the compatible_ufc folder. **If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated UCF may not work for the new device and a board spin may be required.** MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.

A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.

Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.

Target FPGA

Pin Compatible FPGAs

- [-] kintex7
 - [-] 7k
 - xc7k410t-ffg900

User Guide Version Info < Back Next > Cancel

Note: Presentation applies to the KC705

Generate MIG Example Design



➤ Select Memory Type

- DDR3 SDRAM
- Click Next

Generate MIG Example Design

➤ Select

- Clock Period: **1250 ps**
- Type: **SODIMMs**
- Part: **MT8JTF12864HZ-1G6**
- Data Mask: **Checked**
- Click Next

Options for Controller 0 - DDR3 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range (1072 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information. 1250 ps 800.00 MHz

The allowed period range is PRELIMINARY. The final range will be listed after characterization.

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices. 4:1

Vccaux_io: Vccaux_io must be set to 2.0V in the High Performance banks for the highest data rates. Vccaux_io is not available in the High Range banks. Note that Vccaux_io is common to groups of banks. Consult the 7 Series Datasheets and FPGA SelectIO Resources User Guide for more information. 2.0V

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above. SODIMMs

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II. MT8JTF12864HZ-1G6
Create Custom Part

Memory Voltage: Select the Voltage of the Memory part selected. 1.5V

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above. 64

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported. Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.

Memory Details: 1GB, x8, row:14, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, single rank, 1.5V

< Back Next > Cancel

Generate MIG Example Design

Memory Options for Controller 0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

5000 ps (200 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length
The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control
Programmable impedance for the output buffer.

RZQ/7

Controller Chip Select Pin
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Enable

RTT (nominal) - On Die Termination (ODT)
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 (40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configurations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

RZQ/6

Memory Address Mapping Selection

User Address

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000
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ROW BANK COLUMN

< Back Next> Cancel

➤ Select:

- Input Clock Period: **5000 ps**
- RTT: **RZQ/6**
- Click Next

Generate MIG Example Design

The screenshot shows a configuration window for the MIG (Memory Initialization Generator) example design. The window is titled "Generate MIG Example Design" and contains several sections with dropdown menus and checkboxes.

- System Clock:** Choose the desired input clock configuration. Design clock can be Differential or Single-Ended. **System Clock** is set to **Differential**.
- Reference Clock:** Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended. **Reference Clock** is set to **Use System Clock**.
- System Reset Polarity:** Choose the desired System Reset Polarity. **System Reset Polarity** is set to **ACTIVE HIGH**.
- Debug Signals Control:** This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals. **Debug Signals for Memory Controller** is set to **ON**. **Sample Data Depth** is set to **1024**.
- Internal Vref:** Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs. **Internal Vref** is set to .
- IO Power Reduction:** Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITES and periods of inactivity.

At the bottom of the window, there are three buttons: **< Back**, **Next >**, and **Cancel**.

➤ Select

- Reference Clock: **Use System Clock**
- System Reset: **ACTIVE HIGH**
- Debug: **ON**
- Click Next

Generate MIG Example Design

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- AXI Parameter
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options
- IO Planning Options
- Bank Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB Information
- Design Notes

Internal Termination for High Range Banks

Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies **only** to the HR banks used in the interface.

Internal Termination Impedance 50 Ohms

DDR3 SDRAM

Digitally Controlled Impedance (DCI)

The DCI (Digitally Controlled Impedance) I/O standards are applied appropriately in High Performance banks. DQ and DQS/DQS# signals utilize DCI standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). DCI is not used for the Address/Control output signals. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.

DCI Cascading Information

Select the DCI Cascade for the DCI reference pins to achieve better pin efficiency. The constraint file must be updated manually to select the Master/Slave banks.

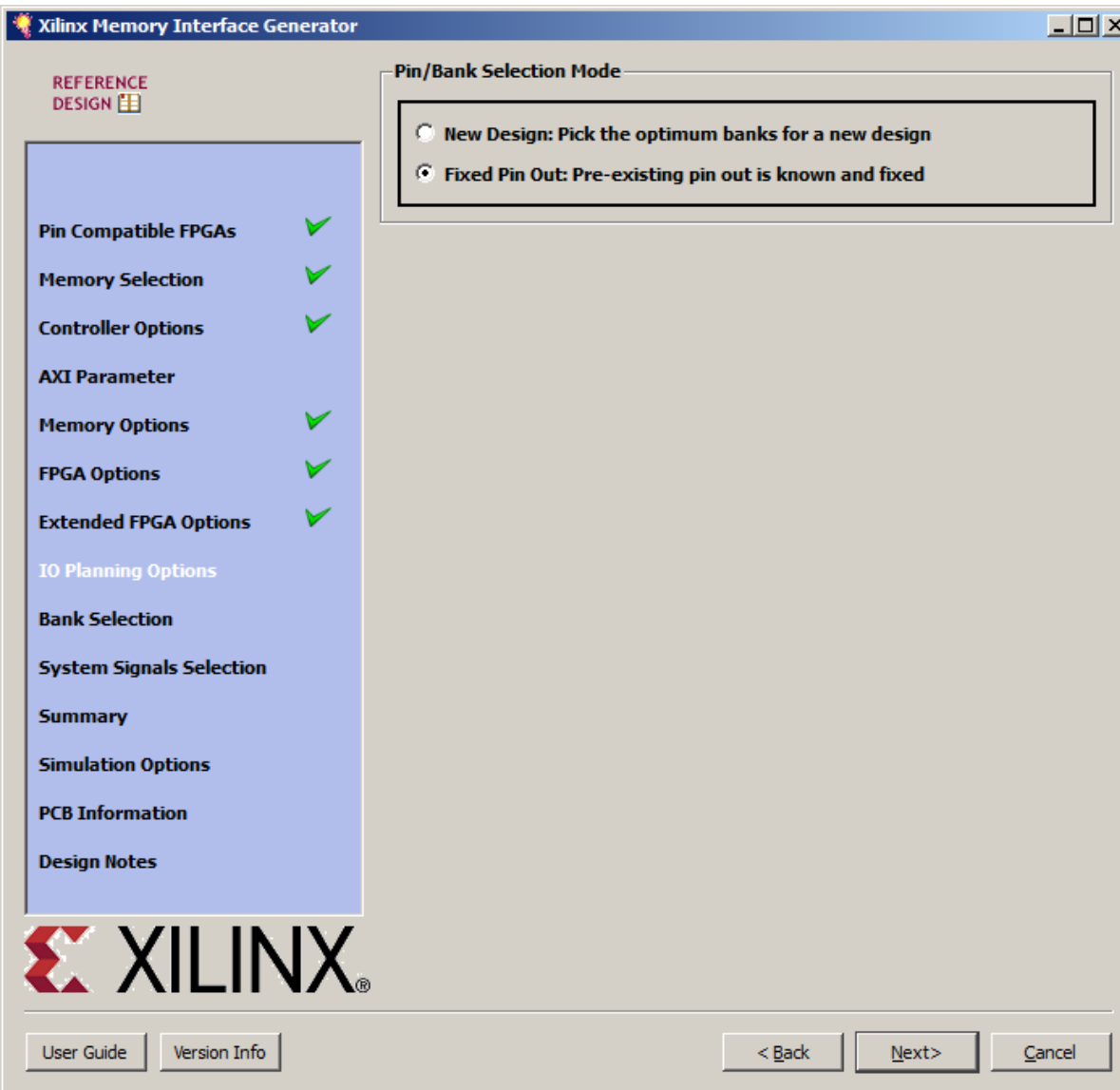
DCI Cascade

User Guide Version Info < Back Next > Cancel

➤ Select

- DCI Cascade: **Checked**
- Click Next

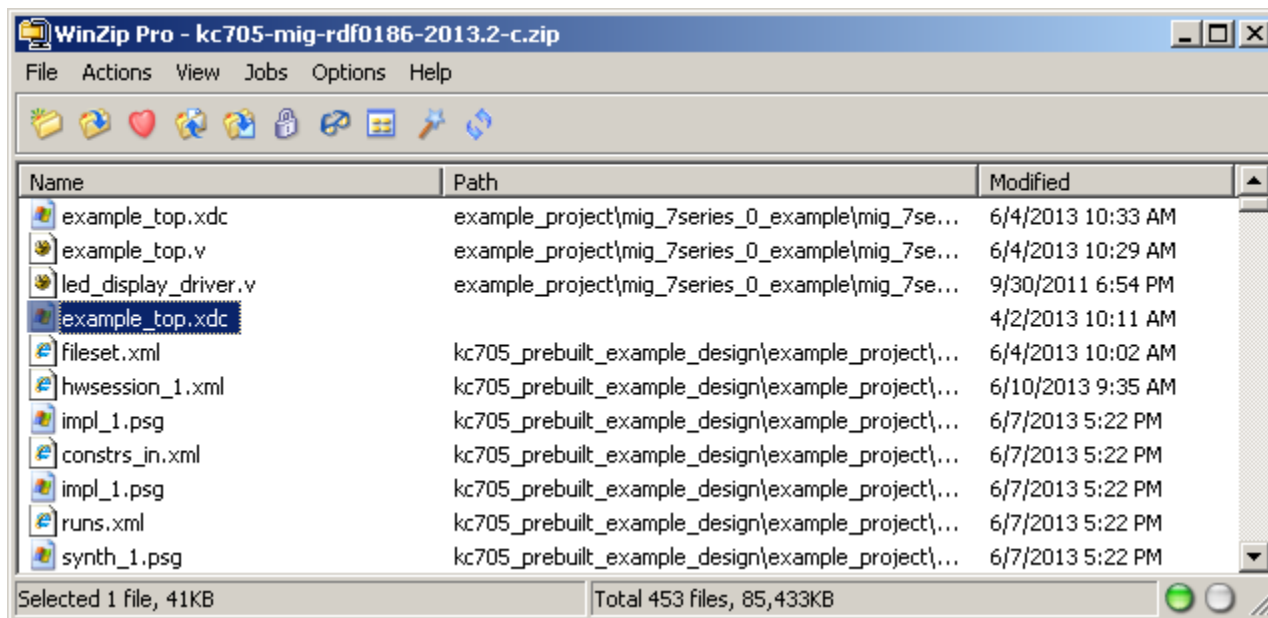
Generate MIG Example Design



- **Select Fixed Pin Out**
 - Click Next

Modifications to Example Design

- Open the KC705 MIG Vivado Design Files (2013.2 C)
 - Available through <http://www.xilinx.com/kc705>
 - Extract the file, “**example_top.xdc**” *only* to C:\kc705_mig_vivado
 - Contains the constraints needed for KC705 MIG design
 - This zip file will be needed later in the presentation



Generate MIG Example Design

➤ Select Read XDC/UCF

- Open the file:
example_top.xdc

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	All Banks	Select Byte	Select Pin	
2	ddr3_dq[1]	All Banks	Select Byte	Select Pin	
3	ddr3_dq[2]	All Banks	Select Byte	Select Pin	
4	ddr3_dq[3]	All Banks	Select Byte	Select Pin	
5	ddr3_dq[4]	All Banks	Select Byte	Select Pin	
6	ddr3_dq[5]	All Banks	Select Byte	Select Pin	
7	ddr3_dq[6]	All Banks	Select Byte	Select Pin	
8	ddr3_dq[7]	All Banks	Select Byte	Select Pin	
9	ddr3_dq[8]	All Banks	Select Byte	Select Pin	
10	ddr3_dq[9]	All Banks	Select Byte	Select Pin	
11	ddr3_dq[10]	All Banks	Select Byte	Select Pin	
12	ddr3_dq[11]	All Banks	Select Byte	Select Pin	
13	ddr3_dq[12]	All Banks	Select Byte	Select Pin	
14	ddr3_dq[13]	All Banks	Select Byte	Select Pin	
15	ddr3_dq[14]	All Banks	Select Byte	Select Pin	
16	ddr3_dq[15]	All Banks	Select Byte	Select Pin	

INFO : Press Validate to proceed.

Validate **Read XDC/UCF** Save

< Back Next >

Load your UCF

Look in: kc705_mig_vivado

- kc705_mig_vivado.cache
- kc705_mig_vivado.data
- kc705_mig_vivado.runs
- kc705_mig_vivado.srds
- example_top.xdc**

File name: example_top.xdc

Files of type: Constraint Files (*.xdc *.ucf)

Note: Presentation applies to the KC705

Generate MIG Example Design

- Once it finishes reading in the XDC, click **Validate**
 - Click OK

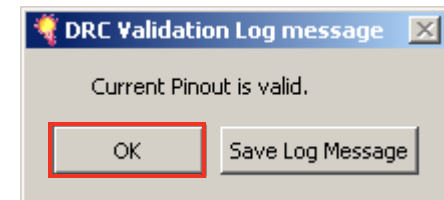
Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	32	T3	AA15	SSTL15_T_DCI
2	ddr3_dq[1]	32	T3	AA16	SSTL15_T_DCI
3	ddr3_dq[2]	32	T3	AC14	SSTL15_T_DCI
4	ddr3_dq[3]	32	T3	AD14	SSTL15_T_DCI
5	ddr3_dq[4]	32	T3	AA17	SSTL15_T_DCI
6	ddr3_dq[5]	32	T3	AB15	SSTL15_T_DCI
7	ddr3_dq[6]	32	T3	AE15	SSTL15_T_DCI
8	ddr3_dq[7]	32	T3	Y15	SSTL15_T_DCI
9	ddr3_dq[8]	32	T2	AB19	SSTL15_T_DCI
10	ddr3_dq[9]	32	T2	AD16	SSTL15_T_DCI
11	ddr3_dq[10]	32	T2	AC19	SSTL15_T_DCI
12	ddr3_dq[11]	32	T2	AD17	SSTL15_T_DCI
13	ddr3_dq[12]	32	T2	AA18	SSTL15_T_DCI
14	ddr3_dq[13]	32	T2	AB18	SSTL15_T_DCI
15	ddr3_dq[14]	32	T2	AE18	SSTL15_T_DCI
16	ddr3_dq[15]	32	T2	AD18	SSTL15_T_DCI

INFO : Press Validate to proceed.

Validate Read XDC/UCF Save PinOut

< Back Next > Cancel



Generate MIG Example Design

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	32	T3	AA15	SSTL15_T_DCI
2	ddr3_dq[1]	32	T3	AA16	SSTL15_T_DCI
3	ddr3_dq[2]	32	T3	AC14	SSTL15_T_DCI
4	ddr3_dq[3]	32	T3	AD14	SSTL15_T_DCI
5	ddr3_dq[4]	32	T3	AA17	SSTL15_T_DCI
6	ddr3_dq[5]	32	T3	AB15	SSTL15_T_DCI
7	ddr3_dq[6]	32	T3	AE15	SSTL15_T_DCI
8	ddr3_dq[7]	32	T3	Y15	SSTL15_T_DCI
9	ddr3_dq[8]	32	T2	AB19	SSTL15_T_DCI
10	ddr3_dq[9]	32	T2	AD16	SSTL15_T_DCI
11	ddr3_dq[10]	32	T2	AC19	SSTL15_T_DCI
12	ddr3_dq[11]	32	T2	AD17	SSTL15_T_DCI
13	ddr3_dq[12]	32	T2	AA18	SSTL15_T_DCI
14	ddr3_dq[13]	32	T2	AB18	SSTL15_T_DCI
15	ddr3_dq[14]	32	T2	AE18	SSTL15_T_DCI
16	ddr3_dq[15]	32	T2	AD18	SSTL15_T_DCI

INFO : Validation successful. Press Next to proceed.

Validate Read XDC/UCF Save PinOut

< Back **Next>** Cancel

- The Next button is enabled once the pinout is validated.
 - Click Next

Generate MIG Example Design

- Leave this page as is
 - Click Next

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the UCF after the design is generated. For more information see [UG586 Bank and Pin rules](#).

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Clock Pin Selection

The **sys_clk** is used as the system clock for the memory interface. This signal should be connected to a low jitter external clock source via a differential (P/N) pair for best performance. This signal should be in the address/control bank, but may be placed in an adjacent bank if there are not enough pins available such as when fitting a 16 bit interface in a single bank.

	Signal Name	Bank Number	Pin Number
1	sys_clk_p/n	33	AD12/AD11(CC_P/N)

Reference Clock Pin Selection

The **clk_ref** input is used as the reference clock for the IODELAY. Refer the "7 Series FPGA SelectIO Resources User Guide" for more information. This input can be generated internally or can be connected to an external clock source on a clock capable differential (P/N) pair. This selection will be faded when Reference Clock type chosen is **Use System Clock**.

	Signal Name	Bank Number	Pin Number
1	clk_ref_p/n	Select Bank	Select Pin

Status Signals

These signals may be connected internally to other logic or brought out to a pin.

All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).

< Back Next > Cancel

Generate MIG Example Design

- Leave this page as is
 - Click Next

Xilinx Memory Interface Generator

REFERENCE DESIGN

Pin Compatible FPGAs ✓
Memory Selection ✓
Controller Options ✓
AXI Parameter
Memory Options ✓
FPGA Options ✓
Extended FPGA Options ✓
IO Planning Options ✓
Pin Selection ✓
System Signals Selection ✓
Summary
Simulation Options
PCB Information
Design Notes

Vivado Project Options:
Target Device : xc7k325t-ffg900
Speed Grade : -2
HDL : verilog
Synthesis Tool : VIVADO

If any of the above options are incorrect, please click on "Cancel", change the CORE Generator Project Options, and restart MIG.

MIG Output Options:
Module Name : mig_7series_0
No of Controllers : 1
Selected Compatible Device(s) : --

FPGA Options:
System Clock Type : Differential
Reference Clock Type : Use System Clock
Debug Port : ON
Internal Vref : disabled
IO Power Reduction : ON
XADC instantiation in MIG : Enabled

Extended FPGA Options:
DCI for DQ, DQS/DQS#, DM : enabled
Internal Termination (HR Banks) : 50 Ohms

/*
Controller 0
*/

Print

User Guide Version Info < Back Next > Cancel

Generate MIG Example Design

The screenshot shows the Xilinx Memory Interface Generator (MIG) software interface. On the left, a navigation pane lists various configuration options, all of which are marked with green checkmarks, indicating they have been completed. The main area displays a license agreement for Micron Technology, Inc. Simulation Model License Agreement. The agreement text is as follows:

Micron Technology, Inc. Simulation Model License Agreement

PLEASE READ THIS SIMULATION MODEL LICENSE AGREEMENT ("AGREEMENT") FROM MICRON TECHNOLOGY, INC. ("MTI") CAREFULLY BEFORE INSTALLING OR USING THIS SIMULATION MODEL (THE "MODEL"). BY INSTALLING OR USING THE MODEL, YOU ARE ACCEPTING AND AGREEING TO THE TERMS AND CONDITIONS OF THIS AGREEMENT. IF YOU DO NOT AGREE WITH THE TERMS AND CONDITIONS OF THIS AGREEMENT, THEN DO NOT INSTALL OR USE THE MODEL.

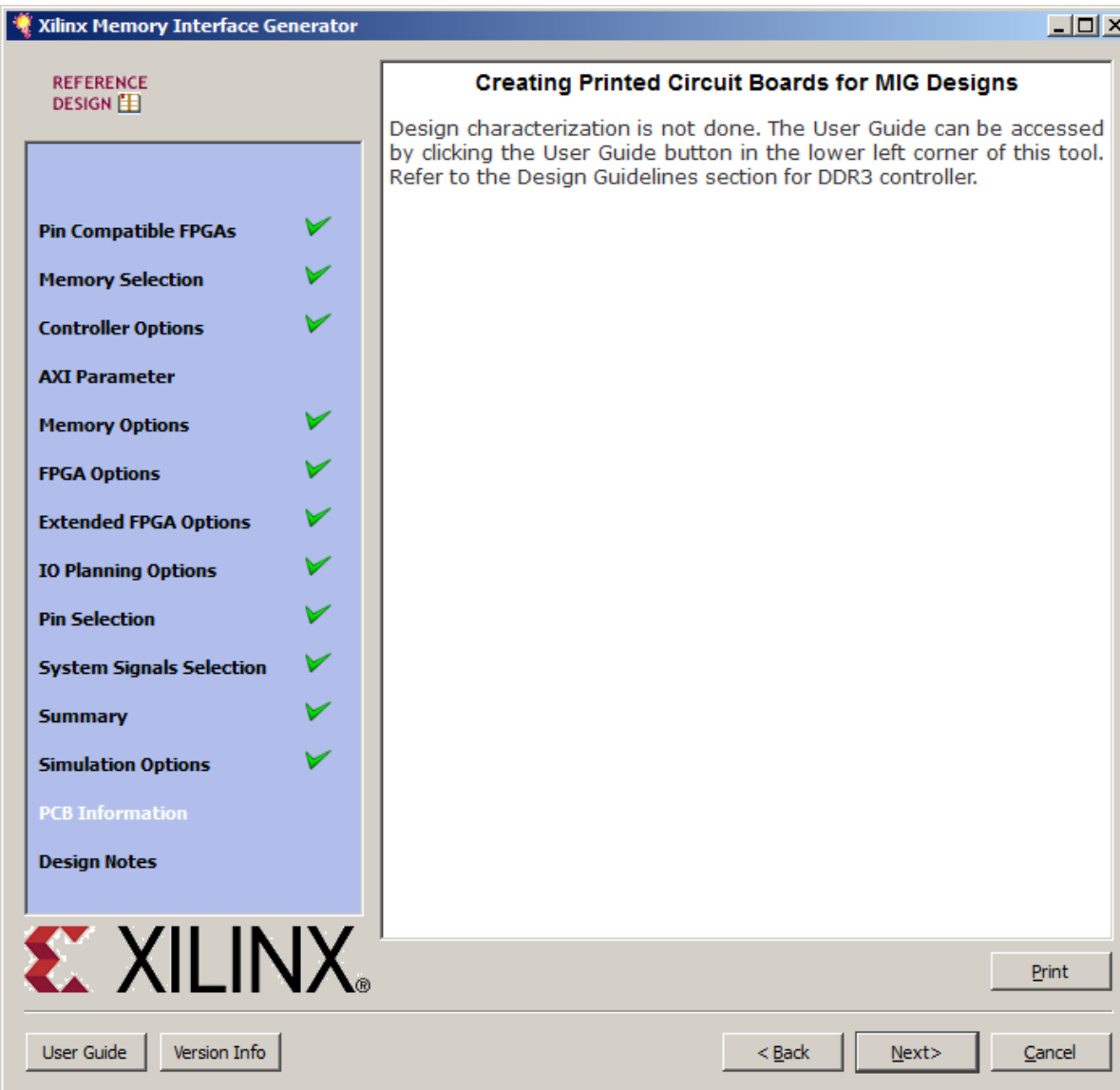
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At the bottom of the window, there are two radio buttons for "Accept" and "Decline", with the "Accept" button selected. Below the radio buttons, there is a "Print" button and a "Check Accept or Decline to proceed" instruction. At the very bottom of the window, there are buttons for "User Guide", "Version Info", "< Back", "Next >", and "Cancel".

- **Accept Simulation license, if desired**
 - Otherwise, Decline license
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

➤ Click Generate

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- AXI Parameter
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options ✓
- IO Planning Options ✓
- Pin Selection ✓
- System Signals Selection ✓
- Summary ✓
- Simulation Options ✓
- PCB Information ✓
- Design Notes

DDR3 SDRAM Design for Kintex-7 FPGAs

Design Notes

1. This design is tested with Vivado 2013.2 version
2. This design is simulated with Questa SIM 10.2a version
3. Components, RDIMMs, UDIMMs and SODIMMs are supported
4. If fly by delays are simulated, they must be limited to 1.2ns
5. Consult the Version Info for known limitations

Key Enhancements from MIG 1.9 to MIG 2.0

1. Added support for ChipScope 2.0

Key Enhancements from MIG 1.7 to MIG 1.8

1. Added support for Verify XDC feature

Key Enhancements from MIG 1.6 to MIG 1.7

1. Support of system clock pin sharing for multi-controller designs

Key Enhancements from MIG 1.5 to MIG 1.6

1. Added support for "No Buffer" option for System Clock

Print

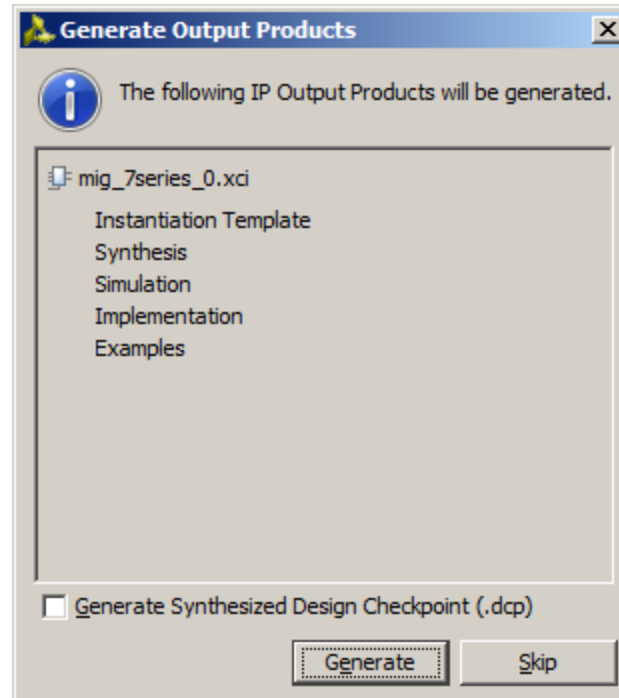
User Guide Version Info < Back Generate Cancel

Note: Presentation applies to the KC705

XILINX ➤ ALL PROGRAMMABLE™

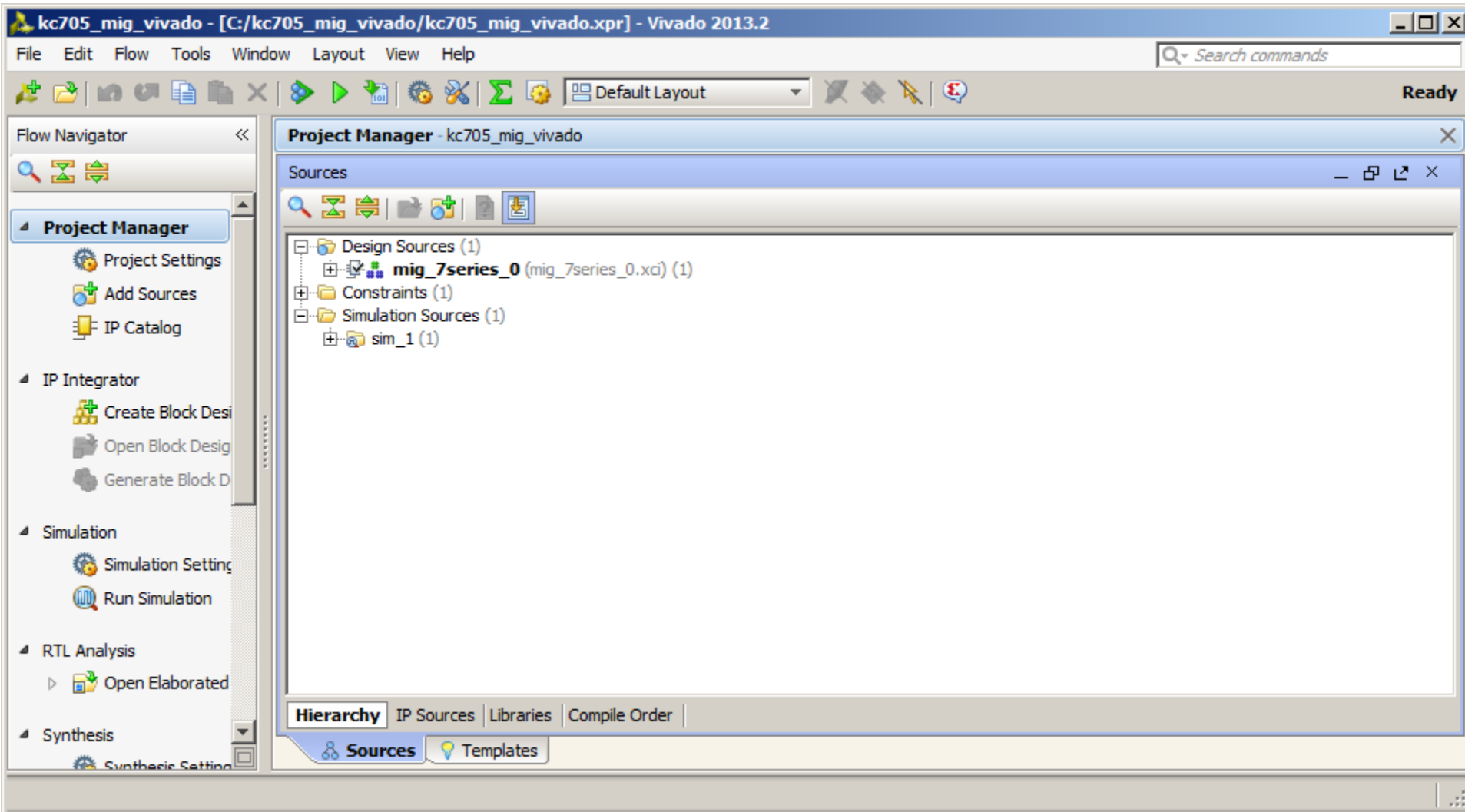
Generate MIG Example Design

➤ Click Generate



Generate MIG Example Design

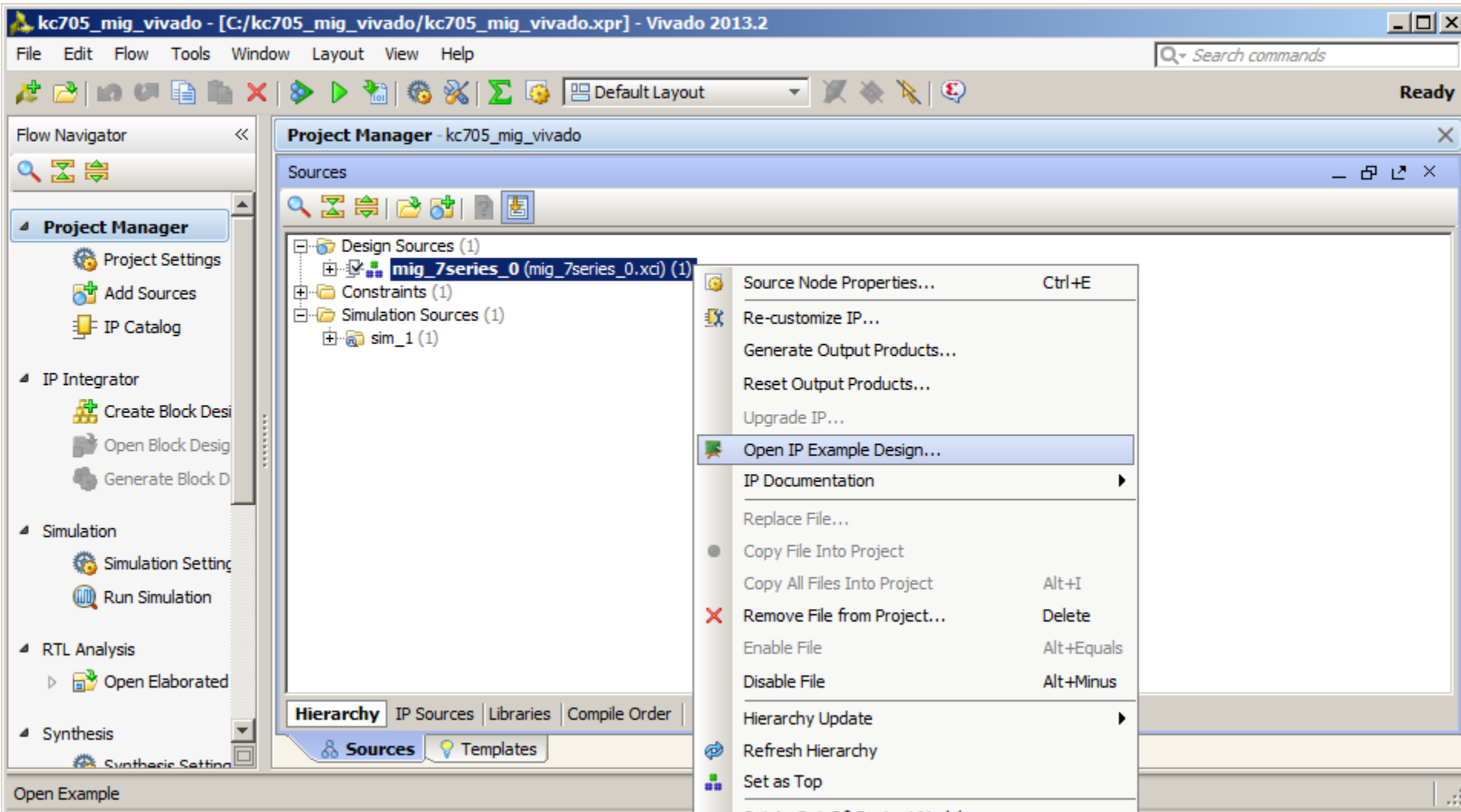
➤ MIG design appears in Design Sources



Note: Presentation applies to the KC705

Compile Example Design

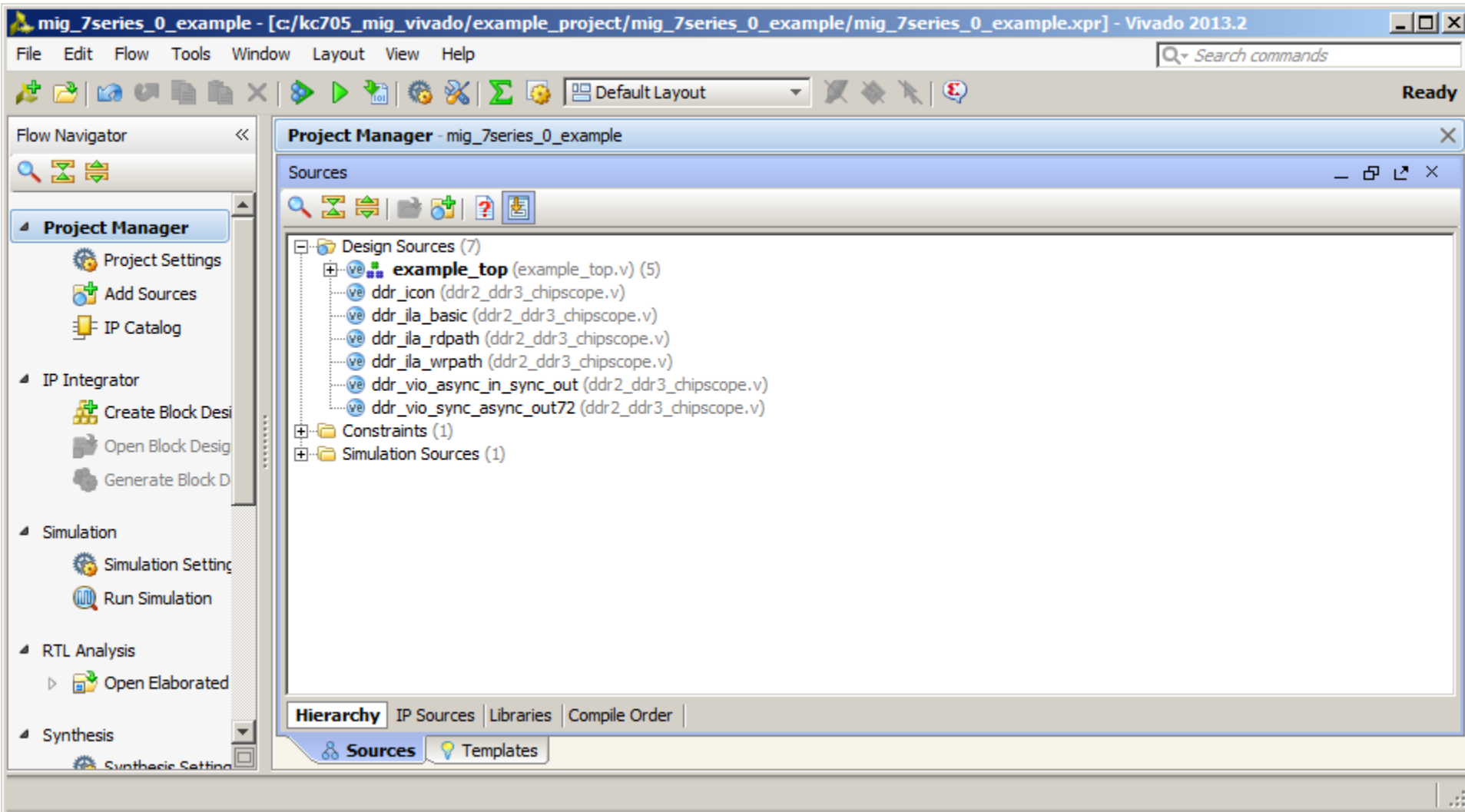
➤ Right click on mig_7series_0 and select Open IP Example Design...



Note: Presentation applies to the KC705

Compile Example Design

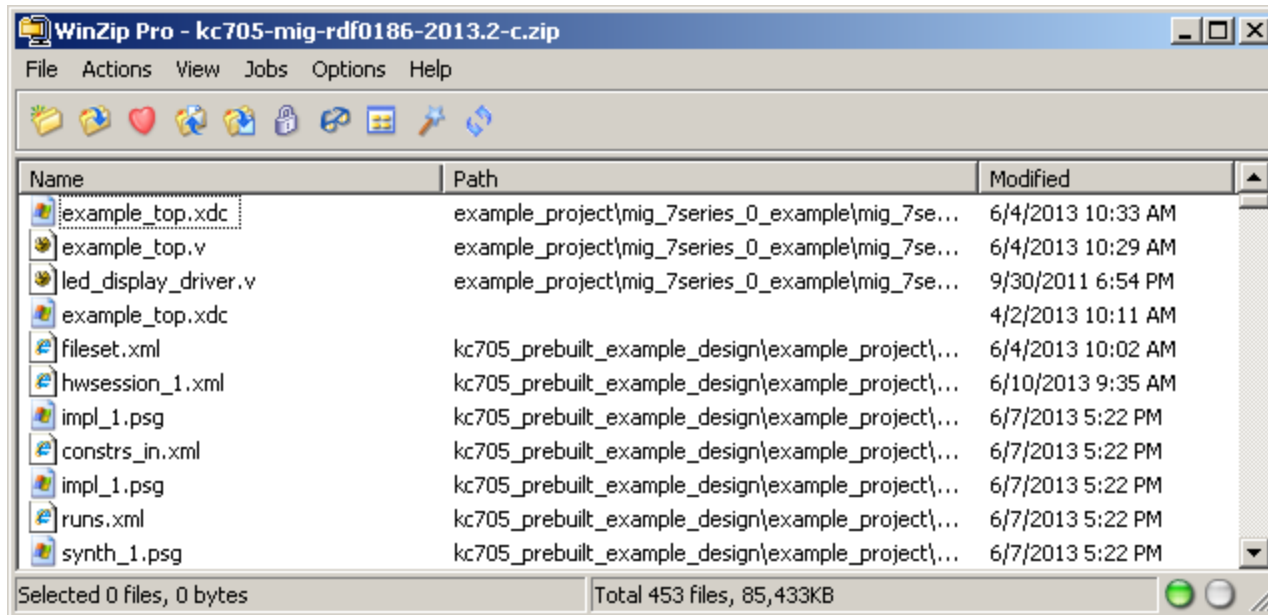
➤ A new project is created under <design path>/example_project



Note: The original project window can be closed

Modifications to Example Design

- Unzip the KC705 MIG Vivado Design Files (2013.2 C) to your C:\kc705_mig_vivado directory
 - Contains several changes needed to support Kintex-7 devices with MIG
 - Do this **after** creating the Example Design; changes only affect the Example Design



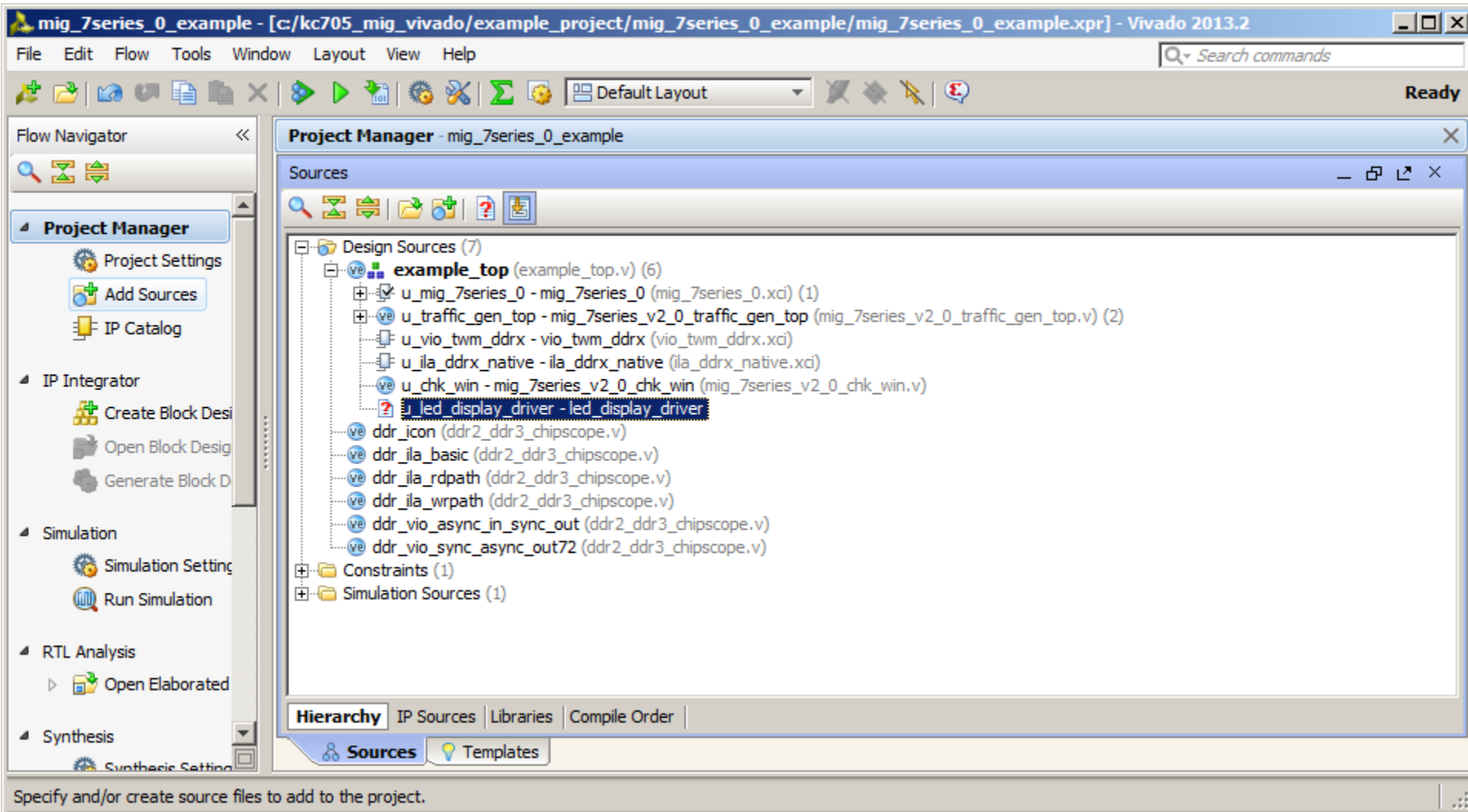
Modifications to Example Design

➤ Modifications to the example design

- Added RTL and XDC modifications to drive LEDs
- Added DCI Cascade constraints to XDC; for more information on using the DCI Cascade constraints for 7 Series refer to [UG899](#)

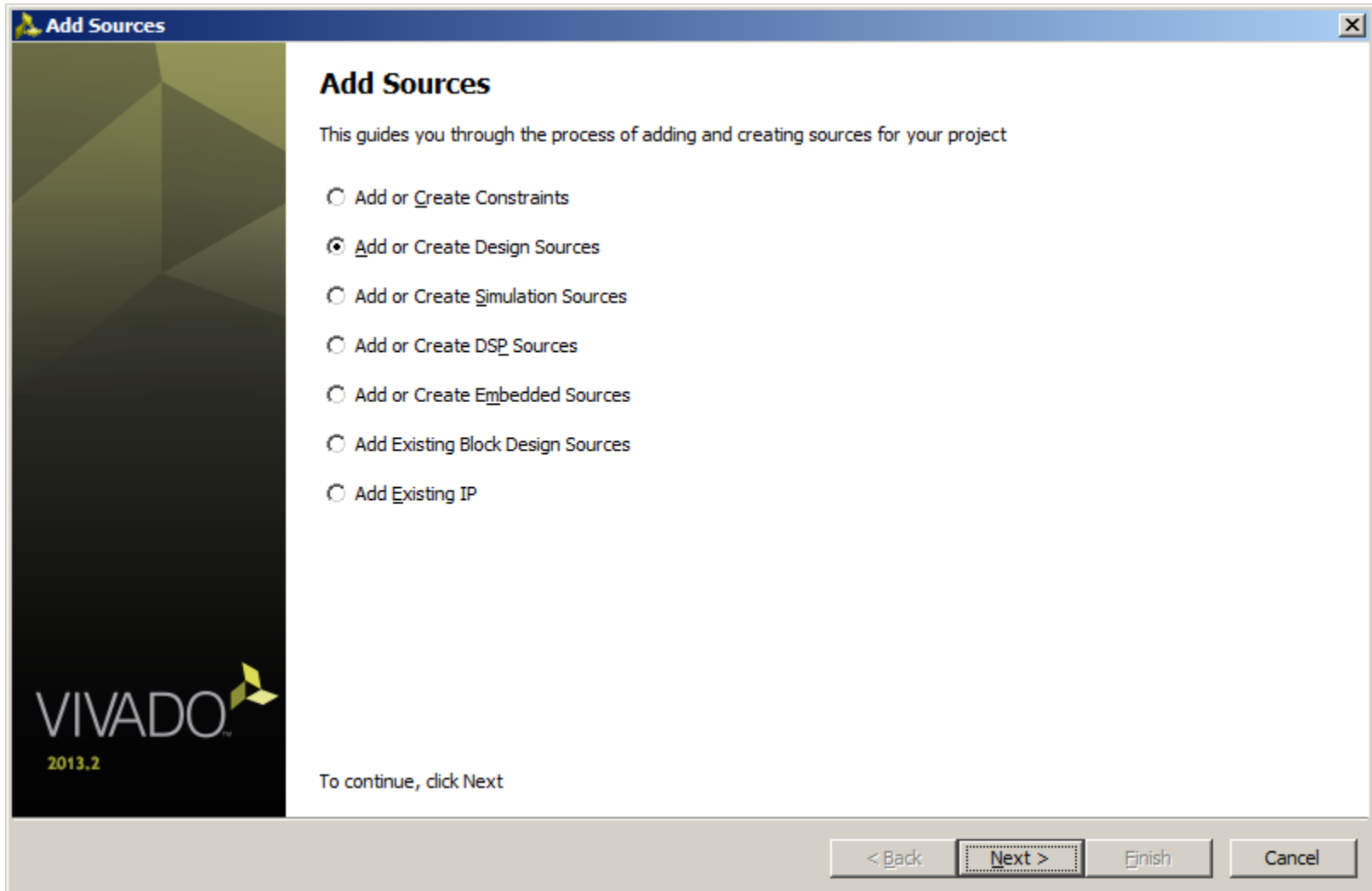
Modifications to Example Design

- The LED Display driver RTL file needs to be added manually
- Click on Add Sources



Modifications to Example Design

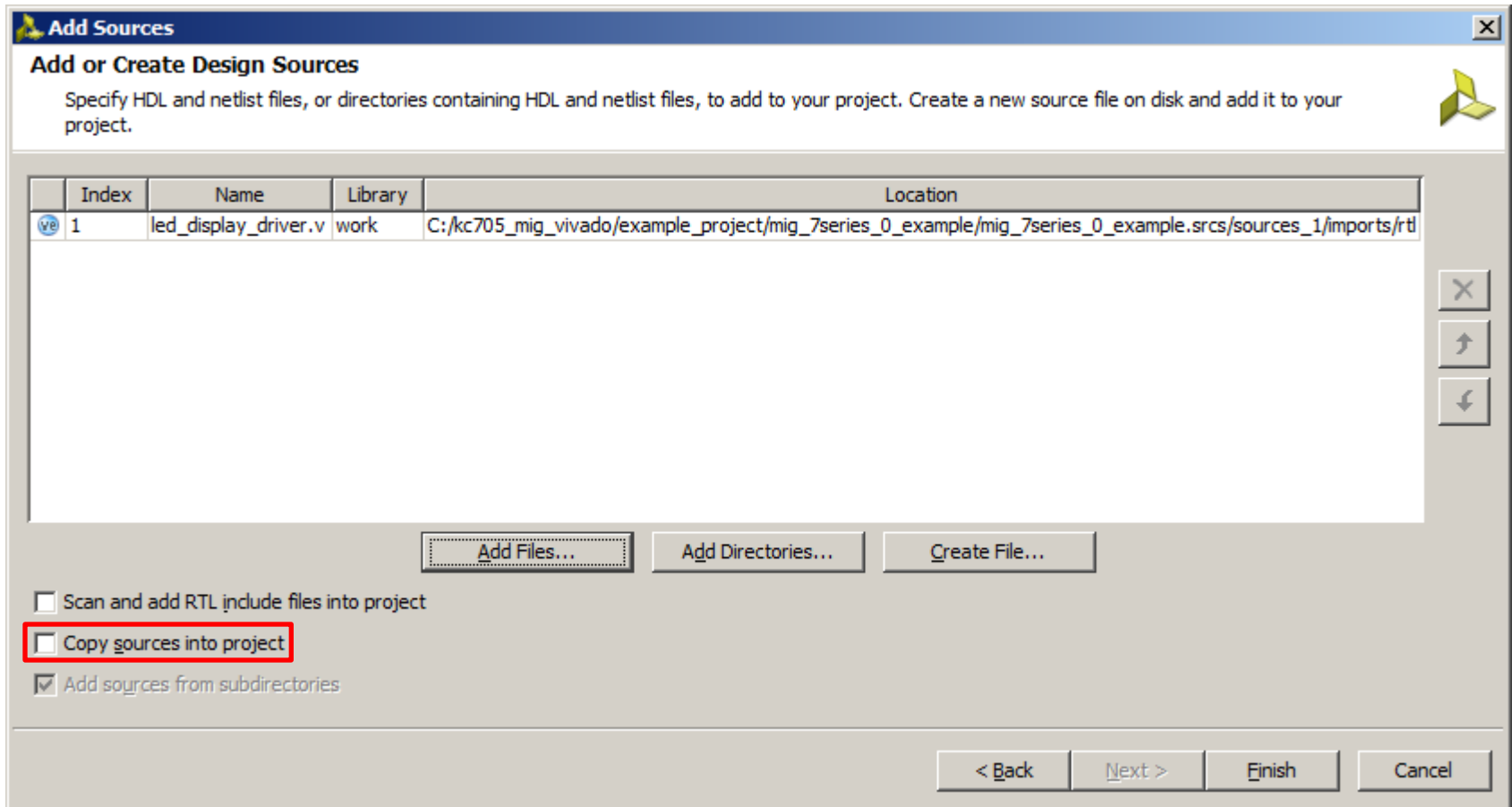
➤ Select Add or Create Design Sources and click Next



Note: Presentation applies to the KC705

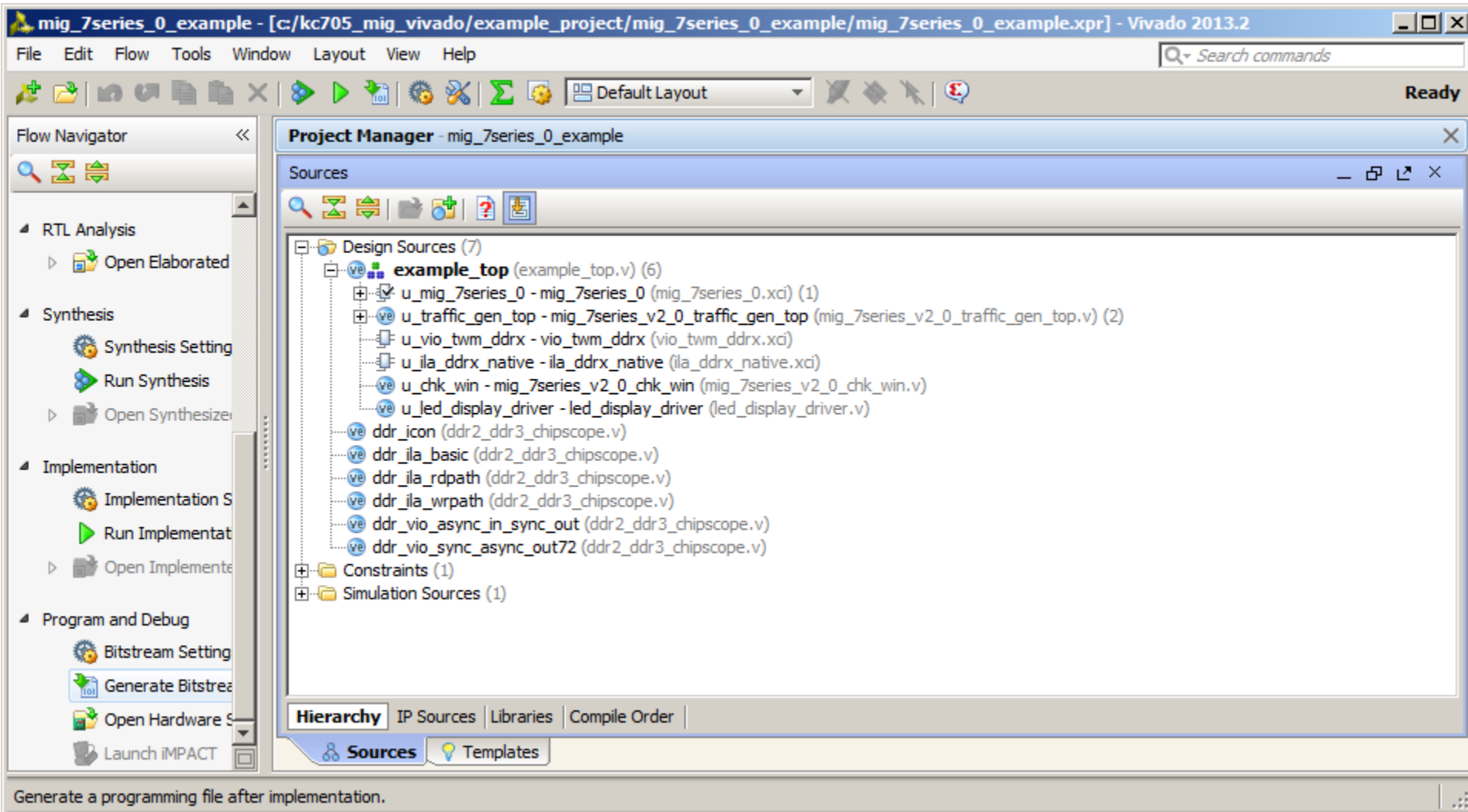
Modifications to Example Design

- Add led_display_driver.v from the example project
- Make sure Copy sources into project is deselected
- Click Finish



Compile Example Design

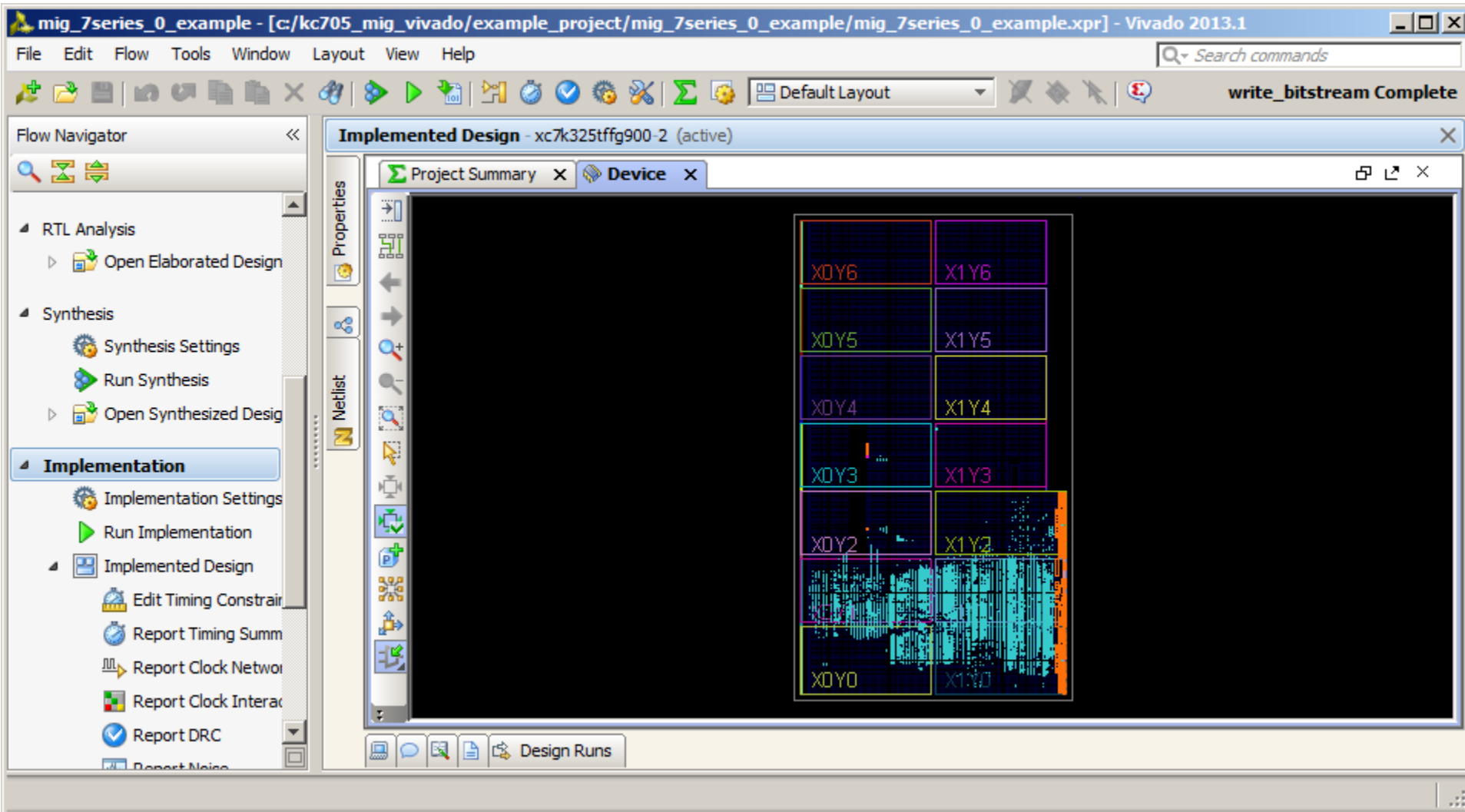
➤ Click on Generate Bitstream



Note: Presentation applies to the KC705

Compile Example Design

➤ Open and view the implemented design



Note: Presentation applies to the KC705

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KC705 Setup

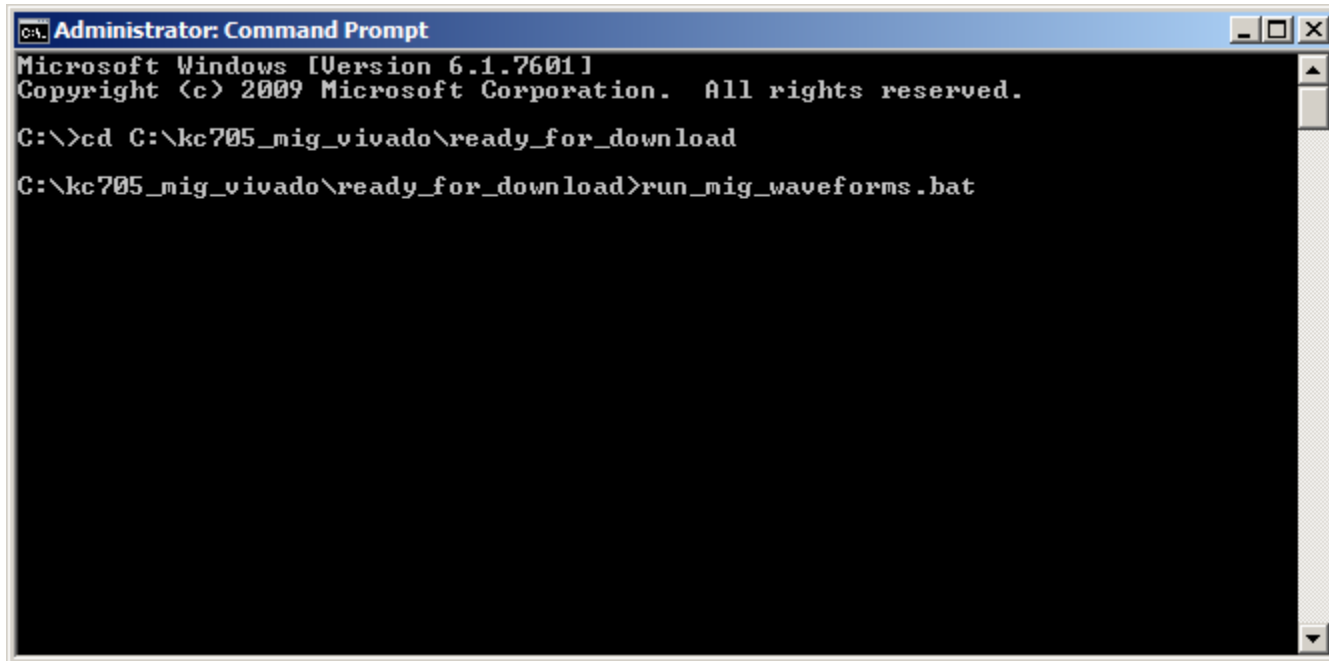


- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
 - Connect this cable to your PC
 - Power on the KC705 board

Run MIG Example Design

➤ From a Command Prompt, type:

```
cd C:\kc705_mig_vivado\ready_for_download  
run_mig_waveforms.bat
```



```
Administrator: Command Prompt  
Microsoft Windows [Version 6.1.7601]  
Copyright (c) 2009 Microsoft Corporation. All rights reserved.  
C:\>cd C:\kc705_mig_vivado\ready_for_download  
C:\kc705_mig_vivado\ready_for_download>run_mig_waveforms.bat
```

Run MIG Example Design

- Under Tcl script control, Vivado opens, loads the bitstream and generates a MIG waveform

The screenshot shows the Vivado 2013.2 interface. The main window is titled "Hardware Session - localhost/xilinx_tcf/Digilent/210203337270A". The "Logic Analyzer" window is open, displaying a waveform for "hw_ila_data_1.wcfg". The waveform shows several signals over time, with a vertical cursor at 1,024. The signals are:

Name	Value
dbg_rddata_valid_r	0
dbg_rddata_r[63:0]	4040404040
dbg_tg_compare_error	0
dbg_cmp_data_valid	0
dbg_cmp_error	0

The waveform shows that the signals are mostly low (0) with some high (1) pulses. The time axis is marked at 0, 2,000, 4,000, and 6,000. The cursor is at 1,024.

Note: Set layout to Logic Analyzer layout to see waveform

Run MIG Example Design

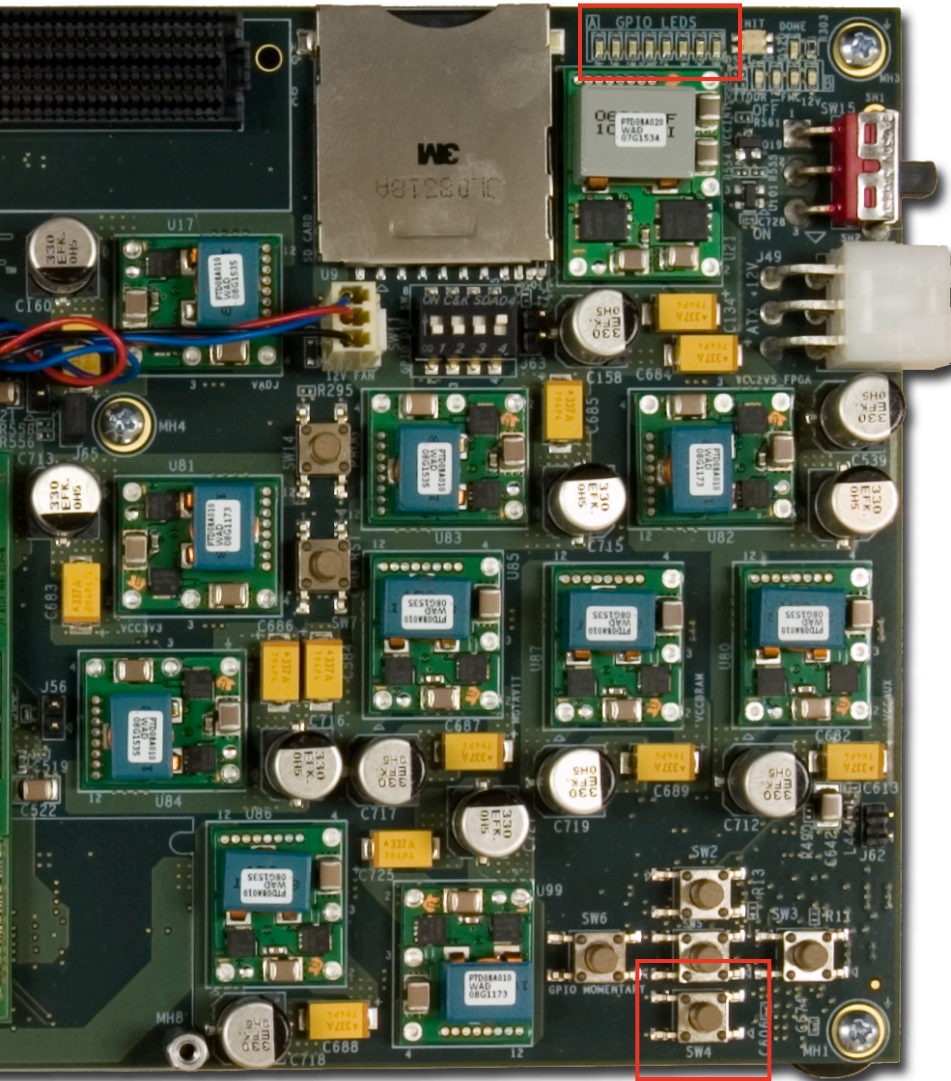
➤ Click and drag to the left to expand the waveform

The screenshot shows the Vivado 2013.2 Logic Analyzer interface. The main window displays a waveform for the design 'hw_ila_data_1.wcfg'. The waveform is currently collapsed, and a 'Zoom Fit X' tooltip is visible over the time axis. The time axis is labeled with values 0, 2,000, 4,000, and 6,000. A yellow vertical line is positioned at 1,024. The waveform shows several signals, including 'dbg_rddata_valid_r', 'dbg_rddata_r[63:0]', 'dbg_tg_compare_error', 'dbg_cmp_data_valid', and 'dbg_cmp_error'. The 'dbg_rddata_r[63:0]' signal is highlighted in green. The 'Value' column in the table below shows the current values for each signal.

Name	Value
dbg_rddata_valid_r	0
dbg_rddata_r[63:0]	4040404040
dbg_tg_compare_error	0
dbg_cmp_data_valid	0
dbg_cmp_error	0

Note: Presentation applies to the KC705

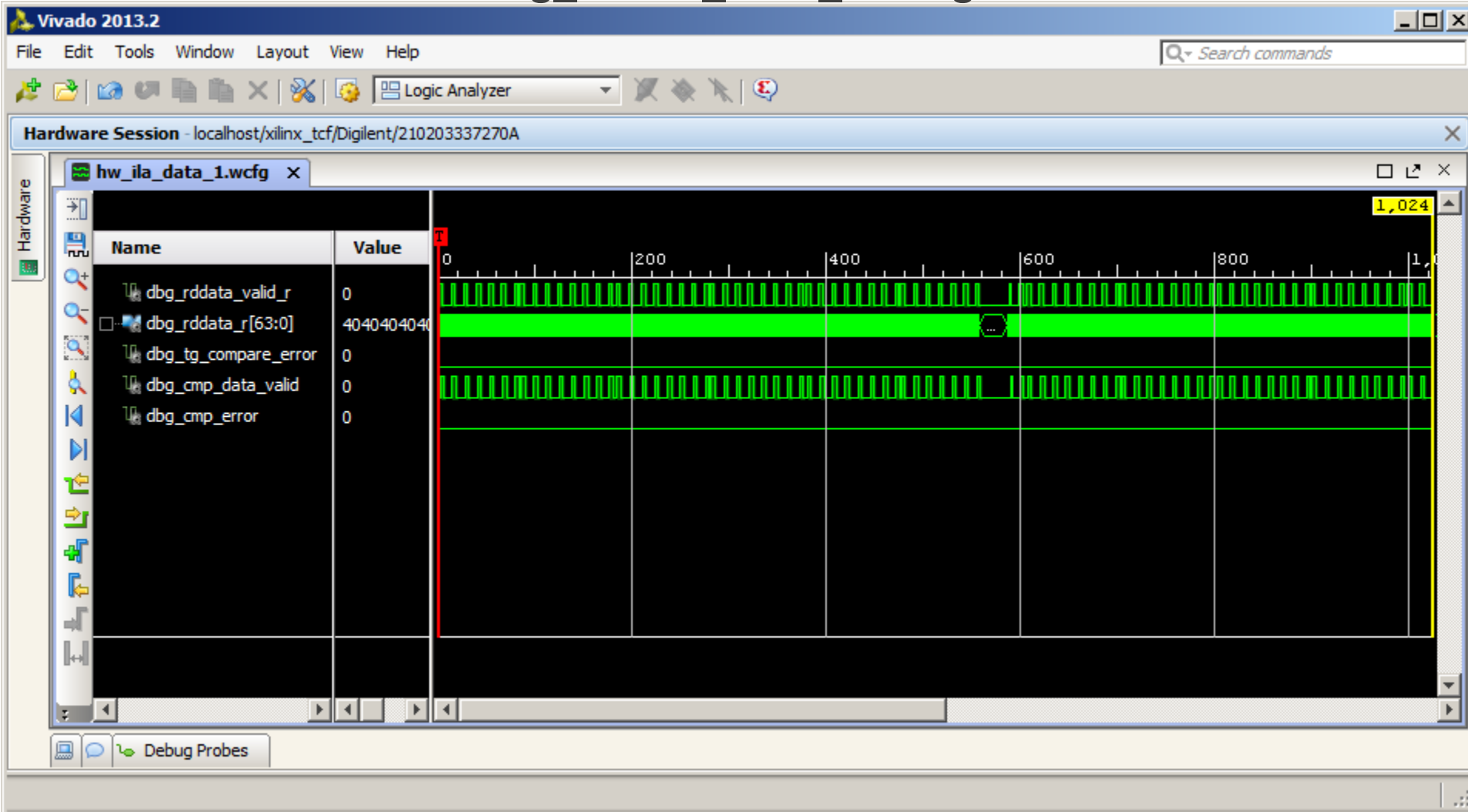
Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
 - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
 - The “South” button, SW4, is the reset

Run MIG Example Design

- View waveforms
- Data is valid when dbg_rddata_valid_r is high



Run MIG Example Design

➤ Click and drag to the right to zoom in

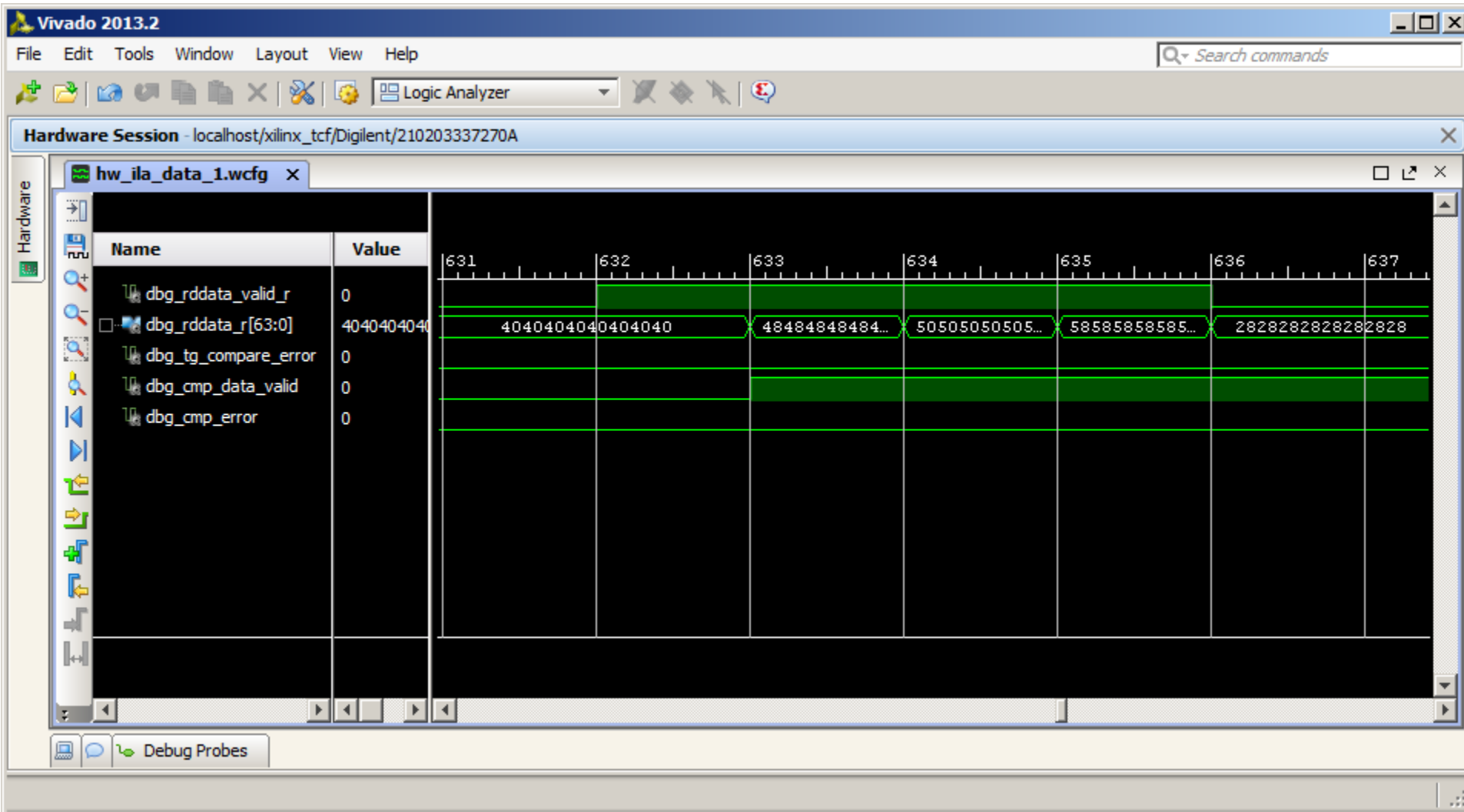
The screenshot shows the Vivado 2013.2 Logic Analyzer interface. The main window displays a waveform for the signal `dbg_rddata_r[63:0]`. The waveform is zoomed in, showing a red vertical line at 626 and a yellow vertical line at 640. A tooltip indicates the zoomed range is from 626 to 640. The signal value is shown as 4040404040. The interface includes a menu bar (File, Edit, Tools, Window, Layout, View, Help), a search bar, and a toolbar with various icons. The hardware session is identified as `localhost/xilinx_tcf/Digilent/210203337270A`. The hardware configuration is `hw_ila_data_1.wcfg`. The signal list on the left includes `dbg_rddata_valid_r`, `dbg_rddata_r[63:0]`, `dbg_tg_compare_error`, `dbg_cmp_data_valid`, and `dbg_cmp_error`. The signal values are 0 for all except `dbg_rddata_r[63:0]` which is 4040404040. The bottom status bar shows `Debug Probes`.

Name	Value
<code>dbg_rddata_valid_r</code>	0
<code>dbg_rddata_r[63:0]</code>	4040404040
<code>dbg_tg_compare_error</code>	0
<code>dbg_cmp_data_valid</code>	0
<code>dbg_cmp_error</code>	0

Note: Presentation applies to the KC705

Run MIG Example Design

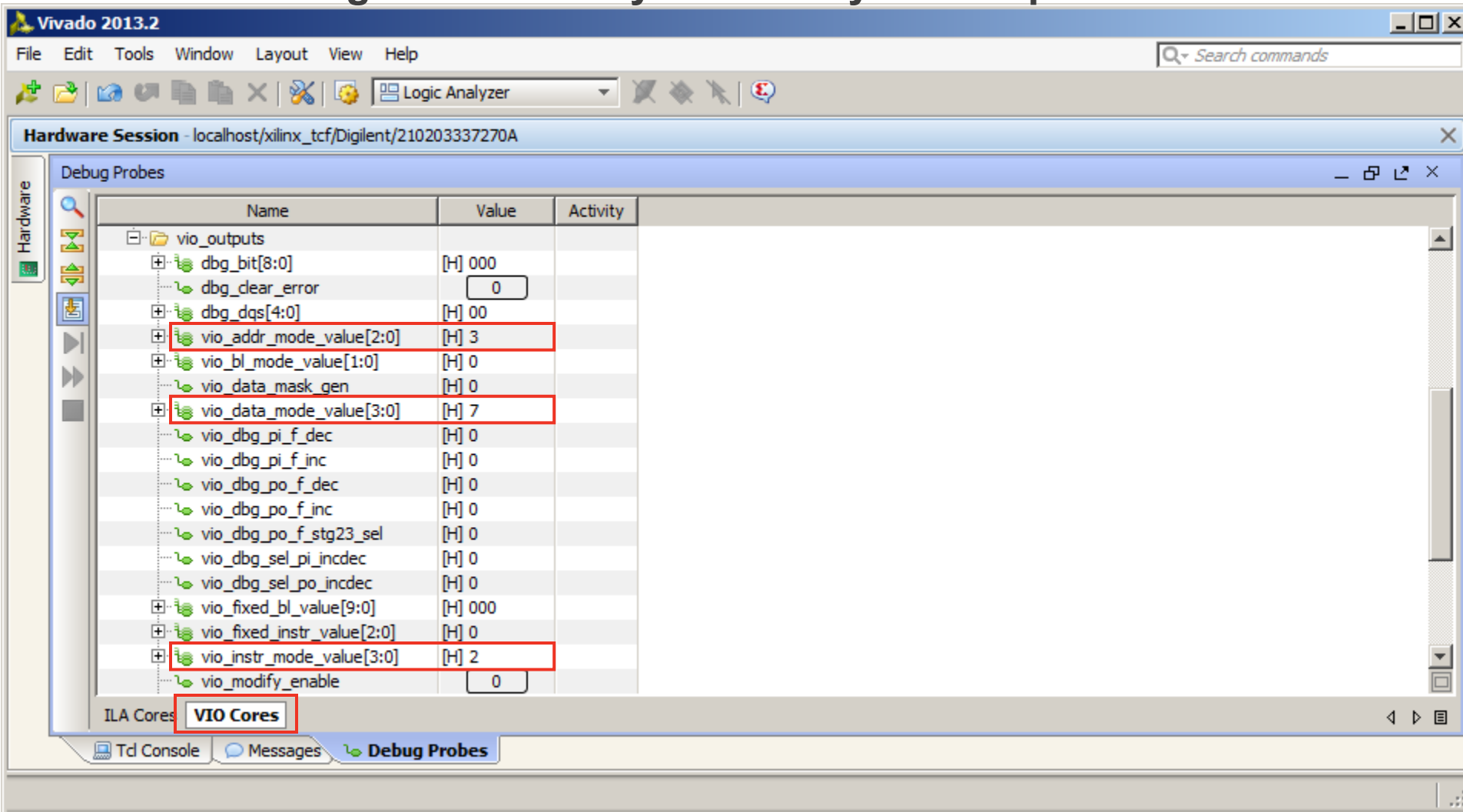
➤ View waveform details



Note: Presentation applies to the KC705

Adjust Data Pattern using VIO Console

- Under the Debug Probes, view the vio_outputs of the VIO Cores
- PRBS settings were already entered by the script but not activated

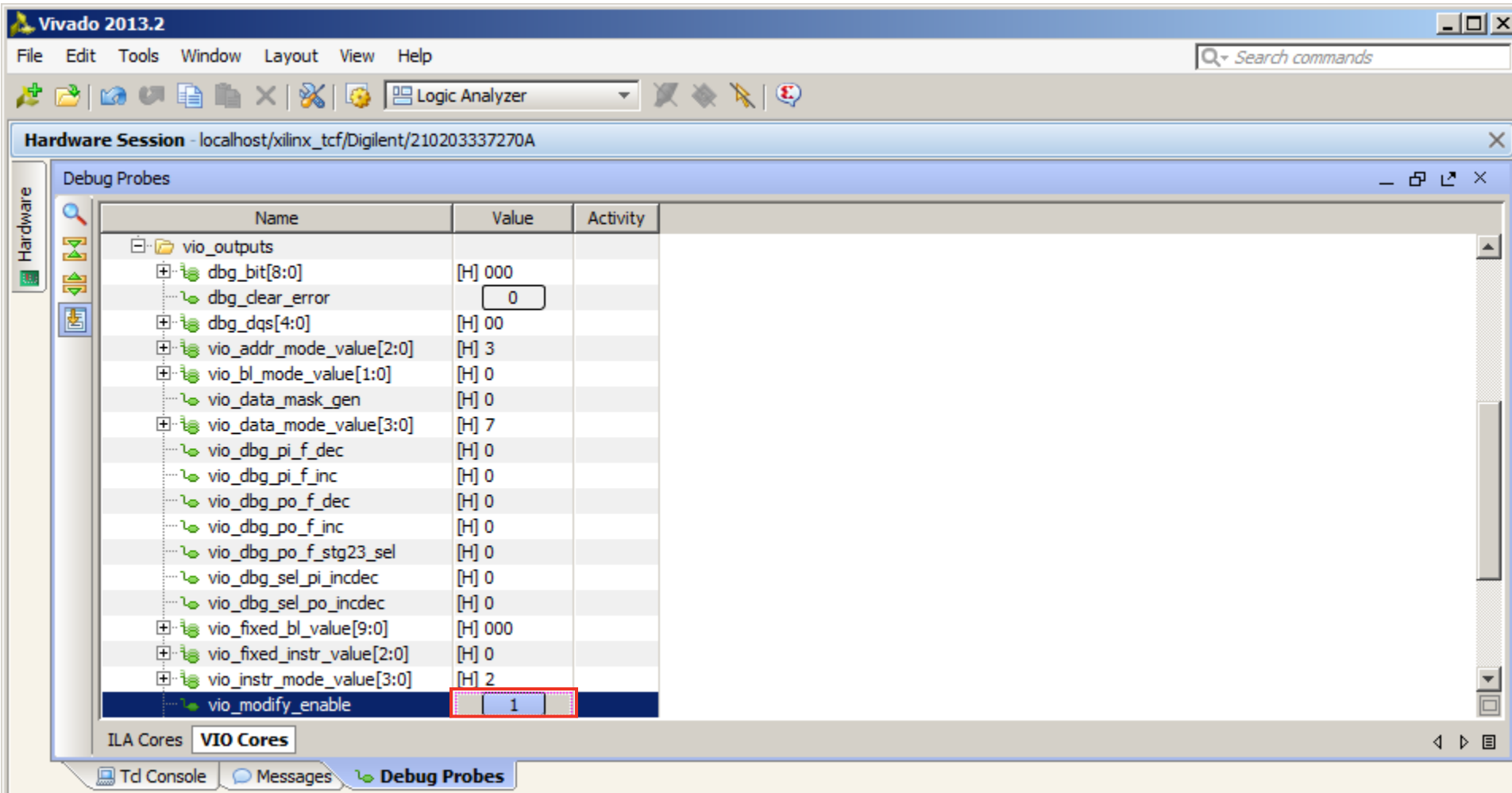


The screenshot shows the Vivado 2013.2 interface with the Debug Probes window open. The window title is "Hardware Session - localhost/xilinx_tcf/Digilent/210203337270A". The "Debug Probes" window displays a table of signals and their values. The "VIO Cores" tab is selected at the bottom. The table is as follows:

Name	Value	Activity
vio_outputs		
dbg_bit[8:0]	[H] 000	
dbg_clear_error	0	
dbg_dqs[4:0]	[H] 00	
vio_addr_mode_value[2:0]	[H] 3	
vio_bl_mode_value[1:0]	[H] 0	
vio_data_mask_gen	[H] 0	
vio_data_mode_value[3:0]	[H] 7	
vio_dbg_pi_f_dec	[H] 0	
vio_dbg_pi_f_inc	[H] 0	
vio_dbg_po_f_dec	[H] 0	
vio_dbg_po_f_inc	[H] 0	
vio_dbg_po_f_stg23_sel	[H] 0	
vio_dbg_sel_pi_incdec	[H] 0	
vio_dbg_sel_po_incdec	[H] 0	
vio_fixed_bl_value[9:0]	[H] 000	
vio_fixed_instr_value[2:0]	[H] 0	
vio_instr_mode_value[3:0]	[H] 2	
vio_modify_enable	0	

Adjust Data Pattern using VIO Console

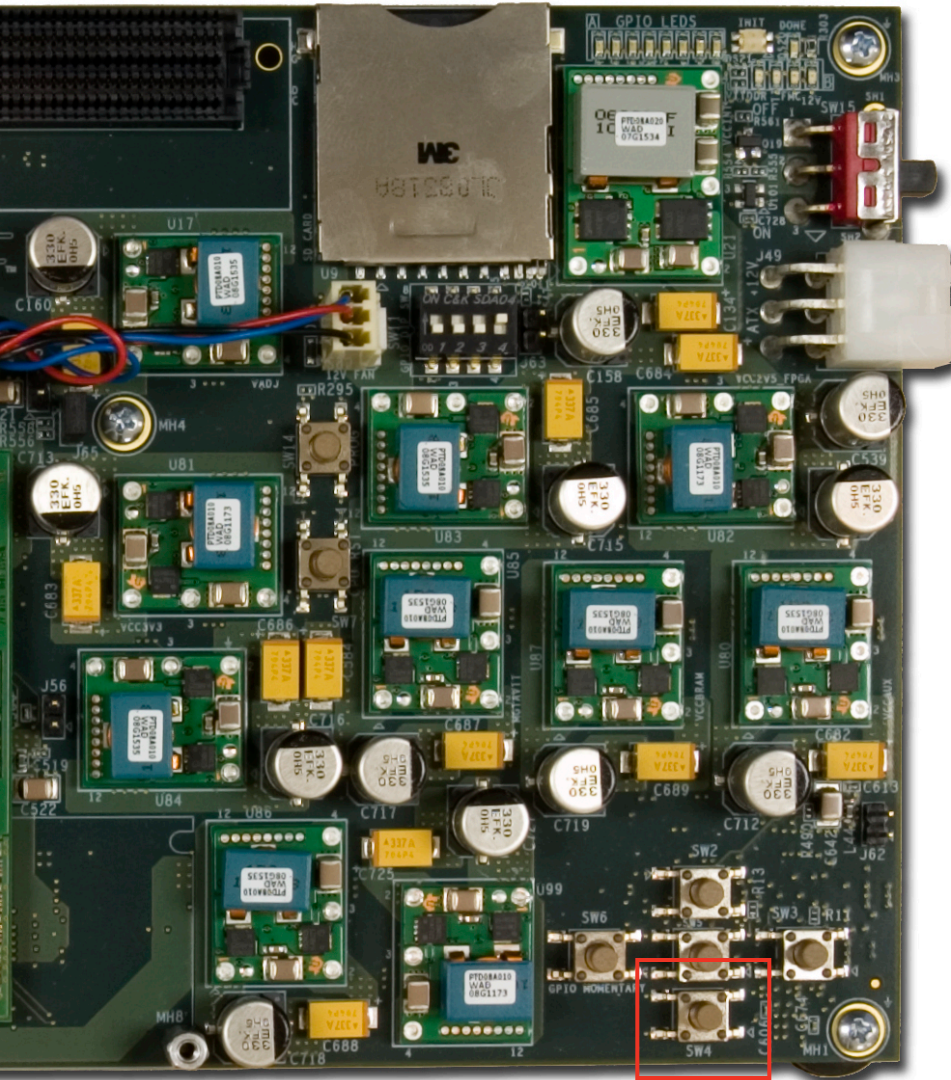
➤ Toggle the `vio_modify_enable` button to “1”



The screenshot shows the Vivado 2013.2 interface. The main window is titled "Hardware Session - localhost/xilinx_tcf/Digilent/210203337270A". The "Debug Probes" window is open, displaying a list of debug probes. The "vio_modify_enable" probe is highlighted in blue, and its value is set to "1".

Name	Value	Activity
vio_outputs		
dbg_bit[8:0]	[H] 000	
dbg_clear_error	0	
dbg_dqs[4:0]	[H] 00	
vio_addr_mode_value[2:0]	[H] 3	
vio_bl_mode_value[1:0]	[H] 0	
vio_data_mask_gen	[H] 0	
vio_data_mode_value[3:0]	[H] 7	
vio_dbg_pi_f_dec	[H] 0	
vio_dbg_pi_f_inc	[H] 0	
vio_dbg_po_f_dec	[H] 0	
vio_dbg_po_f_inc	[H] 0	
vio_dbg_po_f_stg23_sel	[H] 0	
vio_dbg_sel_pi_incdec	[H] 0	
vio_dbg_sel_po_incdec	[H] 0	
vio_fixed_bl_value[9:0]	[H] 000	
vio_fixed_instr_value[2:0]	[H] 0	
vio_instr_mode_value[3:0]	[H] 2	
vio_modify_enable	1	

Run MIG Example Design



- Press and release the CPU RESET switch, SW4, after each change to `vio_modify_enable` or `vio_data_mode_value`

Adjust Data Pattern using VIO Console

- Select the XC7K325T_0 device and click Run Trigger Immediately
- View PRBS data

The screenshot shows the Vivado 2013.2 interface. The 'Hardware' window on the left shows the device tree with 'XC7K325T_0 (2) (a...)' selected. The 'Logic Analyzer' window on the right shows the 'hw_ila_data_1.wcfg' configuration. The data table below shows the captured PRBS data.

Name	Value	630	631	632	633	634
dbg_rddata_valid	1					
dbg_rddata_r[63:0]	3972e4c99	4284091224489020	d1a2458a142...	3d7bf7eedb...	3972e4c993274f9e	
dbg_tg_compare	0					
dbg_cmp_data_val	1					
dbg_cmp_error	0					

Run trigger immediate

References

References

➤ Kintex-7 Memory

- 7 Series FPGAs Memory Interface Solutions User Guide – UG586
 - http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v2_0/ug586_7Series_MIS.pdf

➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_2/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

➤ Kintex-7

– Kintex-7 FPGA Family

- <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>

➤ KC705 Documentation

– Kintex-7 FPGA KC705 Evaluation Kit

- <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>

– KC705 Getting Started Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf

– KC705 User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf