

Spartan-3 PCIe Starter Board

Avnet Engineering Services

www.em.avnet.com/xilinx

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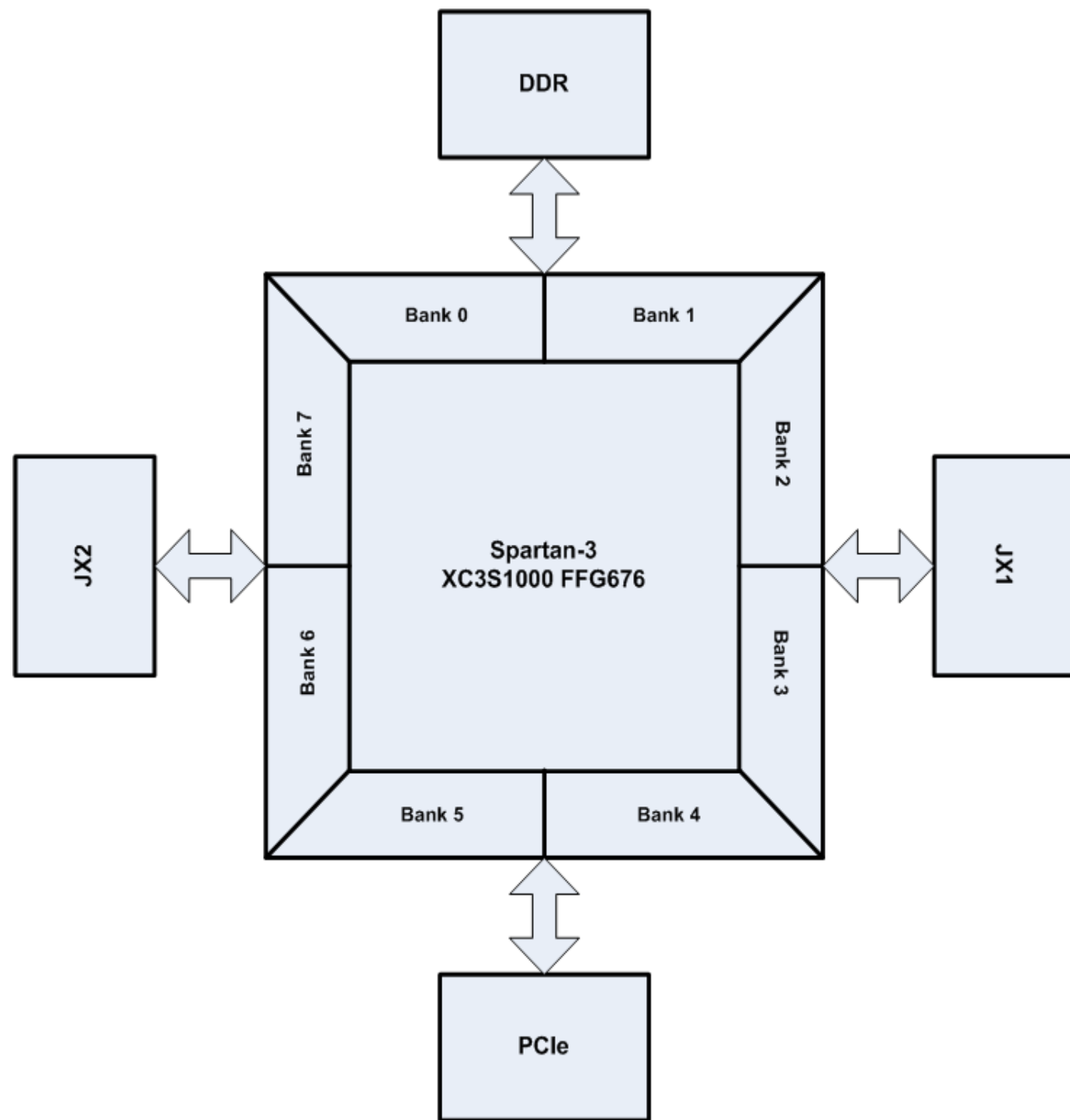
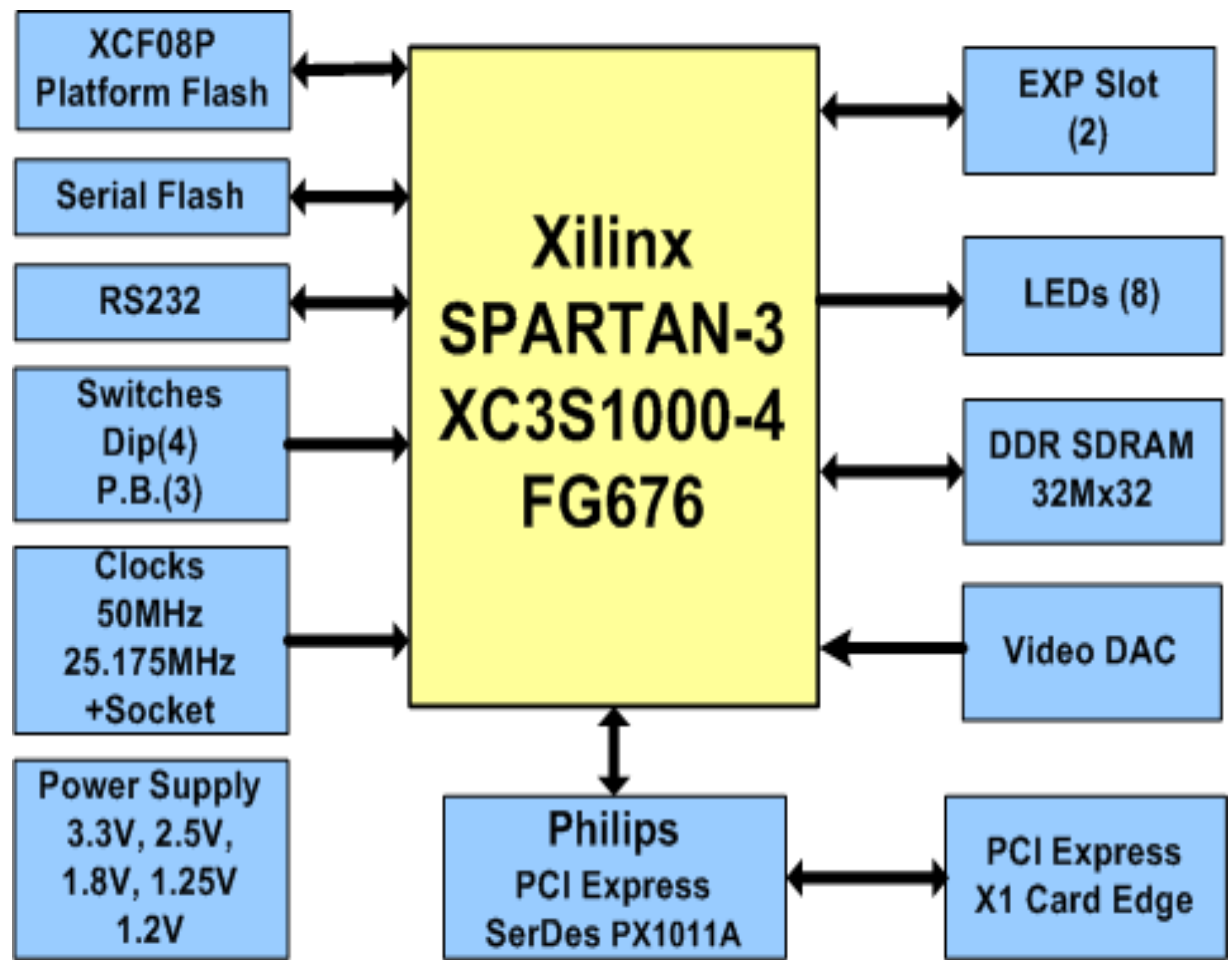
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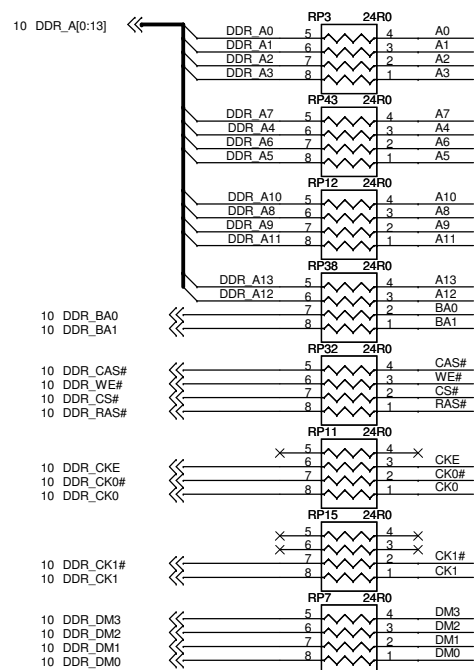
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05/03/07

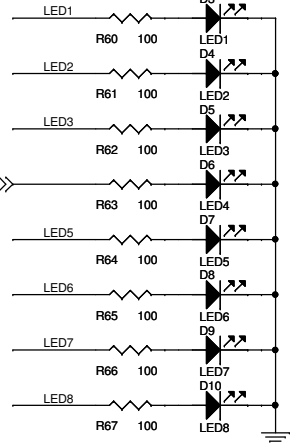
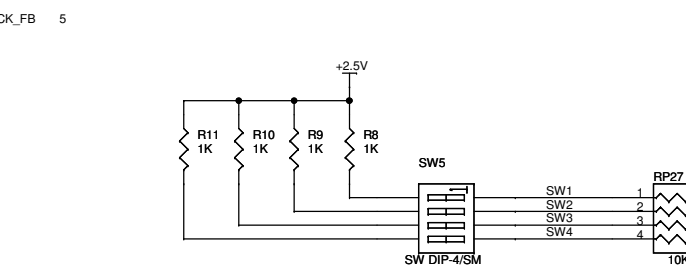
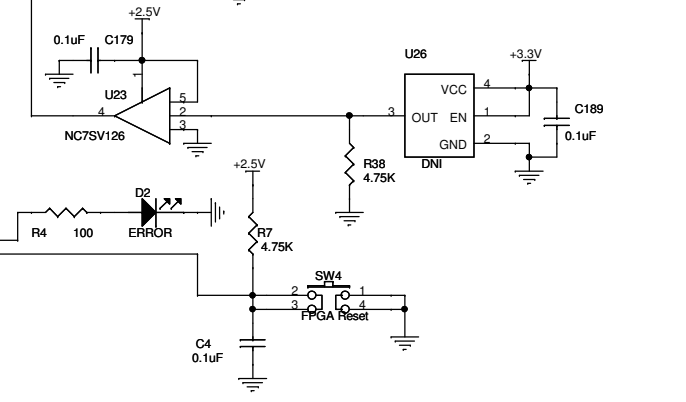
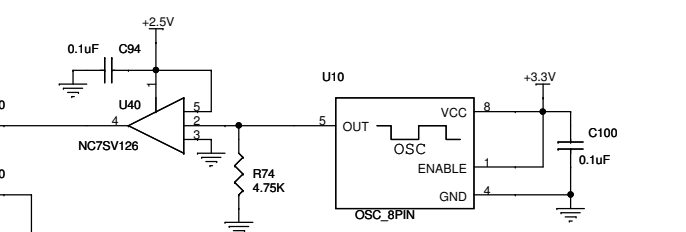
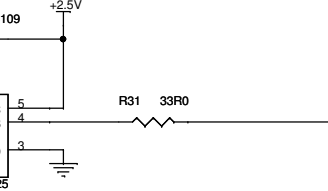
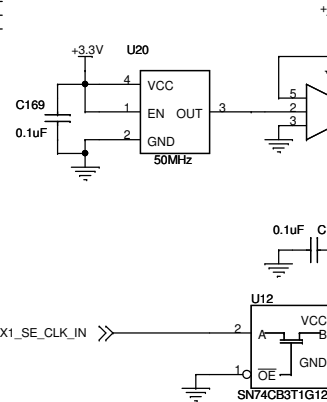
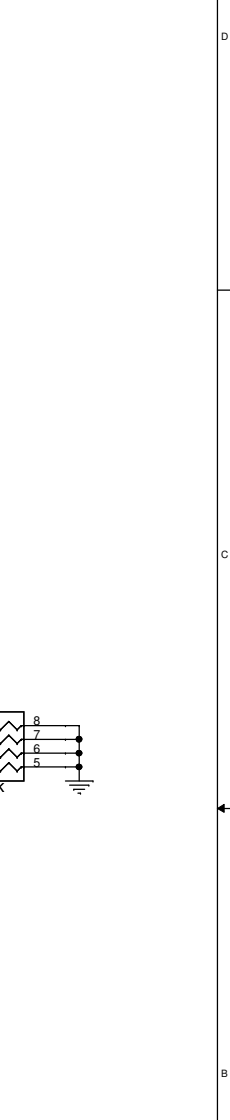
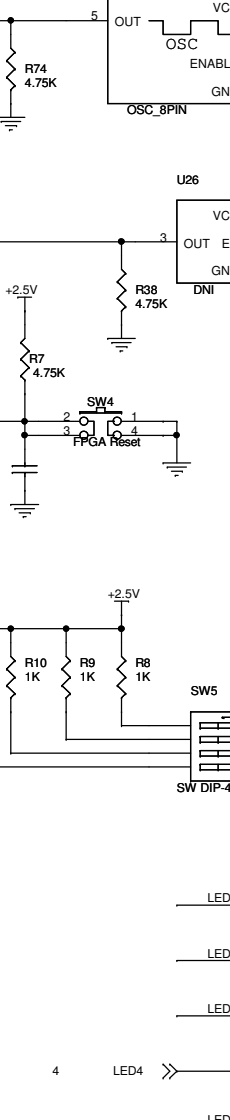
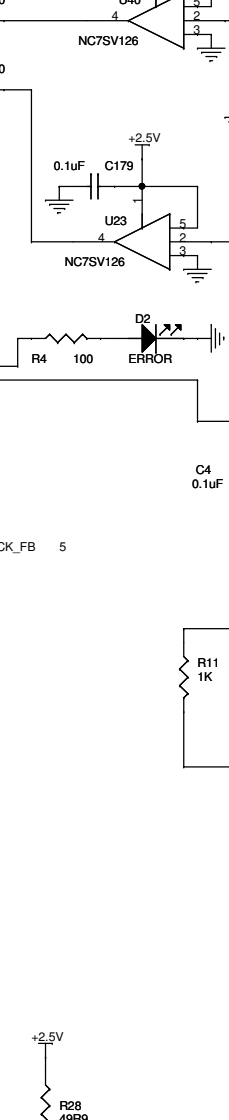
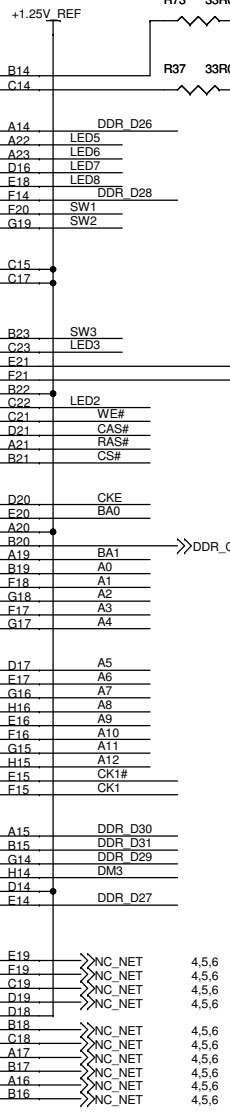
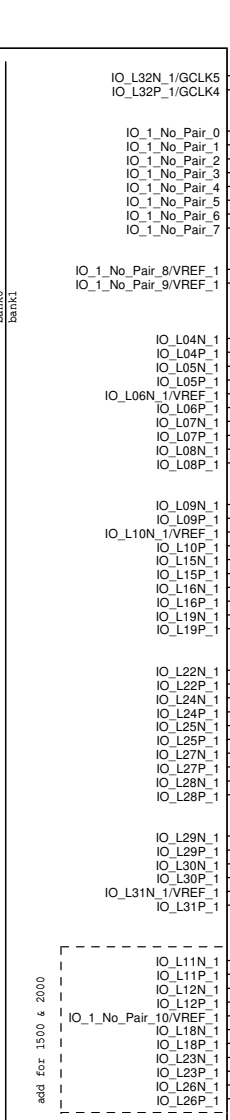
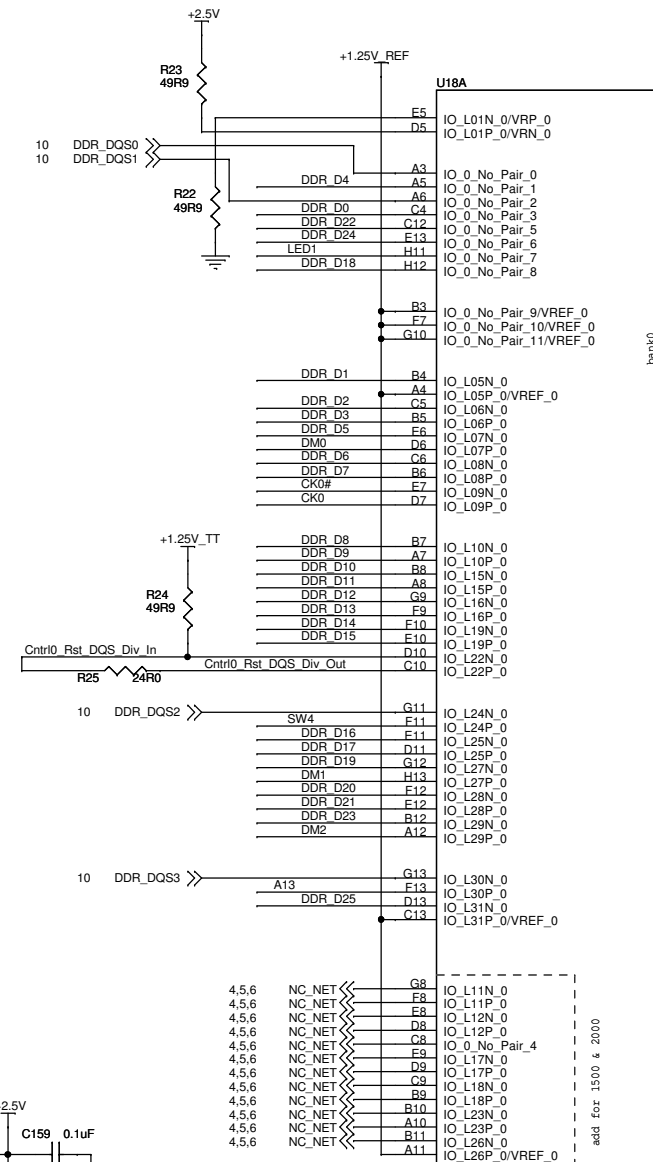
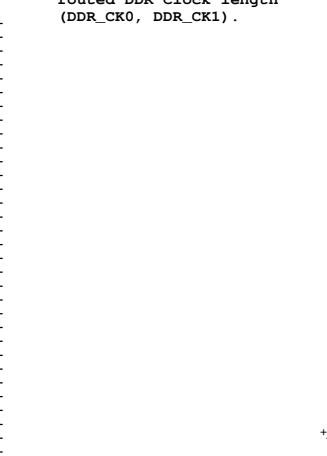
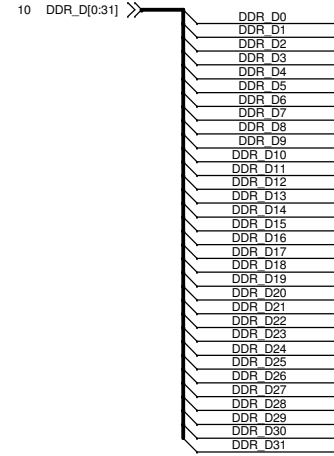
REVISION 2.1

Avnet, Inc. Engineering Services		Copyright 2006
Title	Spartan-3 PCIe Starter Board	Cover sheet
Size B	Document Number AES-SP3-PCIE-SCH	Rev 2.1
Date:	Thursday, May 03, 2007	Sheet 1 of 13

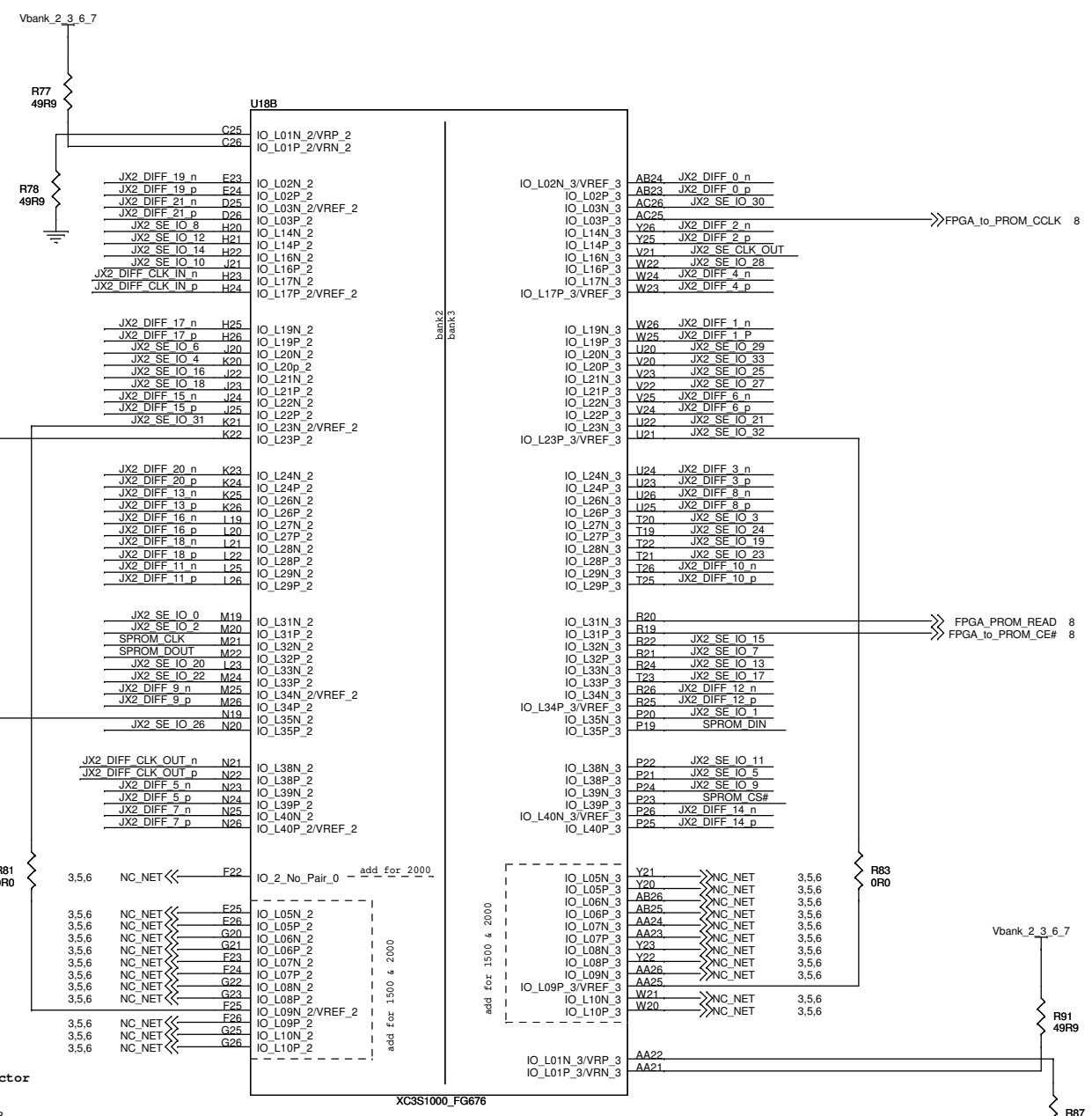
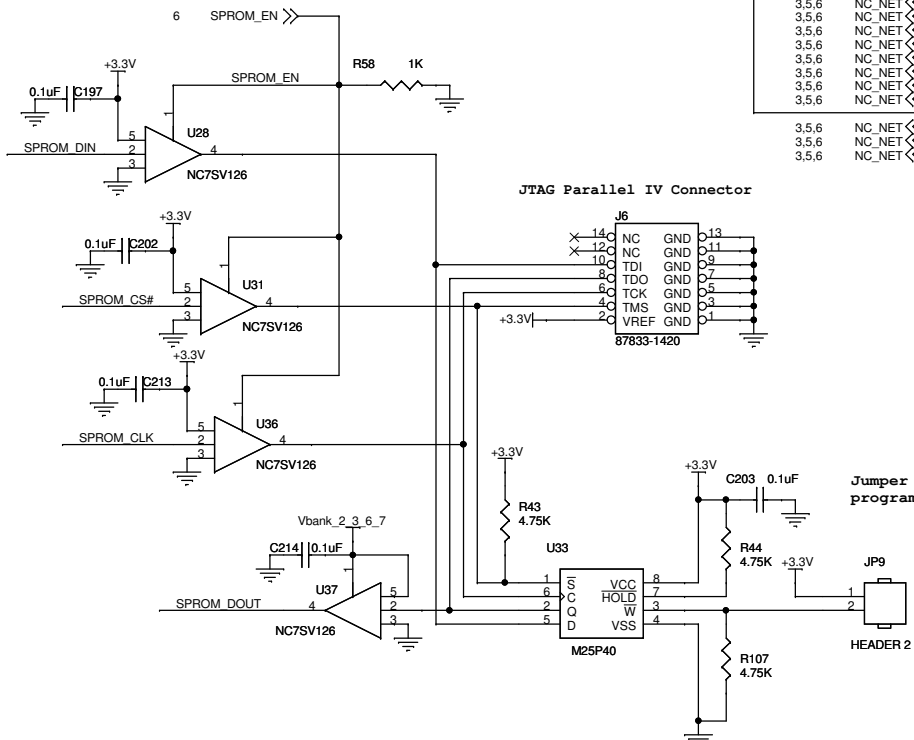
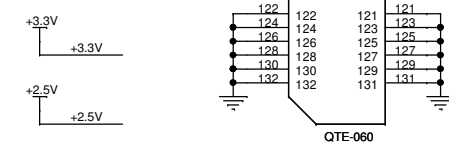


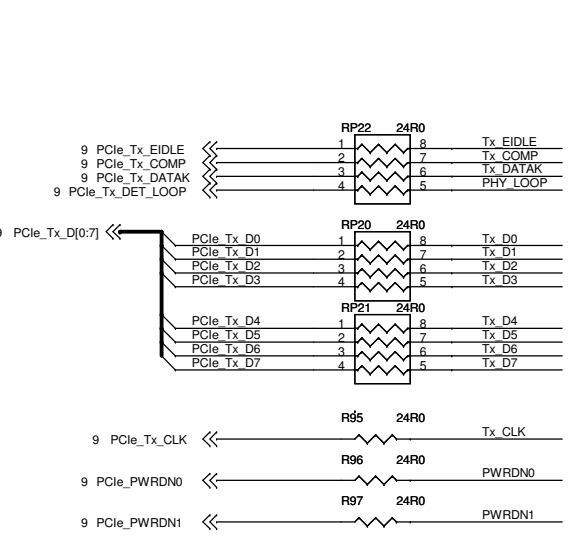


Place R25 close to U18.C10.
 Total length of U18.C10 to R25 to U18.D10 is 2X the routed DDR Clock length (DDR_CK0, DDR_CK1).

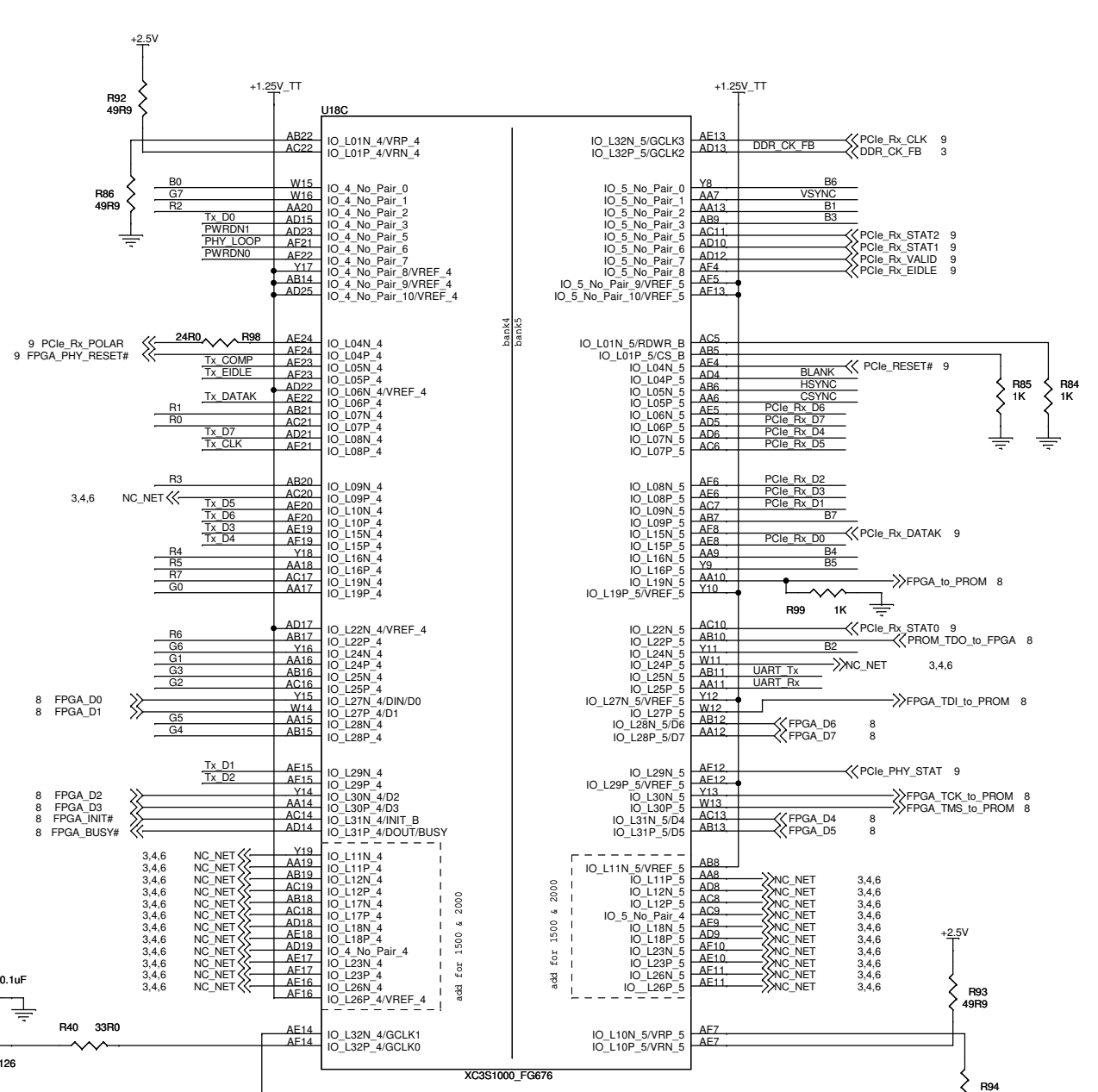
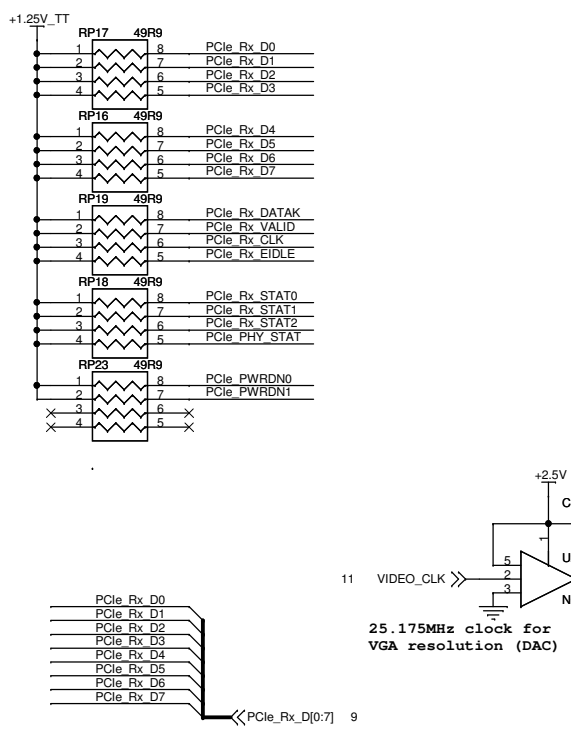


JX2	Pin	Signal	Pin	Signal
JX2 SE IO 0	2	JX2 SE IO 1	1	
JX2 SE IO 2	4	JX2 SE IO 3	3	
	6	+2.5V	5	
JX2 SE IO 4	8	JX2 SE IO 5	7	
JX2 SE IO 6	10	JX2 SE IO 7	9	
	12	+2.5V	11	
JX2 SE IO 8	14	JX2 SE IO 9	13	
JX2 SE IO 10	16	JX2 SE IO 11	15	
	18	+2.5V	17	
JX2 SE IO 12	20	JX2 SE IO 13	19	
JX2 SE IO 14	22	JX2 SE IO 15	21	
	24	+2.5V	23	
JX2 SE IO 16	26	JX2 SE IO 17	25	
JX2 SE IO 18	28	JX2 SE IO 19	27	
	30	+2.5V	29	
JX2 SE IO 20	32	JX2 SE IO 21	31	
JX2 SE IO 22	34	JX2 SE IO 23	33	
	36	+2.5V	35	
JX2 SE IO 24	38	JX2 SE IO 25	37	
JX2 SE IO 26	40	JX2 SE IO 27	39	
	42	JX2 SE IO 28	41	
JX2 DIFF CLK IN p	44	JX2 SE IO 29	43	
JX2 DIFF CLK IN n	46	GND POWER	45	JX2 SE_CLK_IN 5
GND POWER	48	JX2 SE IO 30	47	
JX2 SE IO 31	50	JX2 SE CLK OUT	49	
GND POWER	52	GND POWER	51	
JX2 DIFF 20 p	54	JX2 DIFF 21 p	53	
JX2 DIFF 20 n	56	JX2 DIFF 21 n	55	
GND POWER	58	GND POWER	57	
JX2 DIFF 18 p	60	JX2 SE IO 32	59	
JX2 DIFF 18 n	62	JX2 SE IO 33	61	
GND POWER	64	GND POWER	63	
JX2 DIFF 16 p	66	JX2 DIFF 19 p	65	
JX2 DIFF 16 n	68	JX2 DIFF 19 n	67	
GND POWER	70	GND POWER	69	
JX2 DIFF CLK OUT p	72	JX2 DIFF 17 p	71	
JX2 DIFF CLK OUT n	74	JX2 DIFF 17 n	73	
GND POWER	76	GND POWER	75	
JX2 DIFF 14 p	78	JX2 DIFF 15 p	77	
JX2 DIFF 14 n	80	JX2 DIFF 15 n	79	
	82	JX2 DIFF 13 p	81	
JX2 DIFF 12 p	84	JX2 DIFF 13 n	83	
	86	+3.3V	85	
JX2 DIFF 10 p	88	JX2 DIFF 11 p	87	
JX2 DIFF 10 n	90	JX2 DIFF 11 n	89	
	92	+3.3V	91	
JX2 DIFF 8 p	94	JX2 DIFF 9 p	93	
JX2 DIFF 8 n	96	JX2 DIFF 9 n	95	
	98	+3.3V	97	
JX2 DIFF 6 p	100	JX2 DIFF 7 p	99	
JX2 DIFF 6 n	102	JX2 DIFF 7 n	101	
	104	+3.3V	103	
JX2 DIFF 4 p	106	JX2 DIFF 5 p	105	
JX2 DIFF 4 n	108	JX2 DIFF 5 n	107	
	110	+3.3V	109	
JX2 DIFF 2 p	112	JX2 DIFF 3 p	111	
JX2 DIFF 2 n	114	JX2 DIFF 3 n	113	
	116	+3.3V	115	
JX2 DIFF 0 p	118	JX2 DIFF 1 p	117	
JX2 DIFF 0 n	120	JX2 DIFF 1 n	119	

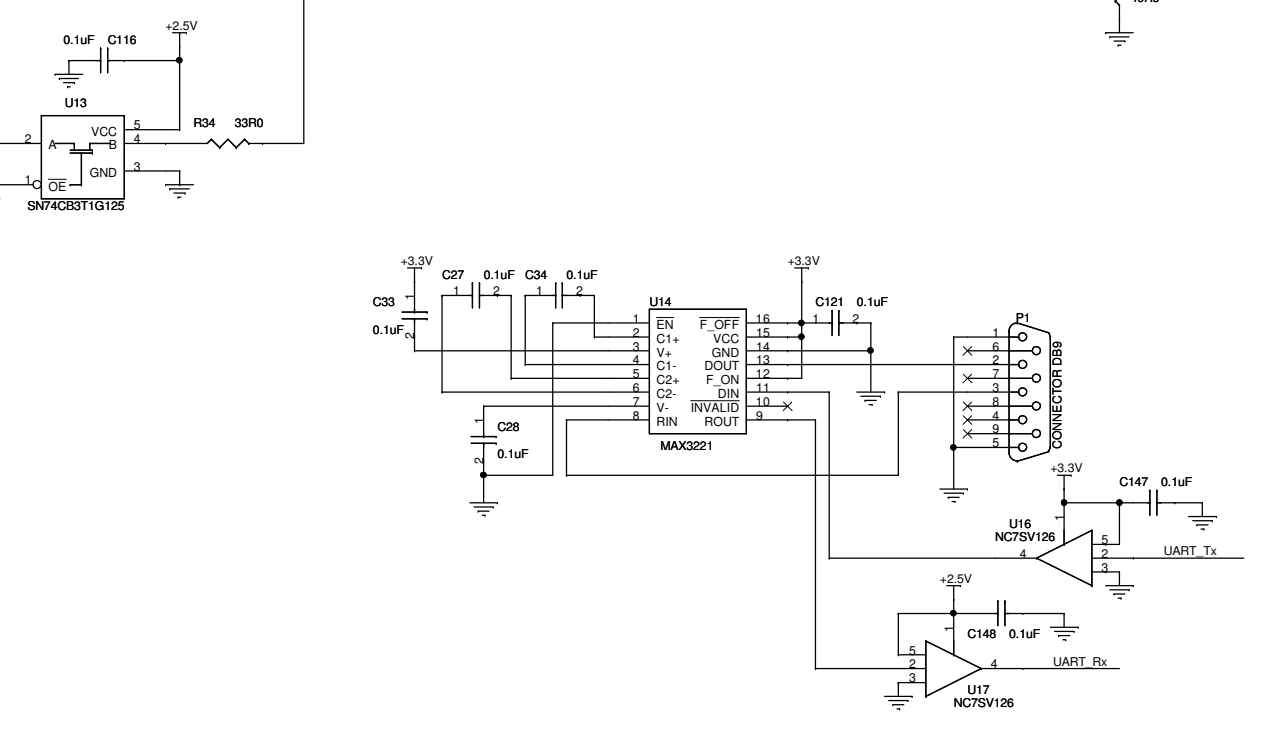
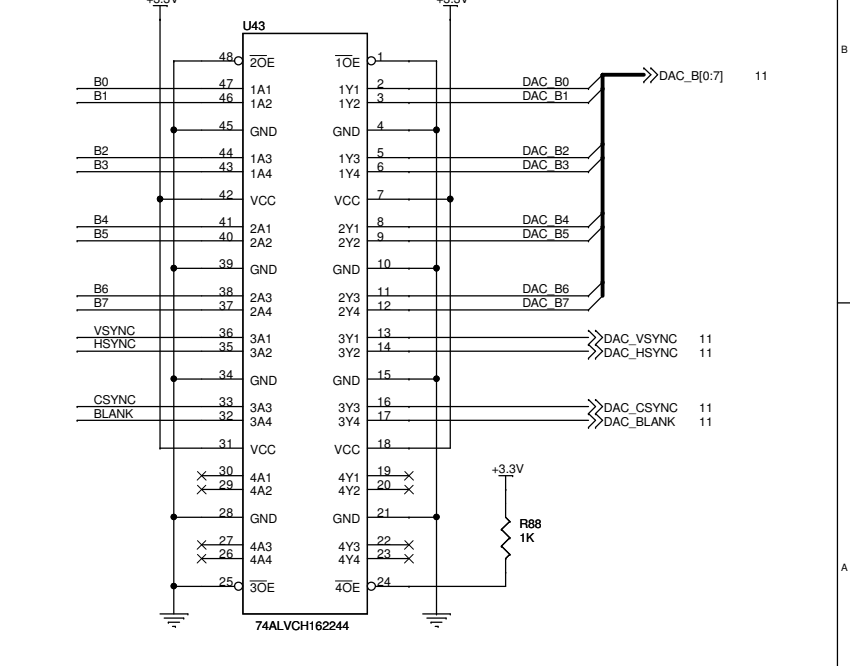
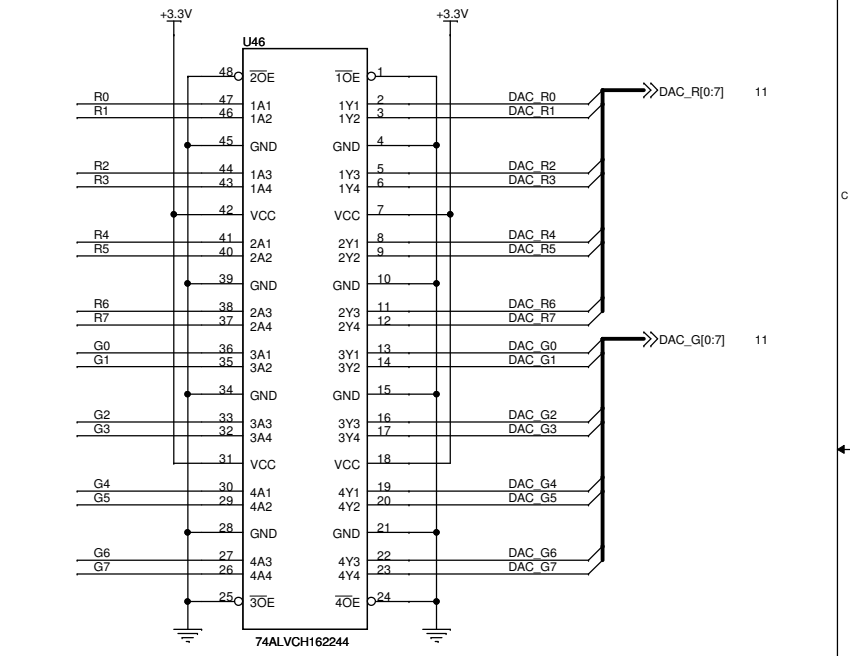
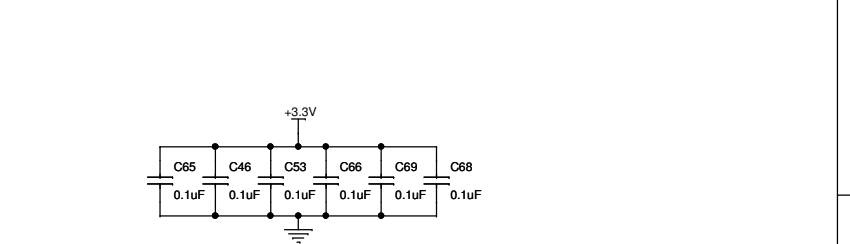


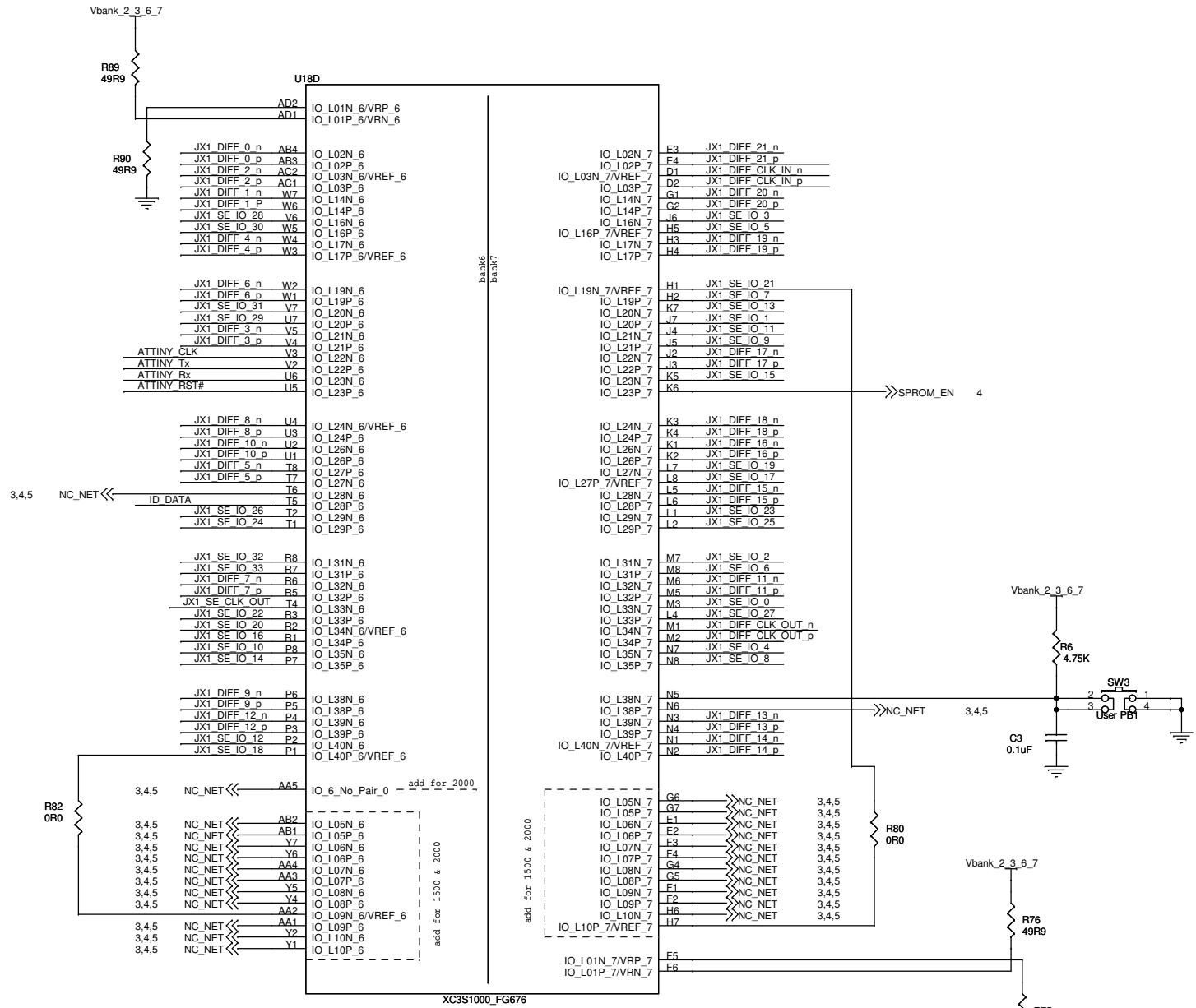
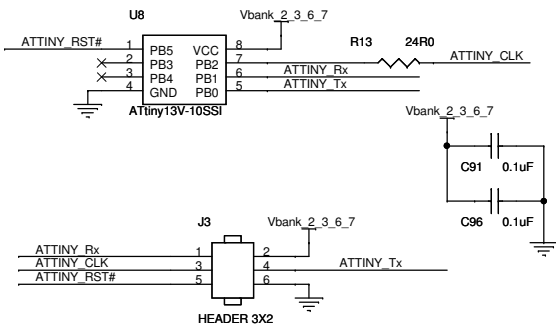
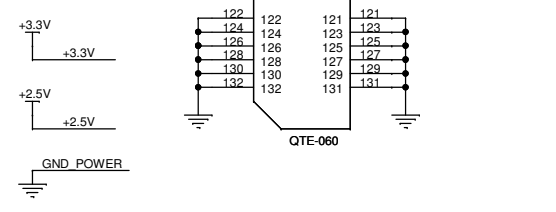
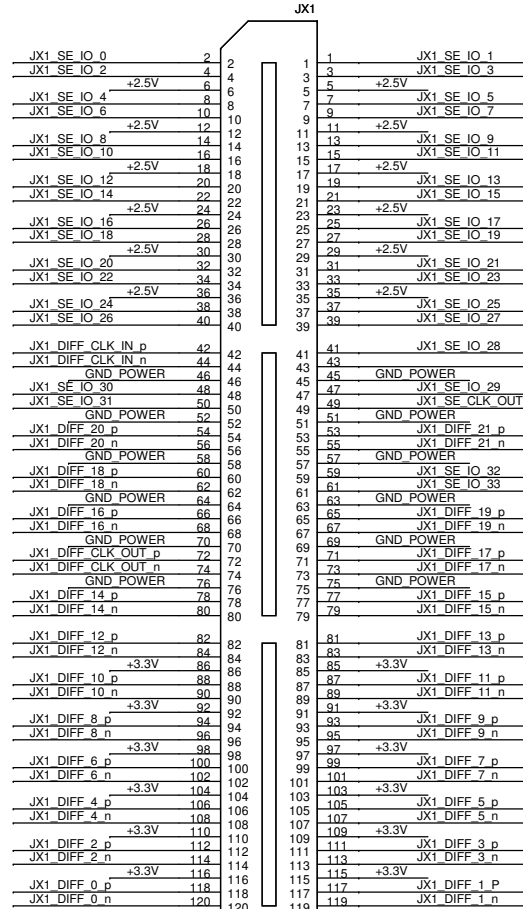


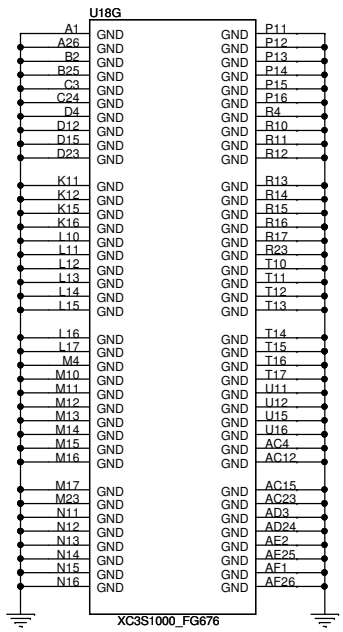
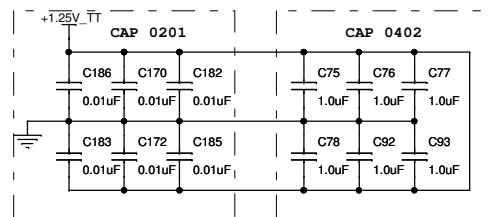
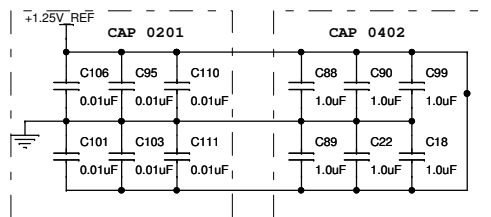
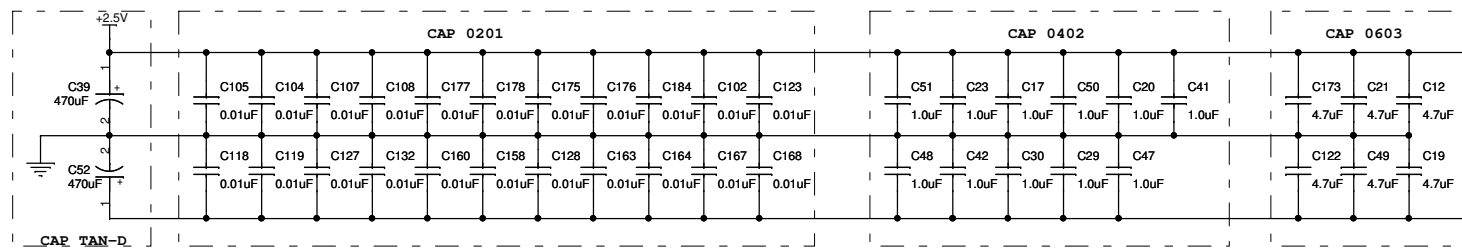
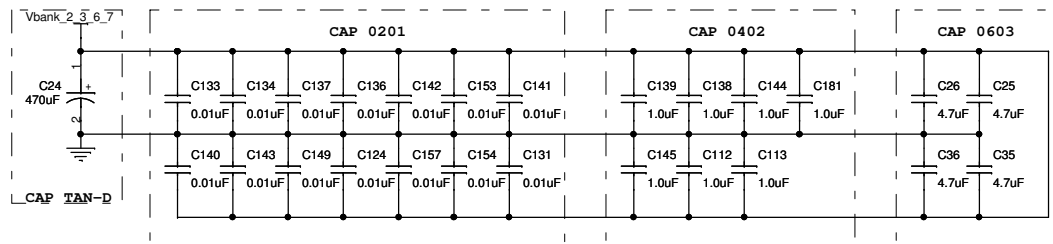
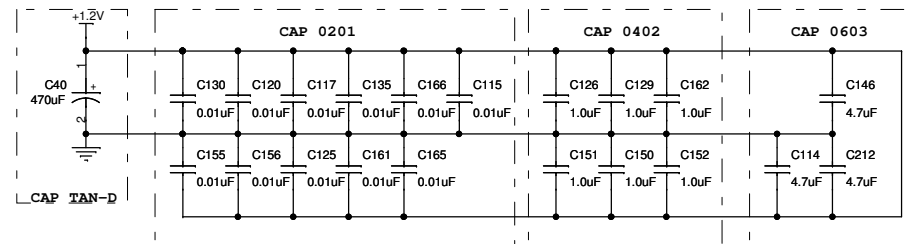
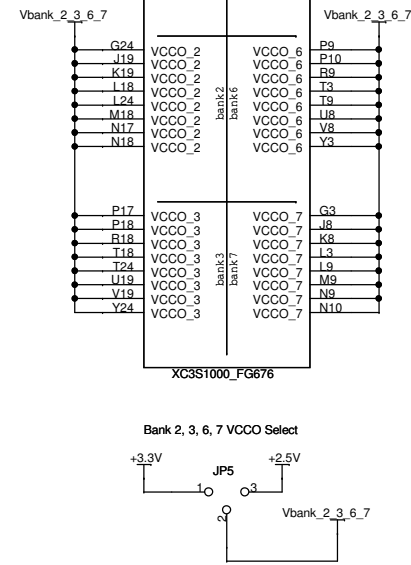
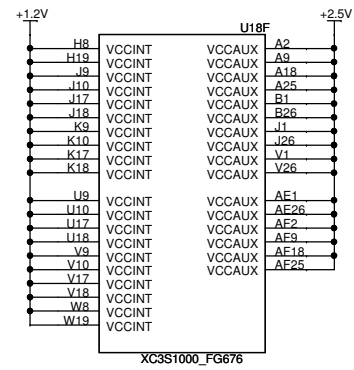
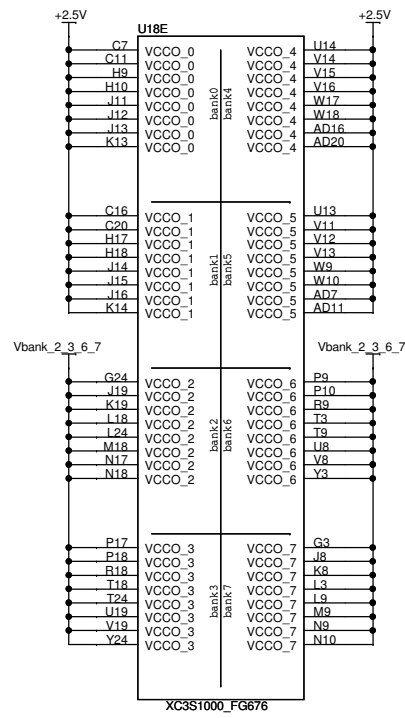
Place RP16 - RP23, R95 - R97 close to U18

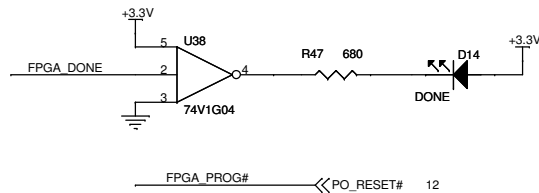
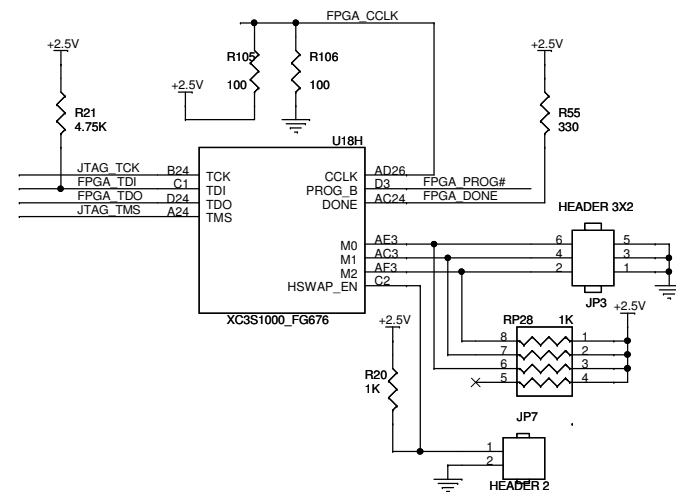
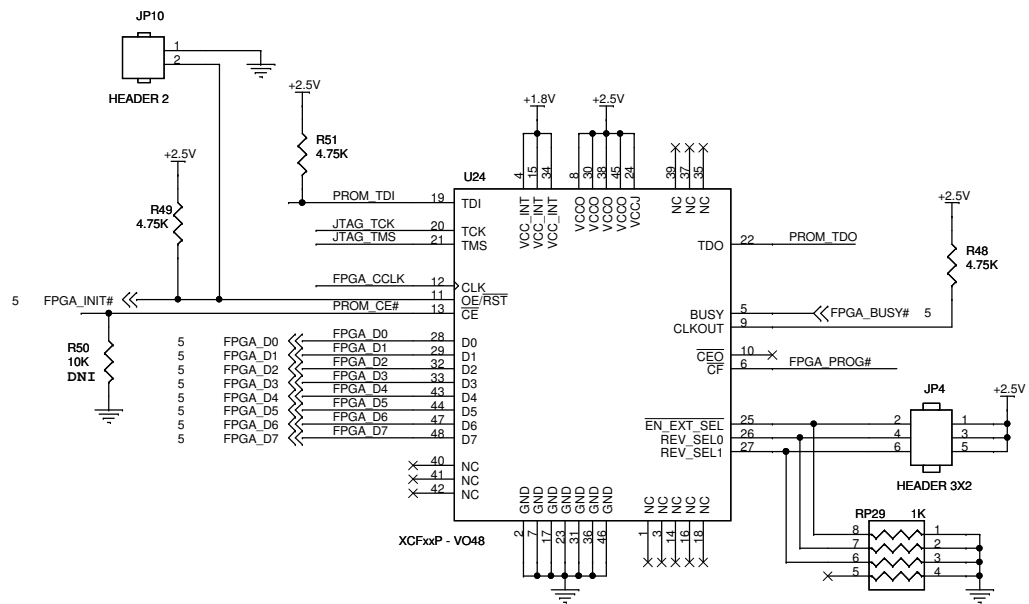


Match lengths of DDR traces, except DDR_CLK_FB make 2X the length



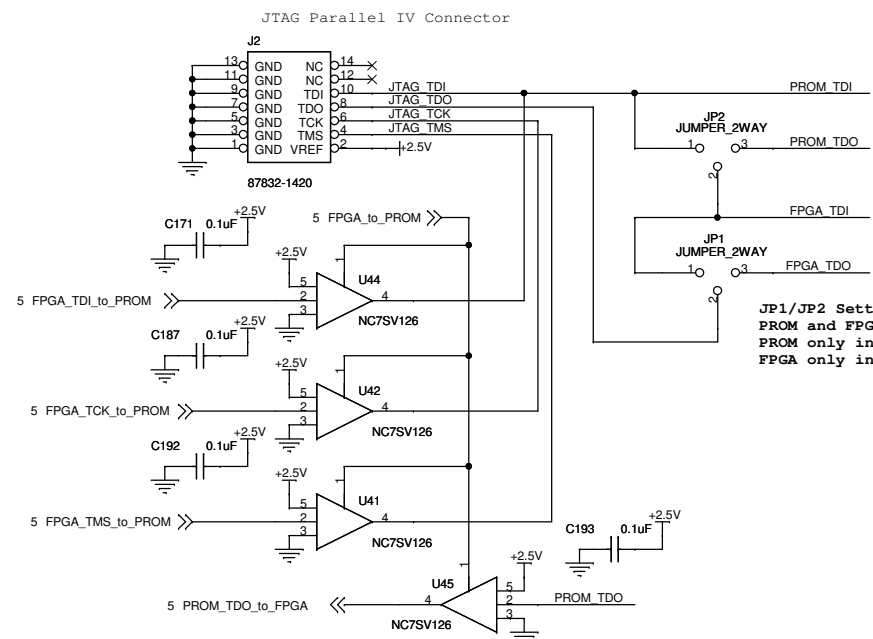
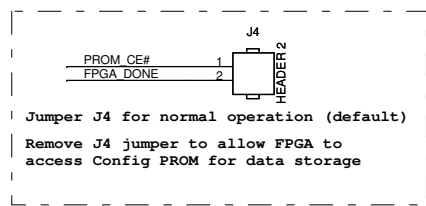
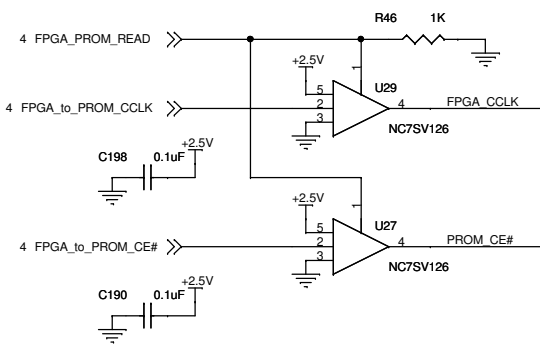




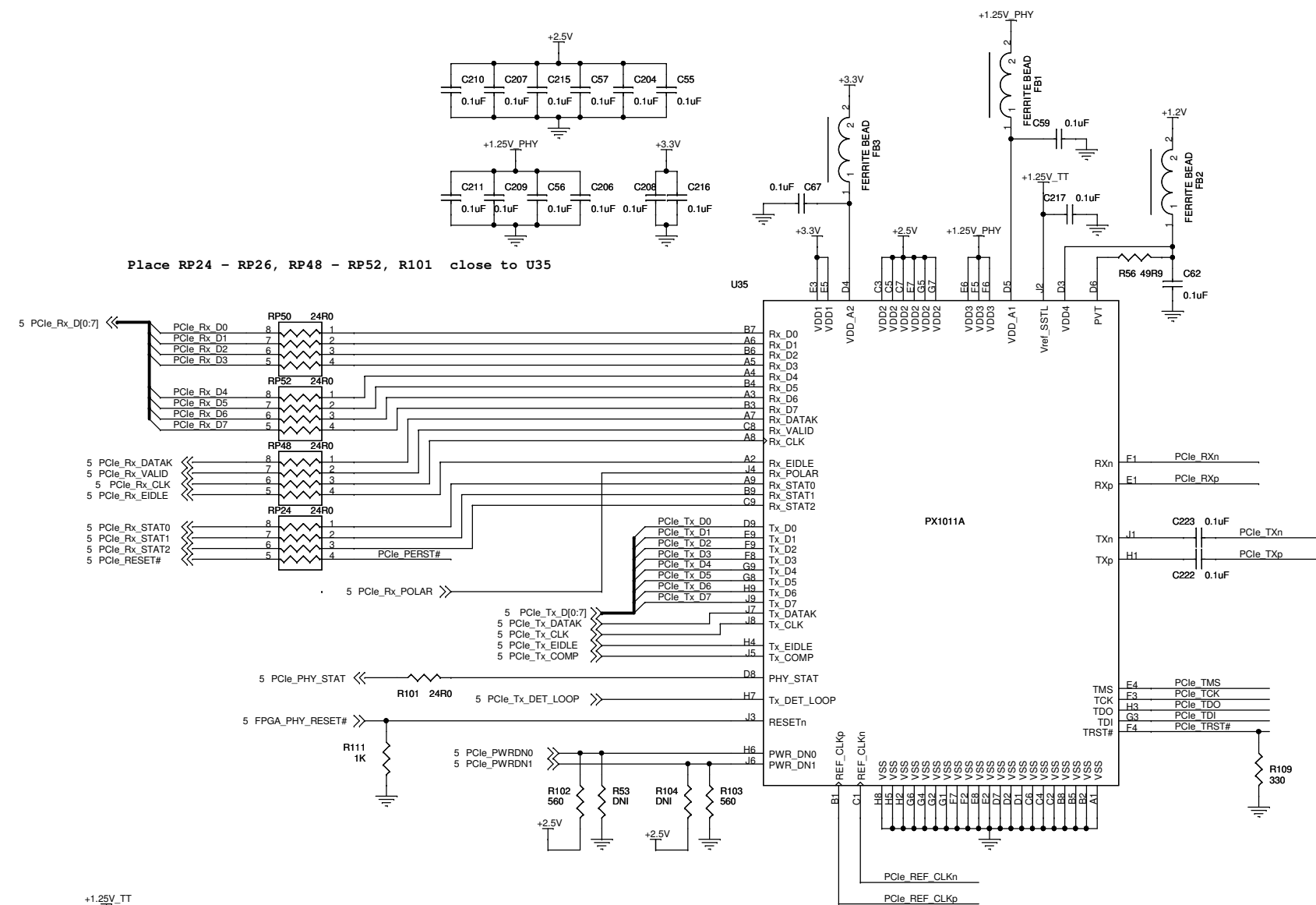


Configuration Mode	M0 (JP3 5:6)	M1 (JP3 3:4)	M2 (JP3 1:2)
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	1	1	0
Slave Parallel	0	1	1
JTAG	1	0	1

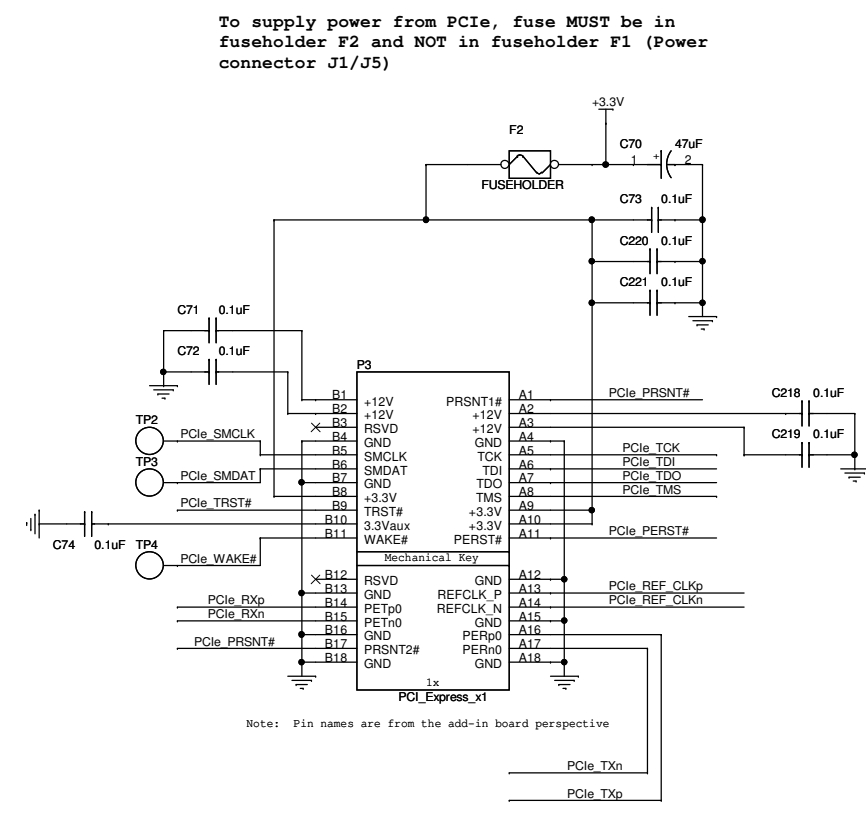
Note: With no shunts installed on JP3, M0 = M1 = M2 = 1 via RP28



JP1/JP2 Settings:
 PROM and FPGA in chain - JP2 2:3, JP1 2:3
 PROM only in chain - JP2 2:3, JP1 1:2
 FPGA only in chain - JP2 1:2, JP1 2:3

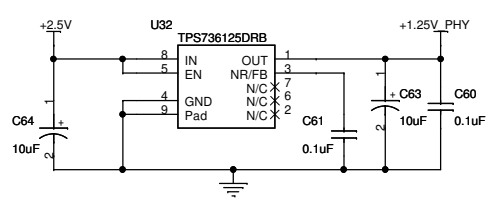
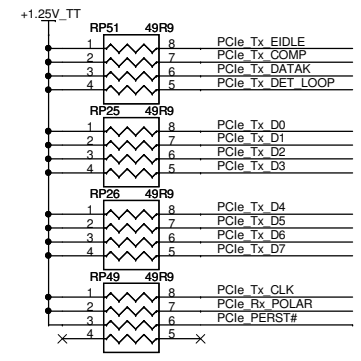


Place RP24 - RP26, RP48 - RP52, R101 close to U35

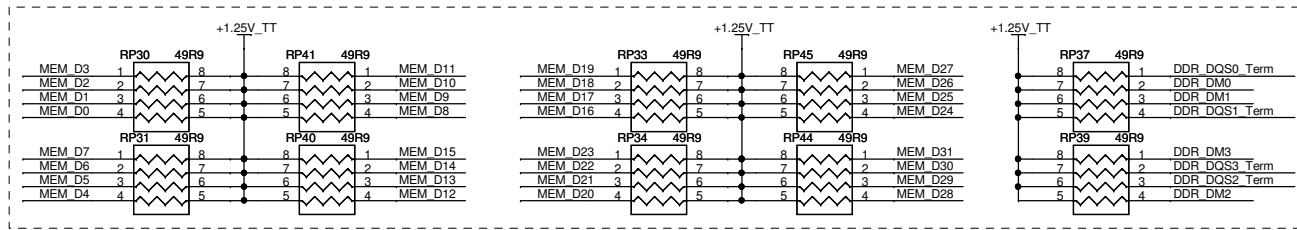


To supply power from PCIe, fuse MUST be in fuseholder F2 and NOT in fuseholder F1 (Power connector J1/J5)

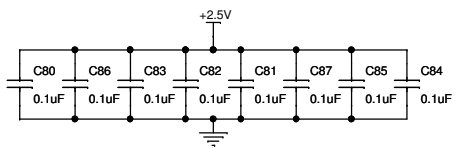
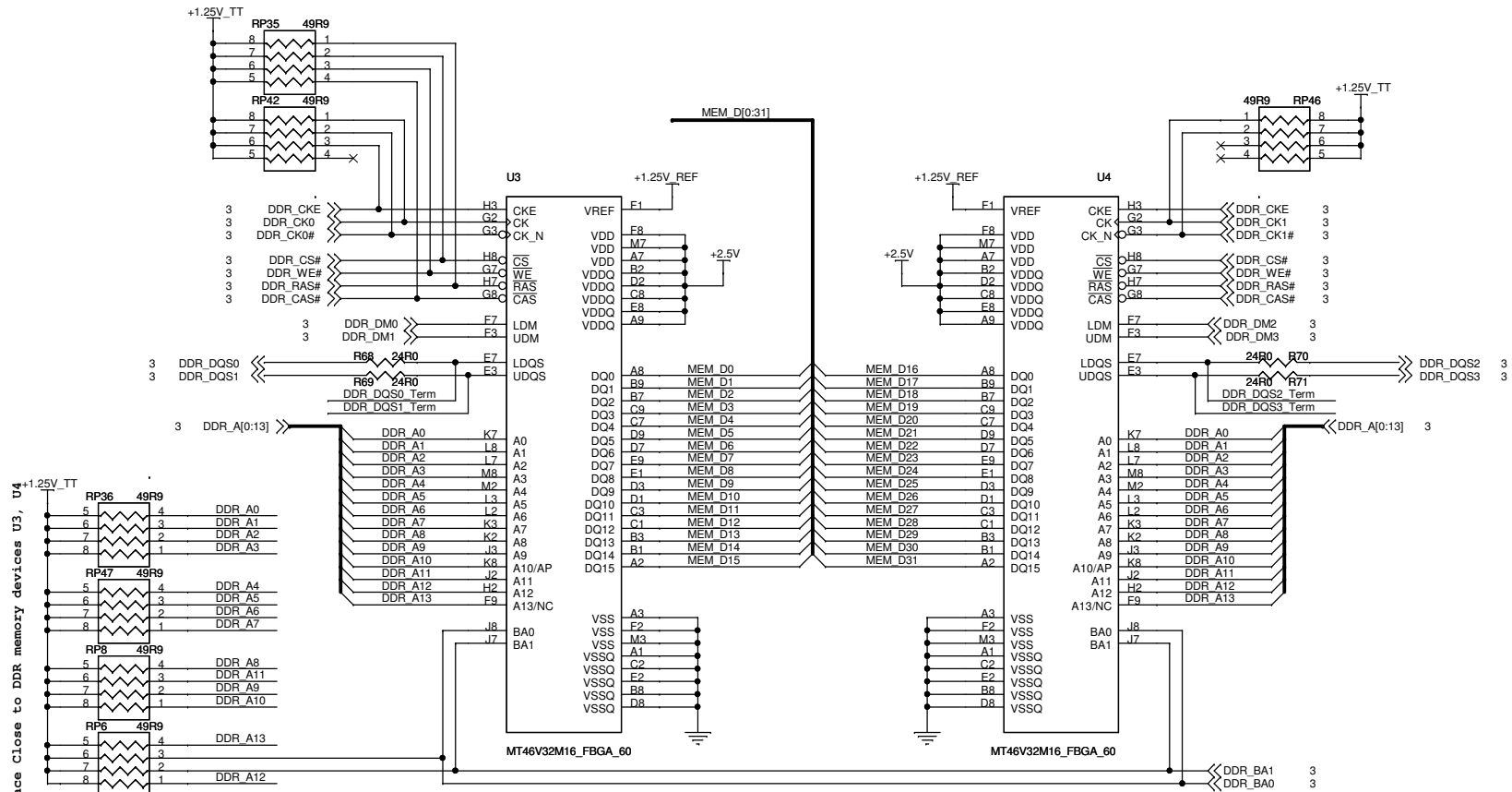
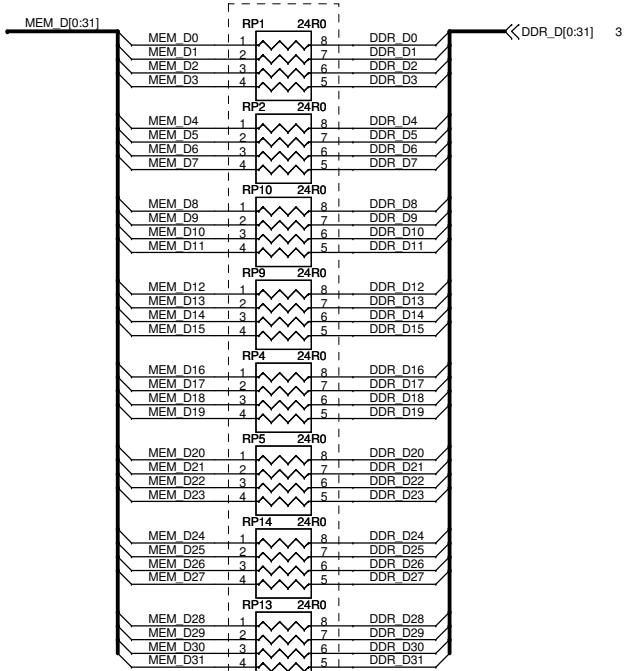
Note: Pin names are from the add-in board perspective



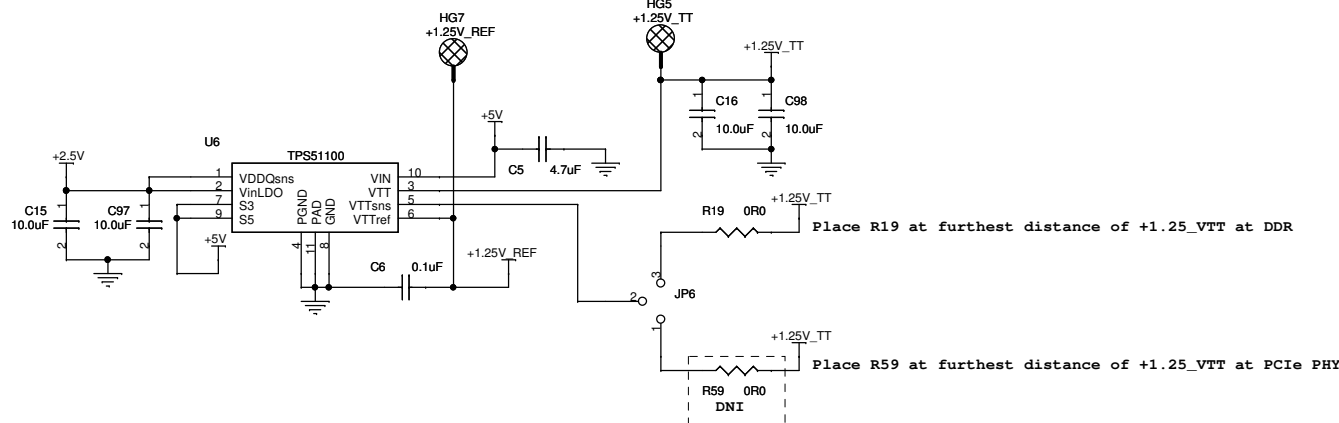
Install Terminators on Far Side of DDR memory devices U3 and U4

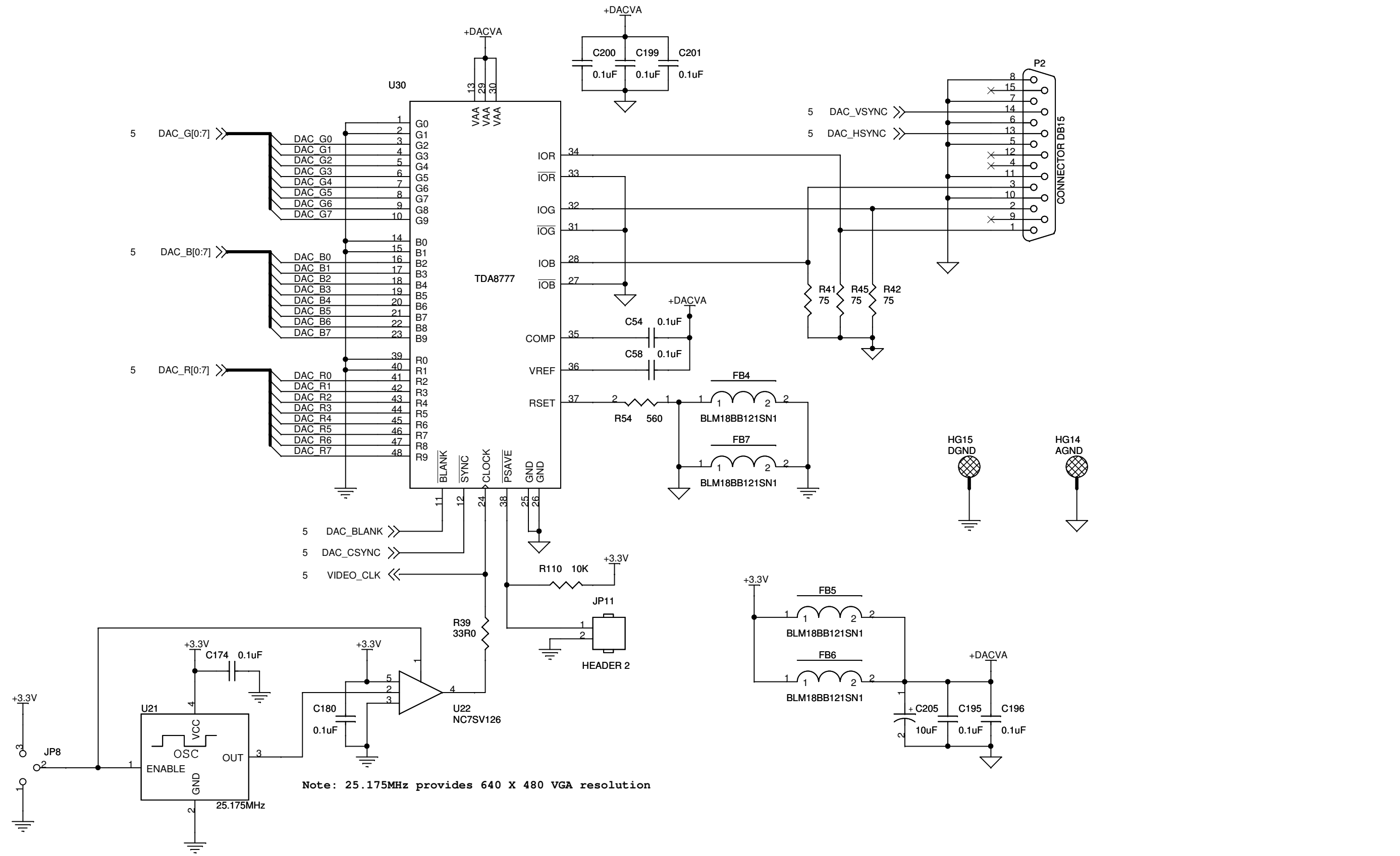


Place Close to DDR memory devices U3 and U4



DDR Termination Voltage





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Title		Spartan-3 PCIe Starter Board Video DAC
Size	Document Number	Rev
B	AES-SP3-PCIE-SCH	2.1
Date:	Thursday, May 03, 2007	Sheet 11 of 13

Changes Rev1 to Rev2:

3/27/06 - Swapped power and ground connections to power switch SW6 to match PCB silk-screen (up = ON)

Clarification:

5/02/07 - Changed names of pin pairs B14/B15 and A16/A17 on PCIe connector P3 to match PCIe CEM Spec.

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Title		Spartan-3 PCIe Starter Board Revision Notes
Size A	Document Number AES-SP3-PCIE-SCH	Rev 2.1
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