

## Introduction

The flip-flop logic is designed to be used with Platform Studio to perform simple logical operations. A Microprocessor Peripheral Definition (MPD) file associated with this module is also included. Users can utilize Xilinx Platform Studio (XPS) to incorporate this module into the Microprocessor Hardware Specification (MHS) file.

This flip-flop logic can serve as glue logic among peripherals. This module is not associated with any system bus.

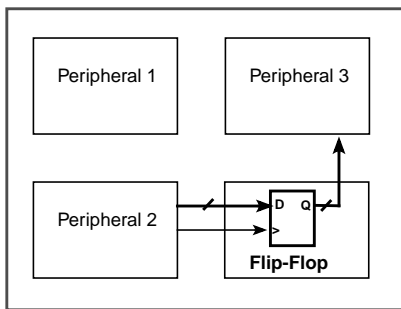


Figure 1: Flip-Flop Logic as Glue Logic in a System

## Features

The flip-flop logic has the following features:

- Configurable size of the vectors
- Supports "synchronous set & clear" or "asynchronous reset & preset"
- Supports optional clock enable

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-4™, Virtex-II Pro™, Virtex™, Virtex-E, Virtex II™, Spartan™ 2, Spartan 2E, Spartan 3	
Version of Core	util_flipflop	v1.00a
Resources Used		
	Min	Max
Slices	1	Variable <sup>1</sup>
LUTs	0	0
FFs	1	Variable <sup>1</sup>
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

1. The number of slices and flip flops depends on the value of C\_SIZE.

## Implementation

### I/O Summary

Table 1: Summary of Flip-Flop I/O

Signal	Interface	I/O	Description
Clk	None	I	Clock signal
Rst	None	I	<p>When asynchronous<sup>1</sup> style is selected (C_USE_ASYNCH=1), this signal is connected as the "reset" signal.</p> <p>When synchronous style is selected (C_USE_ASYNCH=0), this signal is connected as the "clear" signal.</p> <p>This signal has no effect when C_USE_RST = 0.</p>
Set	None	I	<p>When asynchronous style is selected (C_USE_ASYNCH=1), this signal is connected as the "preset" signal.</p> <p>When synchronous style is selected (C_USE_ASYNCH=0), this signal is connected as the "set" signal.</p> <p>This signal has no effect when C_USE_SET = 0.</p>
CE	None	I	<p>Clock enable.</p> <p>This signal has no effect when C_USE_CE = 0.</p>
D	None	I	Input data bus to the flip-flop. Bus width is defined by the parameter C_SIZE.
Q	None	O	Output data bus from the flip-flop. Bus width is defined by the parameter C_SIZE.

1. For more information, please visit <http://support.xilinx.com> for the "Libraries Guide" under Xilinx Software Manuals.

## MPD File Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral's parameters that are fixed at FPGA configuration time. The parameters are described in the following table.

Table 2: MPD Parameters

Parameter	Description	Type
C_USE_RST	When C_USE_RST=1, the input signal "Rst" is connected as the "reset" or "clear" signal of the flipflop depending on the value of C_USE_ASYNCH. When C_USE_RST=0, the input signal "Rst" is not used.	integer
C_USE_SET	When C_USE_SET=1, the input signal "Set" is connected as the "preset" or "set" signal of the flipflop, depending on the value of C_USE_ASYNCH. When C_USE_SET=0, the input signal "Set" is not used.	integer
C_USE_CE	When C_USE_CE = 1, the input signal "CE" is connected as the "CE" (clock enable) of the flipflop. When C_USE_CE = 0, the input signal CE is not used.	integer
C_USE_ASYNCH	When C_USE_ASYNCH = 1, the FDCPE (D Flip-Flop with Clock Enable and Asynchronous Preset and Clear) is inferred. When C_USE_ASYNCH = 0, the FDRSE (D Flip-Flop with Clock Enable and Synchronous Reset and Set) is inferred.	integer
C_SIZE	The size of the vectors. Notice that the width of D and Q must be equal. The minimum value of this parameter is 1.	integer

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.