

## Introduction

The Reduced Logic module is designed to be used with Platform Studio to perform simple logical operations. A Microprocessor Peripheral Definition (MPD) file associated with this module is also included. Users can utilize Xilinx Platform Studio (XPS) to incorporate this module into the Microprocessor Hardware Specification (MHS) file.

This reduced logic takes one input vector, performs a reduced logic operation and generates a single bit result. This module can serve as glue logic among peripherals. This module is not associated with any system bus.

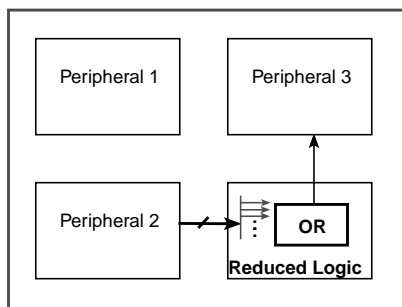


Figure 1: Reduced Logic Operation as Glue Logic in a System

## Features

The Reduced Logic has the following features:

- Configurable size of the input vector
- Configurable reduced logic operation on an input vector

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-4™, Virtex-II Pro™, Virtex™, Virtex-E, Virtex II™, Spartan™ 2, Spartan 2E, Spartan 3	
Version of Core	util_reduced_logic	v1.00a
Resources Used		
	Min	Max
Slices	1	Variable <sup>1</sup>
LUTs	1	Variable <sup>1</sup>
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

1. The number of slices and LUTs depends on C\_SIZE.

## Reduced Logic Operation

Given selected input vector size, this module supports the following operations:

- Reduced AND
- Reduced OR
- Reduced XOR

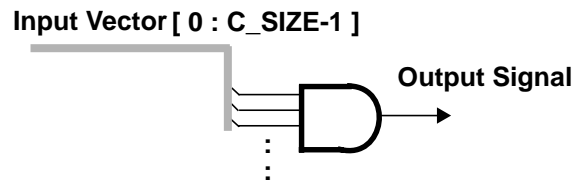


Figure 2: Reduced Logic Operation

## Implementation

### I/O Summary

Table 1: Summary of Reduced Logic I/O

Signal	Interface	I/O	Description
Op1	None	I	Input bus [ 0 : C_SIZE-1 ]
Res	None	O	One bit output signal. Result from the reduced logic operation.

### MPD File Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral's parameters that are fixed at FPGA configuration time. The parameters are described in the following table.

Table 2: MPD Parameters

Parameter	Description	Type
C_SIZE	The vector size of input bus. Minimum value is 2.	integer
C_OPERATION	The vector operation to perform. The supported operations are: "and", "or", "xor"	string

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## Revision History

The following table shows the revision history for this document.

<b>Date</b>	<b>Version</b>	<b>Revision</b>
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.