

Introduction

The Vector Logic in the EDK Infrastructure Library is designed to be used with Platform Studio to perform simple logical operations. A Microprocessor Peripheral Definition (MPD) file associated with this module is also included. Users can utilize Xilinx Platform Studio (XPS) to incorporate this module into the Microprocessor Hardware Specification (MHS) file.

This vector logic takes operands to generate a result with the selected operation. It performs the configured operation on each of the matching bits in the two input vectors to create an output vector, or on a single input vector in the case of the NOT operation. This vector logic can serve as glue logic among peripherals. This module is not associated to any system bus.

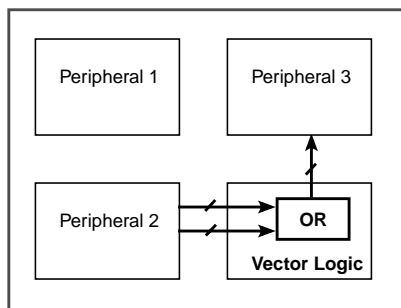


Figure 1: Vector Logic as Glue Logic in a System

Features

The vector logic has the following features:

- Configurable size of the vectors
- Configurable logical operation on vectors.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-4™, Virtex-II Pro™, Virtex™, Virtex-E, Virtex II™, Spartan™ 2, Spartan 2E, Spartan 3	
Version of Core	util_vector_logic	v1.00a
Resources Used		
	Min	Max
Slices	1	Variable ¹
LUTs	1	Variable ¹
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

1. The number of slices and LUTs depends on C_SIZE, where C_SIZE is the number of LUTs.

Vector Logic Operation

Given selected vector size and two operands (Op1 and Op2) the Vector Logic supports the following operations:

- AND
- OR
- XOR
- NOT, will only use the first operand (Op1)

Input Vector(s) Output Vector

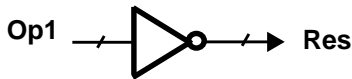


Figure 2: Vector Logic Operations

Implementation

I/O Summary

Table 1: Summary of vector logic I/O

Signal	Interface	I/O	Description
Op1	None	I	Operand 1 vector [0 : C_SIZE-1]
Op2	None	I	Operand 2 vector [0 : C_SIZE-1]
Res	None	O	Result vector [0 : C_SIZE-1]

MPD File Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral's parameters that are fixed at FPGA configuration time. The parameters are described in the following table.

Table 2: MPD Parameters

Parameter	Description	Type
C_OPERATION	The vector operation to perform. The supported operations are: "and", "or", "xor", "not"	string
C_SIZE	The size of the vectors. Notice that the width of Op1, Op2 and Res must be equal. The minimum value of this parameter is 1.	integer

Device Utilization

The following table shows approximate resource utilization for the vector logic. The estimates shown are not guaranteed and can vary with FPGA family and speed grade, parameters selected for implementation, user timing constraints, and implementation tool version. Only parameters that affect resource utilization are shown in the following table.

Table 3: vector_logic Resource Utilization (Virtex™-II Pro)

Parameter value		Device Resources		
C_OPERATION	C_SIZE	Slices	Slice Flip-Flops	4-input LUTs
“and”	8	4	0	8
“xor”	12	6	0	12

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.