

Zynq UltraScale+ RFSoc Product Tables and Product Selection Guide



		Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	
RF Data Converter	Quad-core Arm® Cortex™-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5 MPCore up to 533MHz												
	12-bit RF-ADC w/DDC	# of ADCs	0	8	8	8	16	16	–	–	–	–	
		Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.275	–	–	–	–	
	14-bit RF-ADC w/DDC	# of ADCs	–	–	–	–	–	–	8	4	8	8	16
		Max Rate (GSPS)	–	–	–	–	–	–	2.5	5.0	5.0	5.0	2.5
	14-bit RF-DAC w/DUC	# of DACs	0	8	8	8	16	16	12	8	8	8	16
		Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0
		SD-FEC	8	0	0	8	0		8	0	8	0	
		RF input Freq max. GHz	4					5	6				
		Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x				
		System Logic Cells (K)	930	678	930	930	930	930	930	930	930	930	930
		CLB LUTs (K)	425	310	425	425	425	425	425	425	425	425	425
		Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0
		Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0
		UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5
		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272
		GTY Transceivers	16	8	16	16	16	16	16	16	16	16	16
		PCIe® Gen 3x16	2	1	2	2	2	2	–	–	–	–	–
		PCIeGen3 x16/Gen4 x8 / CCIX	–	–	–	–	–	–	2	2	2	2	2
	Programmable Logic (PL)		150G Interlaken	1	1	1	1	1	1	1	1	1	1
		100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	2	2	2	2	
		System Monitor	1	1	1	1	1	1	1	1	1	1	
		Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	
Package Footprint		Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	
D1156		35x35	214, 72, 208 4, 16 0, 0										
E1156		35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8				214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8		
G1517		40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8		
F1760		42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16					214, 96, 312 4, 16 16, 16
H1760		42.5x42.5							214, 48, 312 4, 16 12, 12				

Zynq® UltraScale+™ RFSoc Ordering Information



XC	ZU	##	D	R	-1	F	F	V	Footprint		E
Xilinx Commercial	Zynq UltraScale+	Value Index	Processor System Identifier D: Quad APU; Dual RPU	Engine Type R: RF Signal	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power	F: Flip-chip w/ 1.0mm Ball Pitch	F: Lid S: Lidless Stiffener	V: RoHS 6/6	D	#####	Temperature Grade (E, I)
									Package Designator	Package Pin Count	

E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = -40°C to +100°C)

Note: -L2E (Tj = 0°C to +110°C); -L2I (Tj = -40°C to +110°C)