Xilinx Power Tools Tutorial

Spartan-6 and Virtex-6 FPGAs

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XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
3/15/10	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This document contains tutorials that describe how to use the XPower Estimator (XPE) and XPower Analyzer (XPA), the Xilinx Power Tools, to arrive at realistic power consumption estimates for your design.

The Xilinx Power Tools cover different stages of the design flow. The tools can supply power estimates from the pre-design phase to the point at which the design is fully implemented. Because the Power Tools supply information throughout the design flow, they can be used for:

- Part selection
- Board design
- System reliability
- Power consumption estimation, analysis, and optimization

Additional Resources

- To download the XPower Estimator (XPE) spreadsheets, see the Power Solutions webpage on the Xilinx website at:

  http://www.xilinx.com/power

- To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

  http://www.xilinx.com/support

- The following are especially pertinent to the subject of this User Guide.
  - *Xilinx Power Estimator User Guide* (UG440)
  - *Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE)* (WP353)
  - Xilinx Power Analyzer (XPA) Online Help
  - *Test Boards for Area Array Surface Mount Package Thermal Measurements*
  - Descriptions of the resources available in an FPGA can be found under **FPGA Device Families** at http://www.xilinx.com/documentation.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File** > **Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**{**`on`**|**`off`**}
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**{**`on`**|**`off`**}

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-6 and Spartan-6 Power Tools Tutorial

Introduction

This tutorial provides advice on how to use the Xilinx® Power Tools for accurate power consumption estimation. The tutorial focuses on a simple Virtex®-6 and Spartan®-6 design for use in both an XPower Estimator (XPE) spreadsheet and XPower Analyzer (XPA) to illustrate Power Tool usage on the designs. This tutorial also describes the power optimization options in the ISE implementations tools.

Power in FPGAs

Xilinx constantly innovates to make sure the power challenges associated with shrinking technologies can be overcome. Xilinx understands that FPGA power consumption is one of the biggest concerns of FPGA users. Xilinx Power Tools help to perform power estimation and analysis for a given design. Power estimation and analysis becomes even more important as FPGAs increase in logic capacity and performance by migrating to smaller process geometries.

Total power in an FPGA is the sum of two components:

- **Static power** - Static power results primarily from transistor leakage current in the device. Leakage current is either from source-to-drain or through the gate oxide, and exists even when the transistor is logically "OFF".
- **Dynamic power** - Dynamic power is associated with design activity and switching events in the core or I/O of the device. Dynamic power is determined by node capacitance, supply voltage, and switching frequency (CV^2f).

The accuracy of the Xilinx Power Tools depends on two primary components:

- Device data models and device characterization integrated into the tools
- Inputs accurately entered by the user into the tools.

For accurate estimates of your application, enter realistic information which is as complete as possible. Modeling a certain aspect of the design in a manner that is overly conservative or that lacks sufficient knowledge of the design can result in unrealistic estimates.

Tutorial Design Information

The design used in this tutorial is not a functional design; it is only used to illustrate power tool capabilities and recommended usage. Synthesis and implementation have been performed on the design in ISE without any power optimization options.

The SAIF (simulation activity) file that is used as an input file for XPA was generated in the ISE Simulator (ISim). The SAIF file is a stimulus file from design simulation. For more details about SAIF generation using ISim, refer to the ISim User Guide (UG660).

Power Estimation Using XPE (XPower Estimator)

The XPower Estimator (XPE) spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project. XPE helps with architecture evaluation and device selection and helps you select the appropriate power supply and the thermal management components which may be required for your application.

As a pre-implementation tool, XPE can be used in the early stages of a design cycle when the RTL description of the design is incomplete. After implementation, the XPower Analyzer (XPA) tool (available in the ISE Design Suite software) can be used for more accurate estimates and power analysis.

XPE is a spreadsheet, so all Microsoft Excel functionality is fully retained in the writable (unprotected) sections of the spreadsheet.

The goal of this tutorial is not to give an exhaustive overview of XPE, but to give an example of basic XPE features, allowing you to perform a quick power estimation for your design. For a complete description of XPE, see the Xilinx Power Estimator User Guide (UG440).

For an accurate XPE estimation, you will have to estimate the amount of device resources your design will use. If you are not sure how to make this estimate it might be best to run through an example design in ISE and take a look at the Map Report file, which contains resource usage information.

XPE displays tabs for each type of component in a device architecture (for example, I/Os, BRAMs, and DCMs). The number of tabs displayed in XPE will vary depending on your device architecture. For example, in this tutorial, the device selected does not have any MGT circuitry and so the MGT tab is not included.

The 11.4 version of XPA is used in this tutorial. Below are the steps that will allow you to perform accurate power analysis using XPE. You can use either the Spartan-6 or Virtex-6 design with this tutorial.

Step 1

Download the latest available spreadsheet for your targeted device, and the tutorial design files. The XPE spreadsheets and the tutorial design files are both available at the Power Solutions web page here:

http://www.xilinx.com/power

This tutorial uses this 11.4 version of the spreadsheet:

- Virtex-6: `Virtex5_Virtex6_XPE_11_4.xls`

  OR

- Spartan-6: `Spartan3a_Spartan6_XPE_11_4.xls`

Step 2

Import the MRP (MAP Report) file from the working directory of either the Virtex-6 or Spartan-6 tutorial design. To do so, click the **Import from ISE** button in the XPE spreadsheet to automatically load the spreadsheet with the design resources.

Note: In many cases, you will be entering information into XPE before your design has been implemented in ISE, and there will not be an MRP file to import into XPE. For this tutorial, however, you imported an MRP file to give the XPE spreadsheet some initial information.

Figure 1: **Import from ISE Button**

File name of tutorial Map Report:

- Virtex-6: `V6_tutorial_top_16bit_map.mrp` (MAP Report to be imported in XPE)
- Spartan-6: `S6_tutorial_top_16bit_map.mrp` (MAP Report to be imported in XPE)

For cases in which you have already used XPE for a given design and you want to upgrade the XPE version, you can click the **Import from XPE** button to import the information from the earlier XPE spreadsheet into the updated XPE spreadsheet.

Figure 2: **Import from XPE Button**

Step 3

In the **Summary** tab, check the **Device** information and enter **Environment** data as follows:

- **Ambient Temp** = 25°C
- **Heat Sink** = None
- **Airflow** = 0

Note: FPGA quiescent power is highly affected by environment settings, so it is important you try to match as precisely as possible your board's environment and the board data. Power Tools can be very useful to perform what-if analysis and define the best thermal strategy for the board.

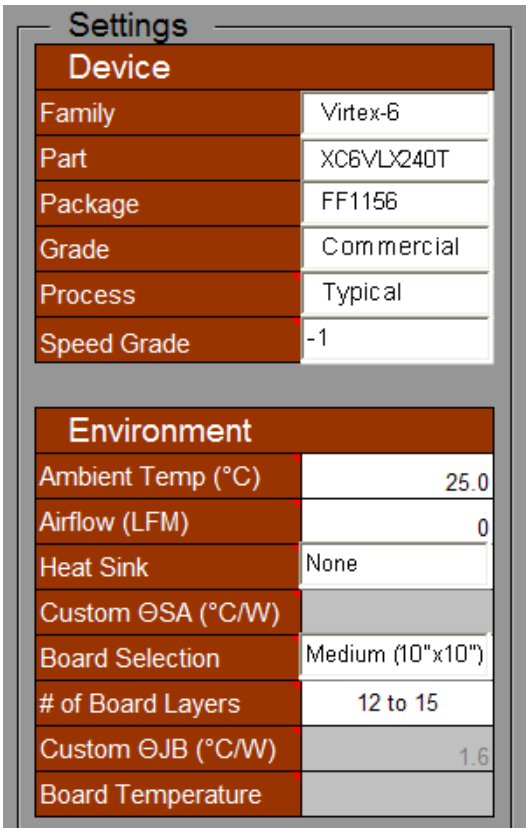


Figure 3: **Device and Environment Settings for Virtex-6 Design**

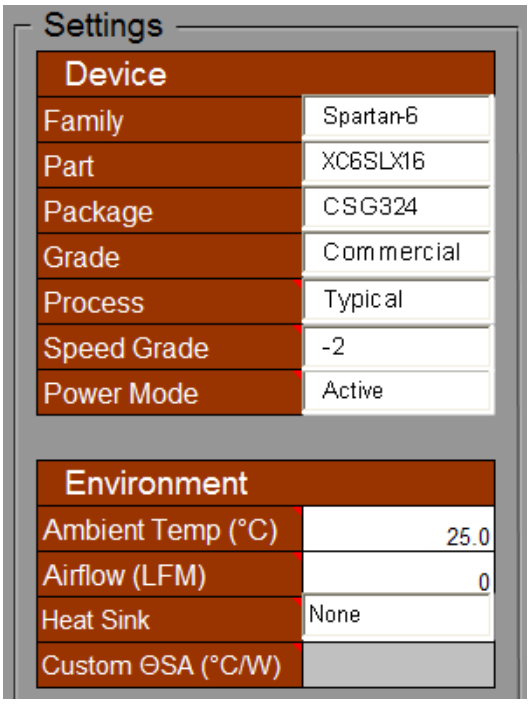


Figure 4: **Device and Environment Settings for Spartan-6 Design**

Step 4

Set the overall Toggle Rate of the spreadsheet. To do so, from the **Summary** tab, click the **Set Toggle Rate** button and enter a rate of **12.5**. This is the default value in the Default Toggle Rate dialog box.

Using the **Set Toggle Rate** toolbar button will set a fixed toggle rate to all relevant design elements (Logic, I/Os, BRAM, DSP), but this toggle rate can be adjusted for individual elements in other tabs of the spreadsheet.

Figure 5: **Set Toggle Rate Button**

Most logic-intensive designs work at around 12.5% of the average toggle rate (12.5% is the default value used in XPE). For a worst- case estimate, a toggle rate of 20% can be used. Average toggle rates greater than 20% are not very common. Arithmetic-intensive modules of a design seem to take toggle rates of up to 50%, which is representative of the absolute worst case. An example of this would be a Multiply-Accumulate operation. It is also common to model toggle rate for random input data at 50%. To appreciate what 100% toggle rate means, think of a constantly enabled toggle flip-flop (TFF) whose data input is tied High. The T-output of this flip-flop toggles every clock edge. Very few designs could have an average toggle rate that high (100%).

Step 5

Set the overall clock frequency of the spreadsheet. To do this, from the **Summary** tab, click the **Set Default Clock** button and set the rate to **200** MHz (the default). This is the default value in the Default Clock Frequency dialog box.

Using this toolbar button sets the clock frequency for all relevant design elements, such as Clocks, Logic, I/Os, BRAMs, and DSP elements. Having a single clock frequency for all these elements is not realistic; however, individual elements can be adjusted in other tabs of the spreadsheet later on.

Figure 6: **Set Default Clock Button**

The default clock frequency of 200 MHz is a conservative value. This provides a conservative, dynamic power estimation.

Step 6

If you are working in the Virtex-6 design, set the clock frequency, multiply counter, and Clock0 Divide values in the **MMCM** tab for the two MMCM components in the design.

Set the first MMCM as follows:

- **Clock (MHz)** = 200MHz
- **Multiply Counter** = 4
- **Clock 0 Divide** = 5
- Leave default value for other fields.

Set the second MMCM as follows:

- **Clock (MHz)** = 33 MHz
- **Multiply Counter** = 25
- **Clock 0 Divide** = 25
- Leave default value for other fields.

At this point, the power number reported in the **Summary** tab will look like this for the Virtex-6 design:

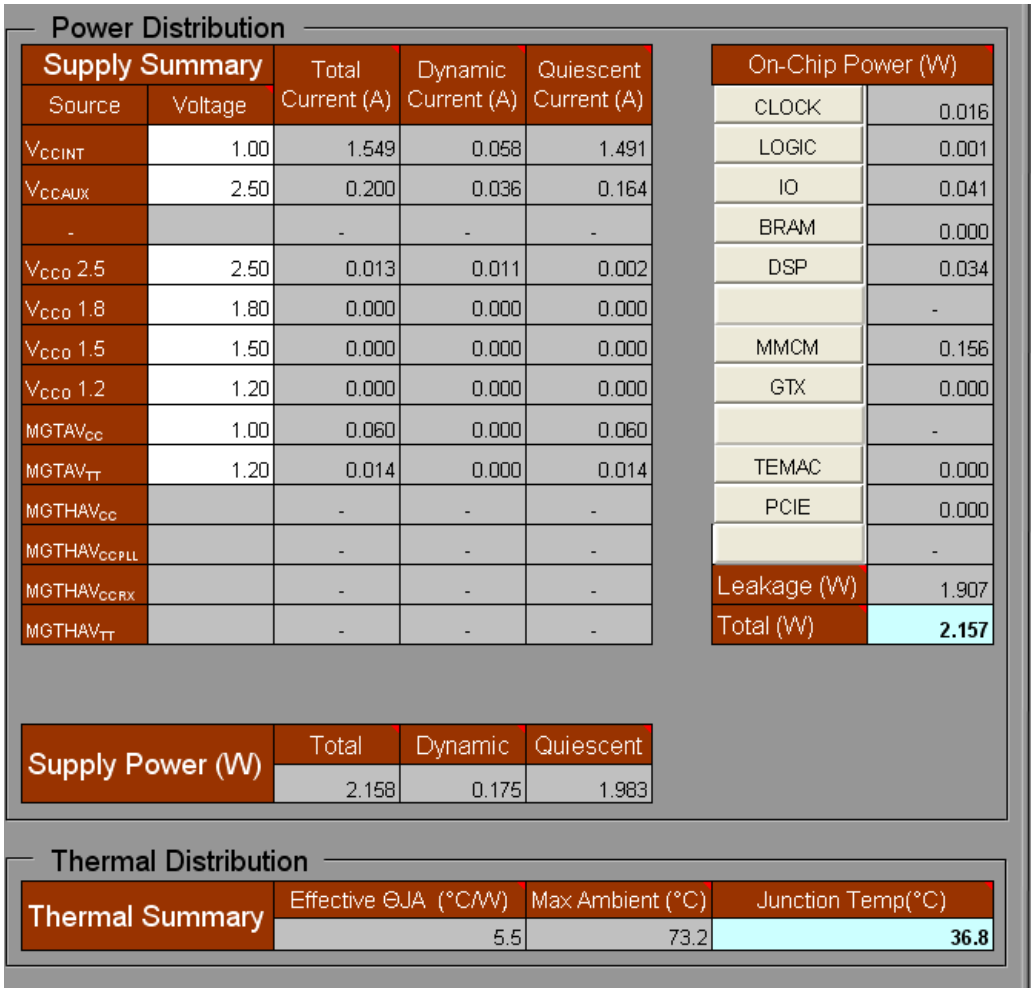


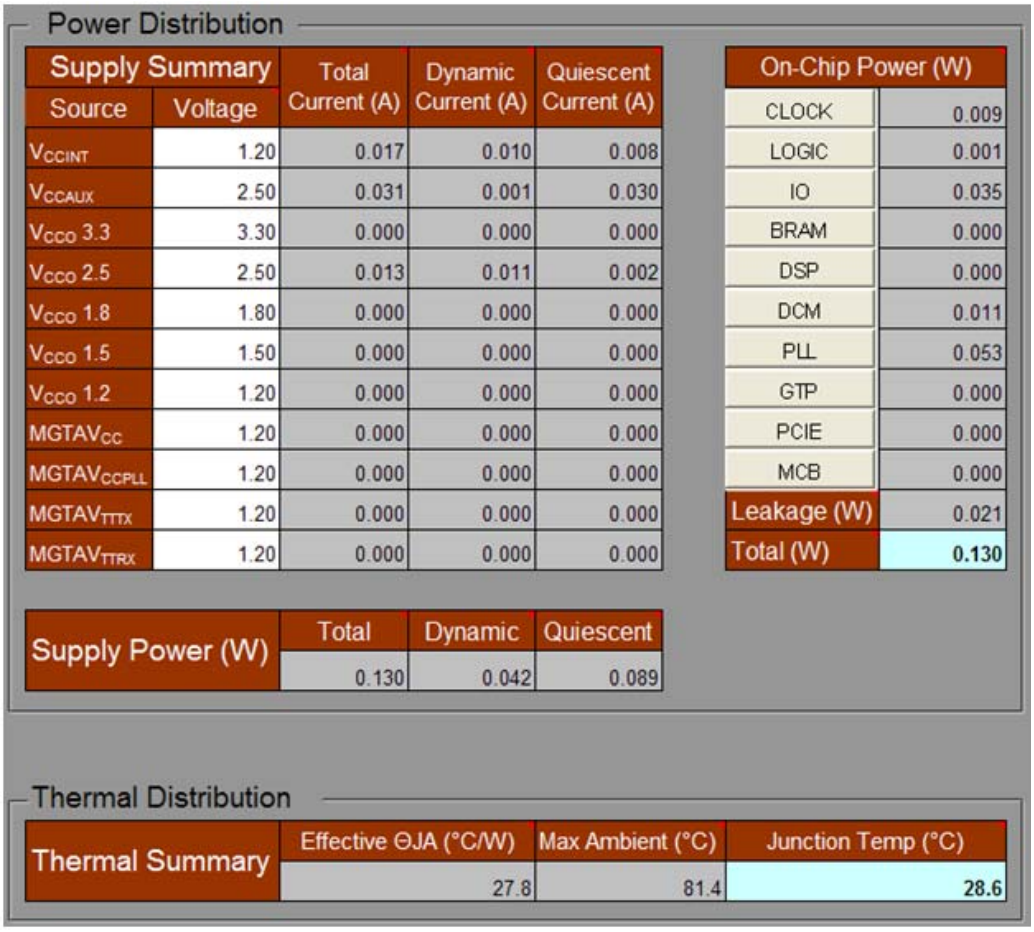
Figure 7: **Power and Thermal Distribution - XPE for Virtex-6 FPGAs**

If you are working in the Spartan-6 design, set the clock frequency, multiply counter, and Clock0 Divide values in the **PLL** tab for the PLL component in the design.

Set the PLL to the following attributes:

- **Clock (MHz)** = 33 MHz
- **Multiply Counter** = 25
- **Clock 0 Divide** = 25
- Leave default values for the rest of the field

At this point, the **Summary** tab of the spreadsheet should look like the following figure for the Spartan-6 design:



Power Distribution

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
V_{CCINT}	1.20	0.017	0.010	0.008
V_{CCAUX}	2.50	0.031	0.001	0.030
V_{CCO} 3.3	3.30	0.000	0.000	0.000
V_{CCO} 2.5	2.50	0.013	0.011	0.002
V_{CCO} 1.8	1.80	0.000	0.000	0.000
V_{CCO} 1.5	1.50	0.000	0.000	0.000
V_{CCO} 1.2	1.20	0.000	0.000	0.000
$MGTAV_{CC}$	1.20	0.000	0.000	0.000
$MGTAV_{CCPLL}$	1.20	0.000	0.000	0.000
$MGTAV_{TTTX}$	1.20	0.000	0.000	0.000
$MGTAV_{TTRX}$	1.20	0.000	0.000	0.000

On-Chip Power (W)	
CLOCK	0.009
LOGIC	0.001
IO	0.035
BRAM	0.000
DSP	0.000
DCM	0.011
PLL	0.053
GTP	0.000
PCIE	0.000
MCB	0.000
Leakage (W)	0.021
Total (W)	**0.130**

Supply Power (W)	Total	Dynamic	Quiescent
	0.130	0.042	0.089

Thermal Distribution

Thermal Summary	Effective ΘJA (°C/W)	Max Ambient (°C)	Junction Temp (°C)
	27.8	81.4	**28.6**

Figure 8: **Power and Thermal Distribution - XPE for Spartan-6 FPGAs**

Step 7

View the ISE Map Report (MRP) file that you imported into XPE to verify that the design elements have been automatically ported into XPE. In XPE, separate the design elements by clock domains.

The **Import from ISE** feature that imported data from a Map Report (MRP) file entered approximate values for design elements in the **CLOCK**, **LOGIC**, **IO**, **BRAM** and **DSP** tabs. This can be improved if you have a good understanding of how these elements are used in

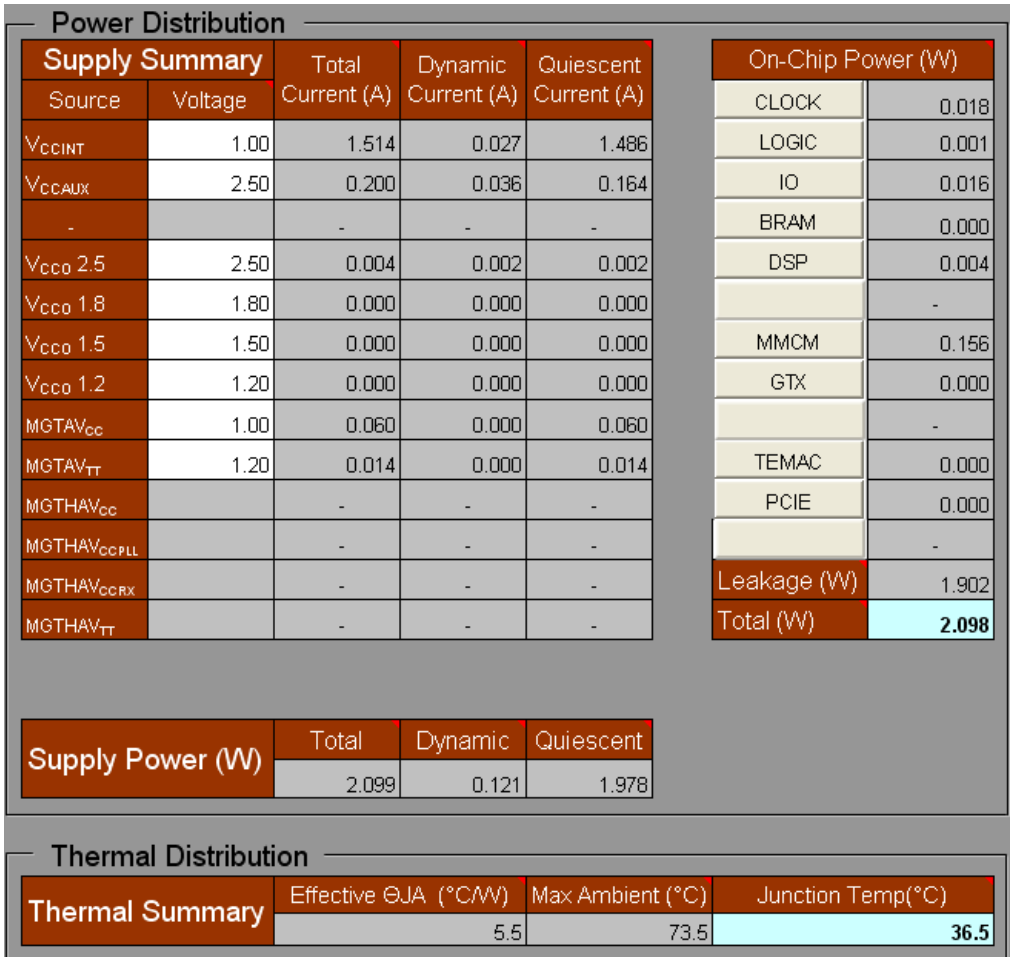
your design. Extracting additional data from the MRP file and adjusting the values in the XPE spreadsheet helps to get a more accurate power estimation.

Note: Using the **`-detail`** option in MAP will generate a verbose Map report that can help you to gather more detailed information on the design. This will help to adjust XPE design elements after data has been imported from the MRP file (MAP report). More information about this option is found in the Command Line Tools User Guide (UG628).

If you are working in the Virtex-6 design, modify the entries for the following elements:

- In the **CLOCK** tab, you can simplify the clock usage to two clocks.
  - The first clock should be set as follows:
    - **Frequency (MHz)** = 200 MHz
    - **Fanout** = 68
  - The second clock should be set as follows:
    - **Frequency (MHz)** = 33 MHz
    - **Fanout** = 63
- In the **LOGIC** tab, change the **Toggle Rate** to 19%, which is the average estimated value for this design.
- In the **IO** tab, change the **Clock (MHz)** (clock frequency) for the LVCMOS I/Os to 33 MHz and the **Toggle Rate** to 14% for both I/O types, which is the average estimated value for all I/Os of this design.
- For the **DSP** tab, change the **Toggle Rate** for all DSP components to 1.5%, which is the average estimated value.

After all relevant setting have been entered or updated, power results are available in the **Summary** tab of the spreadsheet. The following figure shows the new result from modifications for the Virtex-6 design.



Power Distribution

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
V_{CCINT}	1.00	1.514	0.027	1.486
V_{CCAUX}	2.50	0.200	0.036	0.164
-		-	-	-
V_{CCO} 2.5	2.50	0.004	0.002	0.002
V_{CCO} 1.8	1.80	0.000	0.000	0.000
V_{CCO} 1.5	1.50	0.000	0.000	0.000
V_{CCO} 1.2	1.20	0.000	0.000	0.000
$MGTAV_{CC}$	1.00	0.060	0.000	0.060
$MGTAV_{TT}$	1.20	0.014	0.000	0.014
$MGTHAV_{CC}$		-	-	-
$MGTHAV_{CCPLL}$		-	-	-
$MGTHAV_{CCRX}$		-	-	-
$MGTHAV_{TT}$		-	-	-

On-Chip Power (W)	
CLOCK	0.018
LOGIC	0.001
IO	0.016
BRAM	0.000
DSP	0.004
	-
MMCM	0.156
GTX	0.000
	-
TEMAC	0.000
PCIE	0.000
	-
Leakage (W)	1.902
Total (W)	**2.098**

Supply Power (W)	Total	Dynamic	Quiescent
	2.099	0.121	1.978

Thermal Distribution

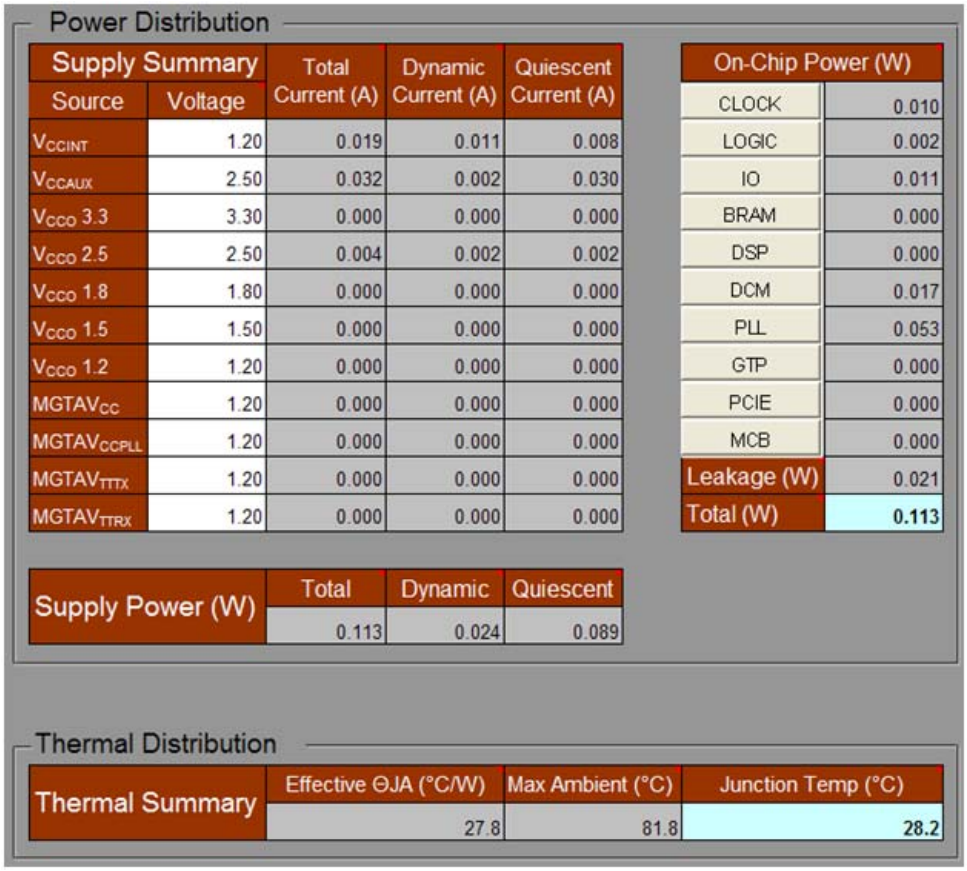
Thermal Summary	Effective ΘJA (°C/W)	Max Ambient (°C)	Junction Temp(°C)
	5.5	73.5	**36.5**

Figure 9: **Updated Power and Thermal Distribution in XPE for Virtex-6 FPGA**

If you are working in the Spartan-6 design, change the entries for the following elements:

- In the **CLOCK** tab, modify the clock usage to two clocks
  - The first clock should be set as follows:
    - **Frequency (MHz)** = 200 MHz
    - **Fanout** = 63
  - The second clock should be set as follows:
    - **Frequency (MHz)** = 33 MHz
    - **Fanout** = 28
- In the **LOGIC** tab, change the **Toggle Rate** to 19%, which is the average estimated value.
- In the **IO** tab, change the **Clock (MHz)** (clock frequency) for the LVCMOS I/Os to 33 MHz and the **Toggle Rate** to 14% for both I/O types, which is the average estimated value for all I/Os of this design.

After all relevant settings have been entered or updated, the power results are available in the **Summary** tab of the spreadsheet. The following figure shows the new results from the recent modification for the Spartan-6 design.



Power Distribution

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
V_{CCINT}	1.20	0.019	0.011	0.008
V_{CCAUX}	2.50	0.032	0.002	0.030
V_{CCO} 3.3	3.30	0.000	0.000	0.000
V_{CCO} 2.5	2.50	0.004	0.002	0.002
V_{CCO} 1.8	1.80	0.000	0.000	0.000
V_{CCO} 1.5	1.50	0.000	0.000	0.000
V_{CCO} 1.2	1.20	0.000	0.000	0.000
$MGTAV_{CC}$	1.20	0.000	0.000	0.000
$MGTAV_{CCPLL}$	1.20	0.000	0.000	0.000
$MGTAV_{TTTX}$	1.20	0.000	0.000	0.000
$MGTAV_{TTRX}$	1.20	0.000	0.000	0.000

On-Chip Power (W)	
CLOCK	0.010
LOGIC	0.002
IO	0.011
BRAM	0.000
DSP	0.000
DCM	0.017
PLL	0.053
GTP	0.000
PCIE	0.000
MCB	0.000
Leakage (W)	0.021
Total (W)	0.113

Supply Power (W)	Total	Dynamic	Quiescent
	0.113	0.024	0.089

Thermal Distribution

Thermal Summary	Effective ΘJA (°C/W)	Max Ambient (°C)	Junction Temp (°C)
	27.8	81.8	28.2

Figure 10: **Updated Power and Thermal Distribution in XPE for Spartan-6 FPGA**

After the data is entered and the part is operating within the thermal limits of the selected grade, the power reported by XPE can be used to specify the voltage rails for the design. If your confidence in the data entered is not very high, you may add additional padding to the numbers to circumvent the possibility of under-designing the power system for the FPGA. If, however, you are fairly certain of the data entered, no additional padding above the data reported by XPE is necessary.

Although XPE is primarily intended to be used early in design conception to scale the power budget it can be used later on in the design stages to get accurate power estimation (as described in Step 7) or to perform worst case power analysis. For further details about this analysis and XPE, refer to the Xilinx Power Estimator User Guide (UG440) and the White Paper Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE) (WP353).

Key Points for Interpreting Power Results

- XPE reports the total supply power reported across all voltage sources (**Supply Power** table). Information is broken out between **Quiescent** and **Dynamic** power. The table includes all power required by the internal logic along with external (off-chip) power eventually sourced by the device, depending on the design IO configurations.
- XPE reports the power dissipated on-chip across all power rails (**On-Chip Power** table). It includes quiescent, leakage and dynamic power and the total is broken out by resource type. This view can help determine the amount of power being consumed

and dissipated by the device. It also helps identify potential areas in the design where power optimization techniques could be used to meet the targeted power budget.

- XPE also reports Thermal data (**Thermal Summary** table), giving the estimated Junction Temperature of the FPGA related to the package characteristics and the thermal power (on-chip power).

Power Reduction Options in ISE

Depending on the design itself, power optimization options used in the ISE design flow can be more or less efficient. When **-power** switches are used in synthesis and implementation, an average power reduction of approximately 10% is expected, with a small runtime penalty (approximately 15%) and a potentially small percentage of performance degradation. Because the design used in this tutorial is rather small, the dynamic power is much lower than the static power. Under these conditions, using power optimization options available in synthesis and implementation aren't relevant and won't help.

In ISE there are a few process properties available to help reduce power in your design. You can set these properties in Synthesis, Map, and PAR processes.

Synthesis Power Reduction

You can reduce power with the **-power** switch in synthesis. The **Power Reduction** property in ISE instructs XST to optimize the design to consume as little power as possible. Macro processing decisions are made to implement functions in a manner that uses minimal power.

To access synthesis properties in ISE:

1. In the Processes tab, right-click **Synthesize** and select **Process Properties**.
2. In the Synthesis Options dialog box, verify or change the Power Reduction setting.

Map Power Reduction

One option in Map for power reduction is to use the **-global_opt** switch (**Global Optimization** property in ISE). This switch will specify that placement is optimized to reduce the power consumed by a design during timing-driven packing and placement, which is set with the Map **-timing** switch. Global optimization includes logic remapping and trimming, logic and register replication, optimization, and logic replacement of tri-states. Depending on the design, this switch can help reduce power. These routines will extend the runtime of Map because of the extra processing that occurs. By default, this option is off. For further information on this option, see the Command Line Tools User Guide (UG628).

Another option in Map for power reduction is to use the **-power** switch (**Power Reduction** property in ISE), and then specify a switching activity file to guide power optimization. The switching activity file is specified with the **-activity** switch (**Power Activity File** property in ISE). This switch will specify that placement is optimized to reduce the power consumed by a design during timing-driven packing and placement, which is set with the Map **-timing** option. When the **-power** option is selected, a switching activity file may also be specified to guide power optimization.

Place & Route (PAR) Power Reduction

Finally, you can reduce power using the **-power** switch in PAR (**Power Reduction** property in ISE). This switch instructs PAR to optimize the capacitance of non-timing critical design signals.

The power savings from using these different options is going to vary depending on the design. Your design may not contain any elements (or any routing options) that are eligible for power optimization.

Power Analysis Using Xilinx Power Analyzer (XPA)

Xilinx Power Analyzer (XPA) does an analysis on real design data. Use XPA after design implementation in ISE, using the NCD file output from Place & Route (PAR). XPA now features a vectorless estimation algorithm; a way of assigning activity rates to nodes even if these activity rates are not defined in the design file or specified in any other way. However, we recommend using simulation activity files (SAIF or VCD) from simulation for accurate power analysis. We recommend always using the latest version of ISE to get the latest version of XPA, which contains the latest characterization data for power analysis.

XPA is used for design power optimization. At the point in your design phase when XPA is used, your ISE project should have successfully completed Place & Route (PAR) and generated an NCD output file. It is important to understand which design files are used by the XPA tool for power estimation. In this tutorial, either a Spartan-6 design on the SP601 board or a Virtex-6 design is used for power estimation and both are included for reference.

XPA can be started as a standalone graphical user interface (GUI), from within a project in ISE, or from the command line. The XPA GUI can be opened standalone by entering **xpa** at the command line. To generate a text-based power report, enter **xpwr**. Note that you can type just **xpwr** in a command shell and all the switch options will be displayed. In ISE, XPower Analyzer can be found in the Processes tab, under **Place & Route**.

To run XPA, you need to at least have an NCD file, meaning your design must successfully pass the Place & Route phase. If you want to improve the accuracy of XPA you can also include optional design files. To include optional files in ISE design flow:

1. In the Processes tab, right-click **XPower Analyzer**.
2. Select **Process Properties**.
3. In the XPower Analyzer Properties dialog box, specify the files.

In the standalone tool, you will have the option to include these files when you load the design. Specify the files to include in the Open Design dialog box.

The files you can specify to add information to your analysis are:

- **NCD** - Output file from PAR that is required by XPA for power analysis.
- **Settings file** - Optional file. The Settings file contains application settings and node activity rates saved from an XPower Analyzer session. Any manual changes (edits) you have made in the XPA window can be saved to a settings file. The settings file (in XML format) can then be used to load any relevant design information from a previous XPA session into a later session.
- **PCF** - Optional file. The PCF (Physical Constraints File) contains constraint information to help determine clock frequencies. All clock information from the UCF (User Constraints File) are reported in the PCF, so if the design is well constrained loading the PCF is important for accurate power results.

- **VCD or SAIF file** - Optional file. These simulation activity files include specific switching information (toggle rates, signal rates, and frequency information) that will give the most accurate power estimation. Note that XPA might not always be able to match all of your design nets with nets in the simulation file so you may have to enter some switching information manually. It is important to make sure you look at what design information was pulled in and what (if any) design information was not pulled in. In the Console window take note of any warning messages, since they may indicate that design information was not pulled into XPA.

The 11.4 version of XPA is used in this tutorial. Below are the key steps that will allow you to perform a power analysis using XPA. You can use either the Virtex-6 or Spartan-6 design for this tutorial.

Step 1

Open XPA in one of these ways:

- In ISE, in the Processes tab, double-click the **XPower Analyzer** process, located under **Place & Route**.

  When you open XPA from ISE, you are analyzing a design that has already been fully placed and routed.

  OR

- Open XPA standalone. To do so:
  a. Select **Start > Run**.
  b. At the command prompt, type **`xpa`** and press **Enter**.

Step 2

In XPA, open the design files in this way:

1. Select **File > Open Design**.
2. In the Open Design dialog box, select the files to use for either the Virtex-6 or Spartan-6 tutorial design.
   - Virtex-6:
     - `V6_tutorial_top_16bit.ncd` (Post-Place and Route NCD file)
     - `V6_tutorial_top_16bit.pcf` (Physical Constraints File)
     - `V6_simulation_XPA_stimulus_file.saif` (Stimulus file from Simulation)
   - Spartan-6:
     - `S6_tutorial_top_16bit.ncd` (Post-Place and Route NCD file)
     - `S6_tutorial_top_16bit.pcf` (Physical Constraints File)

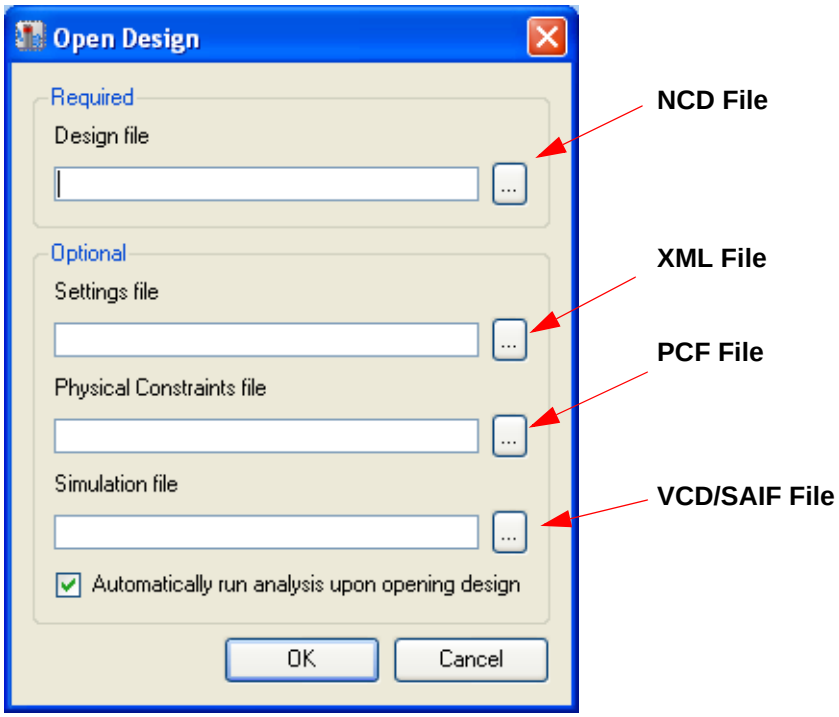


Figure 11: **Open Design Dialog Box (XPA)**

Step 3

Once XPA is completely opened and has analyzed the design using the specified input files, these report views are displayed:

- The **Summary** view displays all the important voltage rail information.
- The **Thermal Information** view shows thermal information to be used in the device power calculation, and allows you to set the relevant thermal setting to match your hardware and environment (see Figure 12). Ambient temperature is 25°C by default, but you can change this value. Also, you can enter a custom junction temperature, a custom Theta JA (if using a heatsink), and airflow information. This thermal information directly affects your power estimation.
- The **Voltage Source Information** view displays the power drawn from each voltage supply along with both quiescent (Iccq) and dynamic current (Icc). In this report view, you can adjust each supply voltage within the recommended operating condition range given in the device datasheet.
- The **Settings** view allows you to change certain settings globally; you can enter output load information, toggle rate, and enable rate information.

When XPA has completed its design analysis after you open the specified input files, go to the **Thermal Information** view and change the relevant thermal settings as follows:

- **Ambient Temp** = 25°C
- **Heat Sink** = None
- **Airflow** = 0

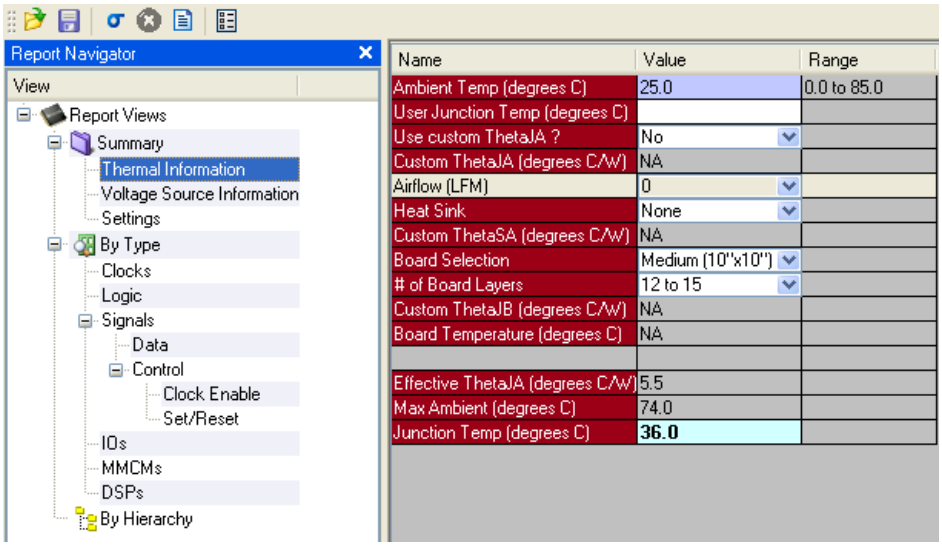


Figure 12: **Thermal Information View - XPower Analyzer (XPA)**

Step 4

For a design in which no VCD or SAIF stimulus file is available yet, you can use the **Settings** view to enter estimated activity rates for all different design elements. The vectorless analysis engine will then propagate these settings to your design.

Note that activity rates from the **Settings** view are used by XPA as initial inputs for the vertorless propagation engine. If you want to set the **By Type** entries (for example, the enable rate for BRAMs or the toggle rate for DSPs) to specific values, make your changes in the appropriate **By Type** view (not in the **Settings** view), so the changes will remain if you then update the power analysis.

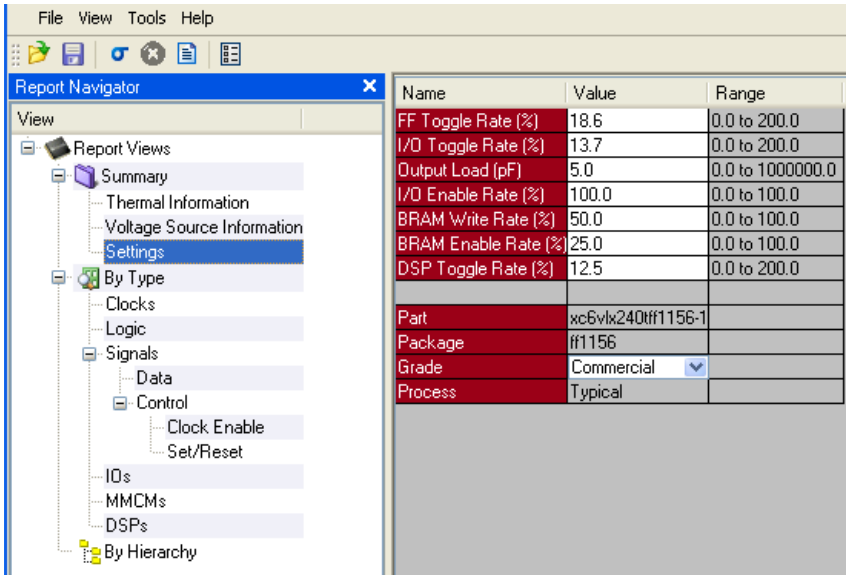


Figure 13: **Settings View - XPower Estimator (XPA)**

Remember that every time a setting or a value is changed or updated in XPA, you must then update the power analysis (**Tools > Update Power Analysis**).

Step 5

The **By Type** views break down the power estimation into specific groups, much like the tabs found in XPE. These components depend on the architecture being targeted and whether the components available in the device are being used in the design. Only those blocks present in your design will be listed.

In the **By Type** views you will also have the option to modify signal rate or toggle rate information, if needed. These sections are similar to what was found in XPE, but in XPA you do not have the option to change much for the power estimation. If a signal needs to change you will need to go back into your design to alter it.

In the **Clocks** view (under **By Type**), make sure all clock frequencies have been correctly extracted from the Physical Constraints File (PCF). If the clocks in your design were properly constrained in the UCF (User Constraints File) before implementation then frequencies should be correctly extracted from the PCF (Physical Constraints File) in XPA.

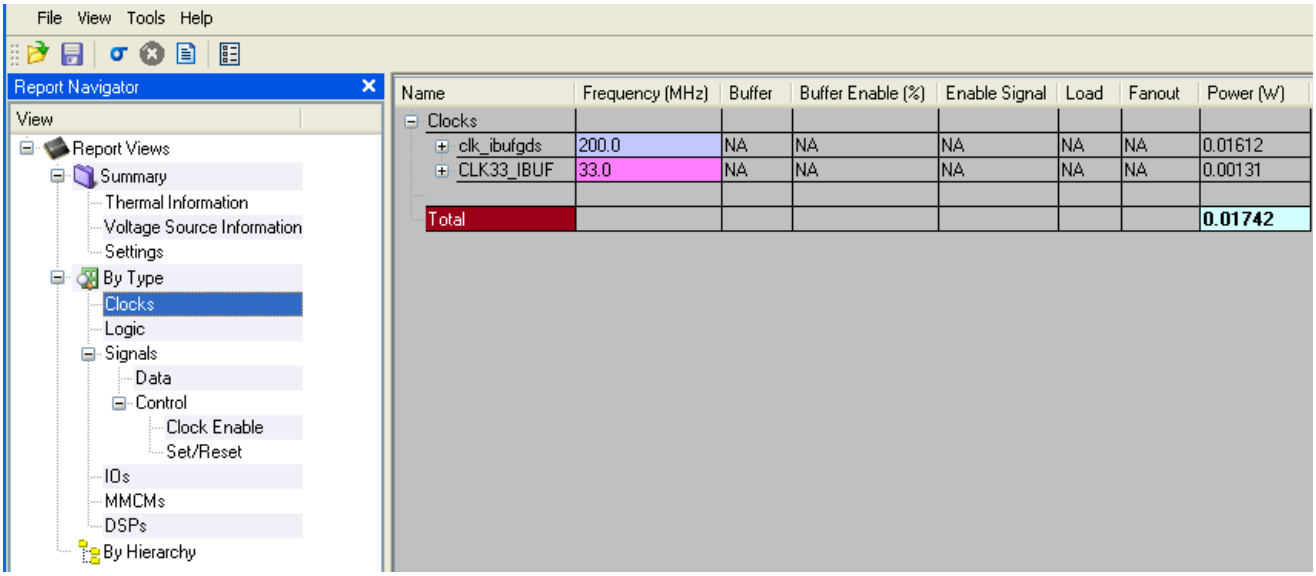


Figure 14: **Clocks View - XPower Analyzer (XPA)**

Once all settings are properly set, the **Summary** lists all relevant power figures for the design analyzed.

The two figures below compare results when XPA is loaded with the same NCD and settings but different stimulus analysis from simulation. In Figure 15, information was estimated by the vectorless estimation algorithm. In Figure 16, information was supplied by an SAIF file extracted from simulation.

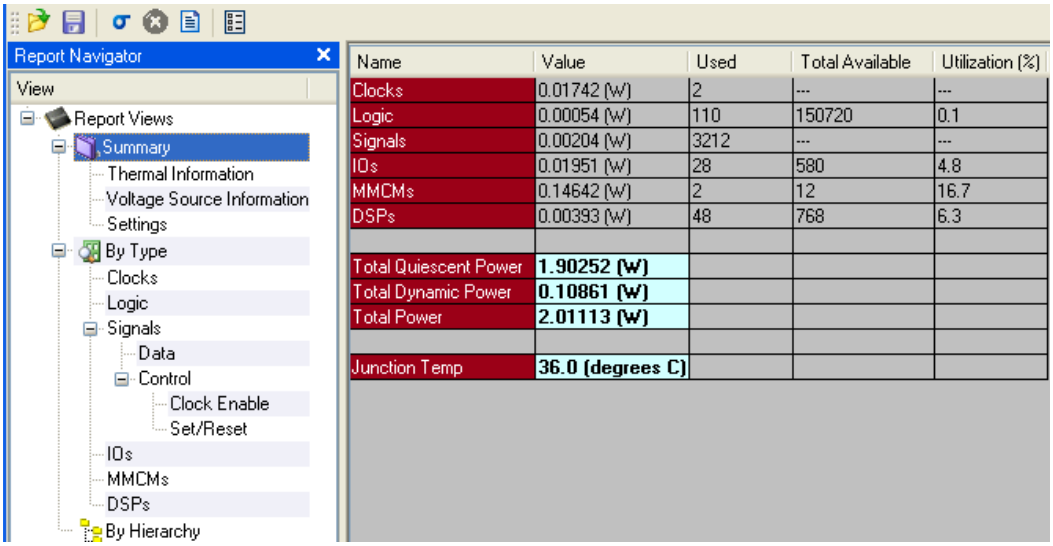


Figure 15: **Summary View Using Vectorless Estimation Algorithm - XPower Analyzer (XPA)**

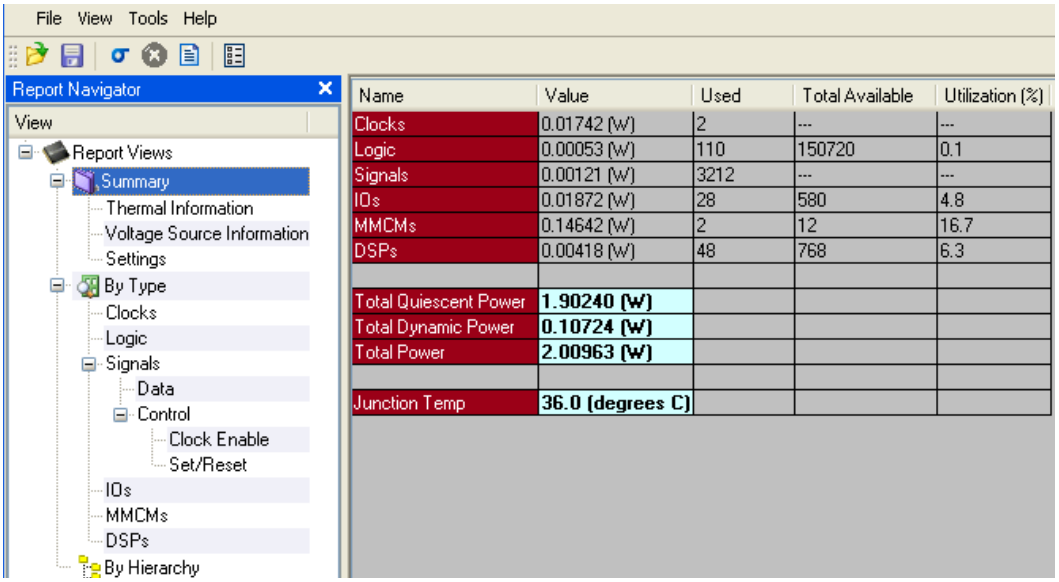


Figure 16: **Summary View with Simulation Data - XPower Analyzer (XPA)**

Although the design used in this tutorial doesn't highlight this very significantly, the vectorless algorithm will display relatively close power numbers, but using an SAIF file that reflects design activity accurately is the recommended flow for XPA power analysis if you are looking for the most accurate results.

For general guidelines for power optimization in Xilinx FPGAs (related to the Power Tools or to your design), refer to the White Paper Virtex-5 FPGA System Power Design Considerations (WP285), which is also valid for Virtex-6 devices.

For further details about XPA, refer to the XPA Help, accessible from the following web page:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/hh_goto.htm#xpa_c_overview.htm

Conclusion

When using the Xilinx Power Tools, XPE is used for pre-design power estimation and XPA is used for post-implementation design power optimization. You can load design information into XPE with your Map Report file; however, you do not need any design information to estimate the power of an FPGA. In XPA, a design NCD file is required to estimate power, and optional stimulus files can be used to increase the accuracy of estimation. Finally, you can also use the different power options in ISE to help reduce power in a given design.

Since the Xilinx Power Tools cover different stages of the design flow, the tools can be used for:

- Part selection
- Board design
- System reliability
- Power consumption estimation for a specific design

The Power Tools can be used for power optimization as well. You can identify which parts in the design are responsible for the most power consumption. You can then find tradeoffs to design for power. This can also be coupled with power optimization options available in synthesis and implementation within ISE.

With precise data entered into the Power Tools, accurate power estimations can be achieved relatively easily by following the advice from this tutorial.