PlanAhead Software Tutorial

Quick Front-to-Back Overview

UG 673 (v 12.3) September 21, 2010

Demo Design License

The PlanAhead™ software source code includes the source code for the following programs:

Centerpoint XML

- The initial developer of the original code is CenterPoint – Connective Software
- Software Engineering GmbH. portions created by CenterPoint – Connective Software
- Software Engineering GmbH. are Copyright© 1998-2000 CenterPoint - Connective Software Engineering GmbH. All Rights Reserved. Source code for CenterPoint is available at http://www.cpointc.com/XML/

NLView Schematic Engine

- Copyright© Concept Engineering.

Static Timing Engine by Parallax Software Inc.

- Copyright© Parallax Software Inc.

Java Two Standard Edition

- Includes portions of software from RSA Security, Inc. and some portions licensed from IBM are available at http://oss.software.ibm.com/icu4j/
- Powered By JIDE – http://www.jidesoft.com

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR
PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Free IP Core License

This is the Entire License for all of our Free IP Cores.

Redistribution and use in source, netlist, binary and silicon forms, with or without modification, are permitted provided that the following conditions are met:

Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.

Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.

Neither the name of ASICS World Services, the Authors and/or the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS “AS IS” AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Table of Contents

Quick Front-to-Back Overview 7
Introduction 7
Sample Design Data 7
Xilinx ISE and PlanAhead Software 7
Required Hardware 7
PlanAhead Documentation and Information 8
Tutorial Description 8
Tutorial Objectives 8
Tutorial Procedure 8
Step 1: Creating a New Project Step 1 9
Step 2: Using the Sources View and the RTL Editor Step 2 15
Step 3: Synthesizing the Design Step 3 18
Step 4: Implementing the Design Step 4 23
Step 5: Analyzing the Results Step 5 25
Step 6: Creating the Bitstream File Step 6 29
Conclusion 30

PlanAhead Tutorial

Quick Front-to-Back Overview

Introduction

This tutorial provides a quick introduction to some of the capabilities and benefits of using the Xilinx® PlanAhead™ software. PlanAhead software can be used during various stages of the design process for a variety of purposes.

Sample Design Data

This tutorial uses sample design data that is included with the PlanAhead software release package. The tutorial design data is located in the following directory:

`<ISE_install_Dir>/PlanAhead/testcases/PlanAhead_Tutorial.zip`

Extract the zip file into any write-accessible location. The location of the unzipped `PlanAhead_Tutorial` data is referred to as the `<Extract_Dir>` throughout this document.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is required each time you run the tutorial. Refer to the *Tutorial Description* section for more information about the example design.

Xilinx ISE and PlanAhead Software

By default, the PlanAhead software is installed with the ISE® Design Suite. Ensure that the PlanAhead software is operational and the sample design data is installed before beginning the tutorial. For installation instructions and information, see the *ISE Design Suite 12: Installation, Licensing, and Release Notes* on the Xilinx web site:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_3/irn.pdf

Required Hardware

Xilinx recommends 2 GB or more of RAM for use with PlanAhead on larger devices. For this tutorial, a smaller design was used, with a limited number of designs open at any one time. 1 GB of RAM should be sufficient, but it could impact performance.

PlanAhead Documentation and Information

For information about the PlanAhead software, please see the following documents, which are available with your software:

- *PlanAhead User Guide* (UG632) - Provides detailed information about the PlanAhead software. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_3/PlanAhead_UserGuide.pdf
- *Floorplanning Methodology Guide* (UG633) - Provides floorplanning hints. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_3/Floorplanning_Methodology_Guide.pdf
- *Hierarchical Design Methodology Guide* (UG748) - Provides an overview of the PlanAhead hierarchical design capabilities. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_3/Hierarchical_Design_Methodology_Guide.pdf
- For additional information about PlanAhead, including video demonstrations, go to http://www.xilinx.com/planahead

Tutorial Description

The small sample design used throughout this tutorial consists of a small design called *bft*. There are several VHDL and Verilog source files in the bft design.

The design targets an xc6vlx75T device. A small design is used to allow the tutorial to be run with minimal hardware requirements and to enable timely completion of the tutorial, as well as to minimize the data size.

The tutorial design data is modified during the process of performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is suggested for each time the tutorial is performed. For more information on the tutorial data, refer to the “Sample Design Data” section of this chapter.

If you have any questions or issues with the tutorial contact Xilinx Technical Support.

Tutorial Objectives

This tutorial provides a quick walk through of the front-to-back, RTL-to-bitstream design flow.

Many of the PlanAhead analysis features are covered in more detail in other tutorials. Not every command or command option is represented here. This tutorial uses the features contained in the PlanAhead software product, which is bundled as a part of ISE Design Suite 12.

Tutorial Procedure

This tutorial contains the following steps:

Step 1 Creating a New Project

Step 2 Using the Sources View and the RTL Editor

Step 3 Synthesizing the Design

Step 4 Implementing the Design

Step 5 Analyzing the Results

Step 6 Creating the Bitstream File

Step 1: Creating a New Project Step 1

PlanAhead enables several types of projects to be created depending on where in the design flow the tool is being used. RTL sources can be used to create a Project for development and analysis, synthesis, implementation and bit file creation.

1-1. Open the software.

- On Windows, select the Xilinx PlanAhead 12 Desktop icon or **Start > Programs > Xilinx ISE Design Suite 12.3 > PlanAhead > PlanAhead**.
- On Linux, change the directory to `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`, and type **`planAhead`**.

The PlanAhead Getting Started Help page opens.

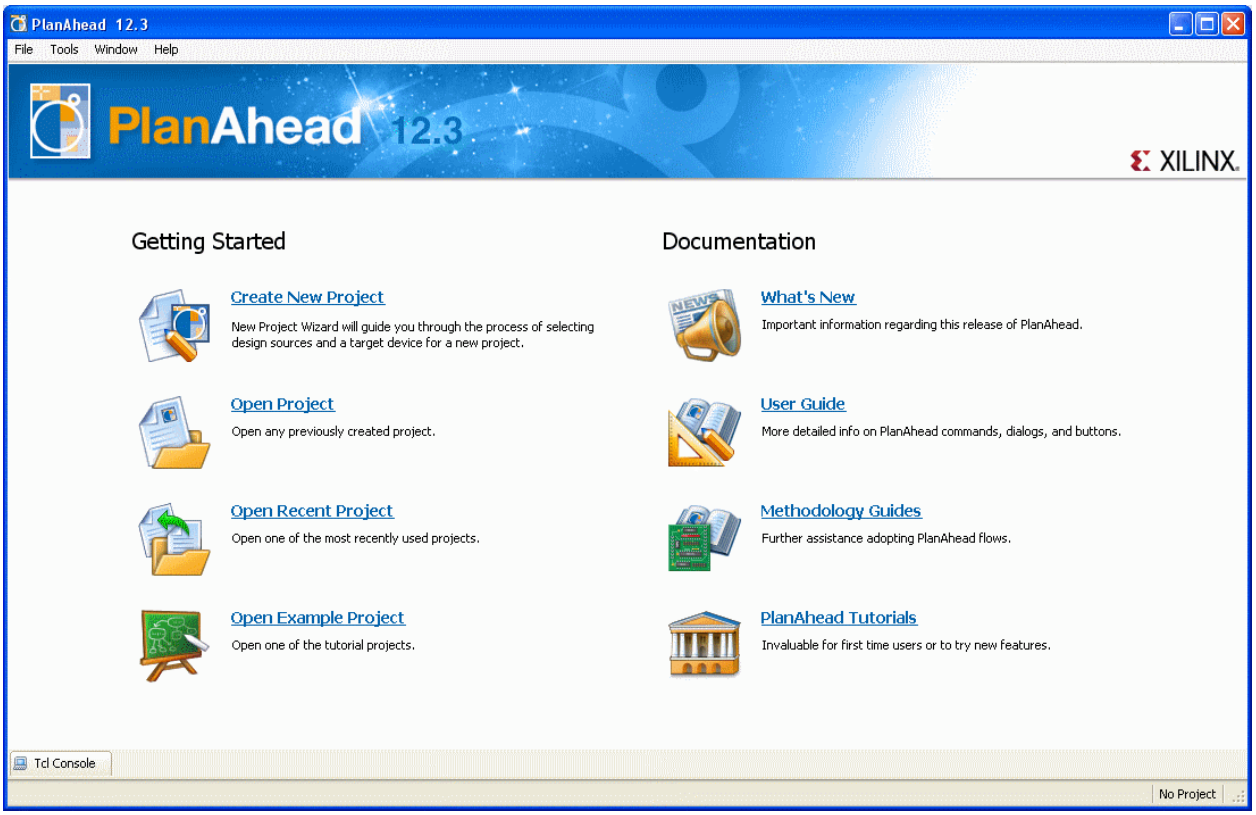

Figure 1: The PlanAhead Getting Started Page

Notice that the *PlanAhead Getting Started* page contains links to open or create projects, and to view documentation.

1-2. Create a new RTL project called *project_1* using some of the RTL source files in the *<Extract_Dir>*\PlanAhead_Tutorial\Sources\hdl directory.

1-2-1. Select the **Create New Project** link on the Getting Started page.

The Create a New PlanAhead Project confirmation dialog box opens.

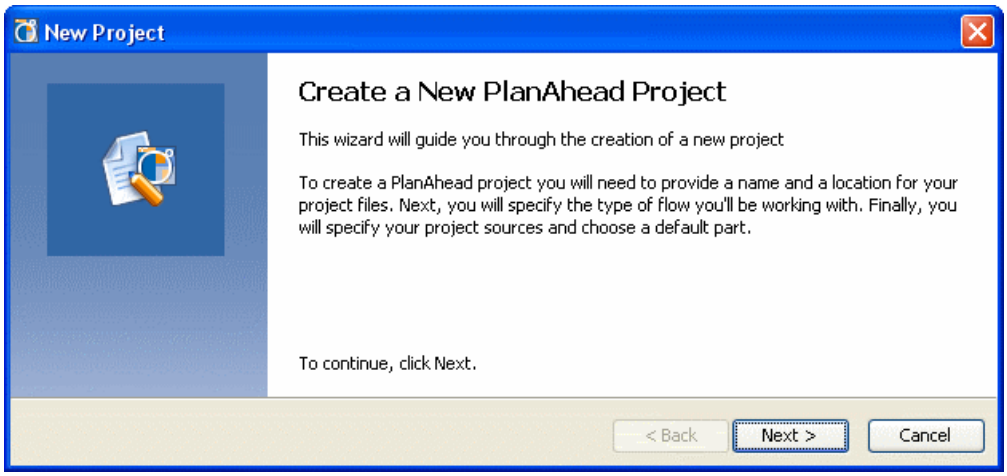

Figure 2: New Project Overview

1-2-2. Click **Next**.

The Project Name page opens.

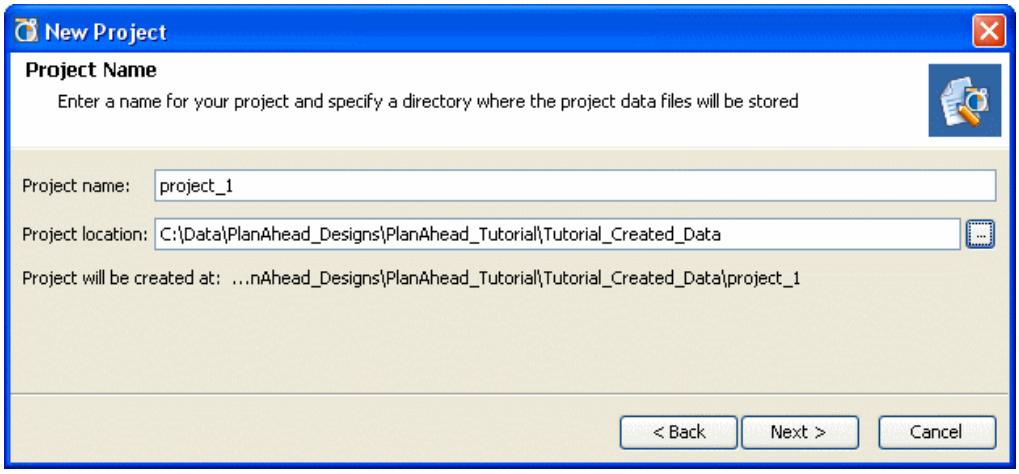

Figure 3: Project Name Page of the New Project Wizard

1-2-3. Browse to and select the following folder: *<Extract_Dir>*\PlanAhead_Tutorial\Tutorial_Created_Data.

1-2-4. Use the default Project name: **project_1**, then click **Next**.

The Design Source page opens.

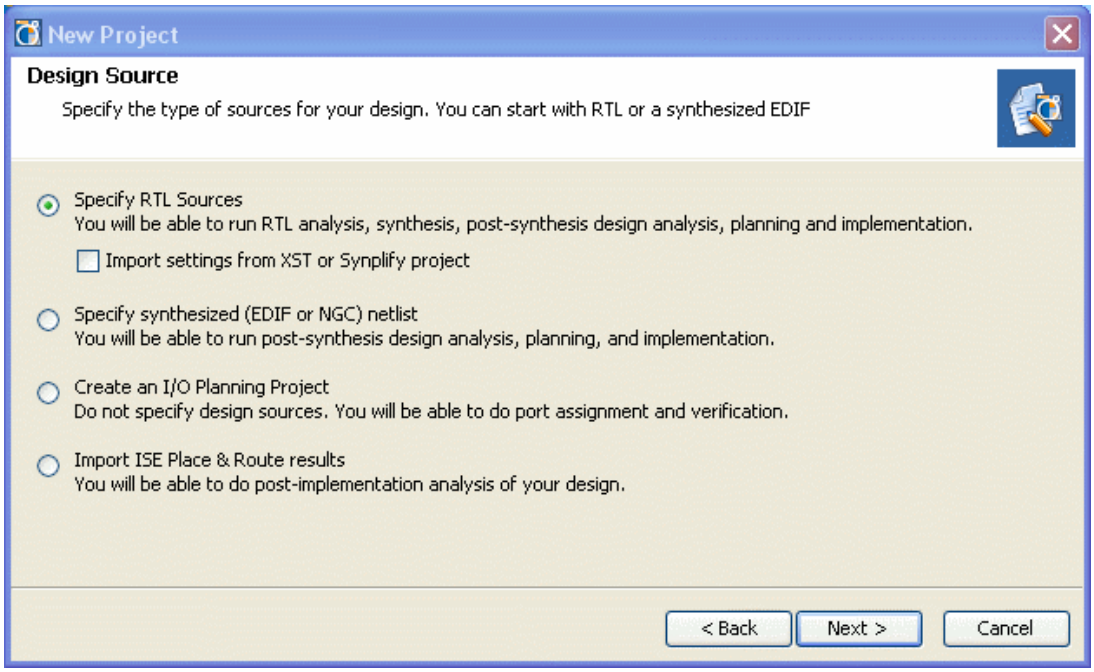

Figure 4: Electing to Import RTL Sources

1-2-5. Click the **Specify RTL Sources** option, and then click **Next**.

The Add/Create Sources page opens (Figure 5).

1-3. Add directories and files, and set the VHDL Library.

1-3-1. Click the **Add Files** button and browse to the following directory:
`<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl.`

1-3-2. Press the **Ctrl** key to select *bft.vhdl, FifoBuffer.v*, and *async_fifo.v,* and click **Open.**

1-3-3. Select the Add Directories button, and browse to select the following directory:
<*Extract_Dir*>**/PlanAhead_Tutorial/Sources/hdl/bftLib**.

1-3-4. Click on the **work** entry in the Library field for bftLib, and type **bftLib**.

1-3-5. Click to select the **Copy Sources into Project** checkbox.

1-3-6. Click to unselect the Add Sources from Subdirectories checkbox.

1-3-7. Verify that the page looks like Figure 5.

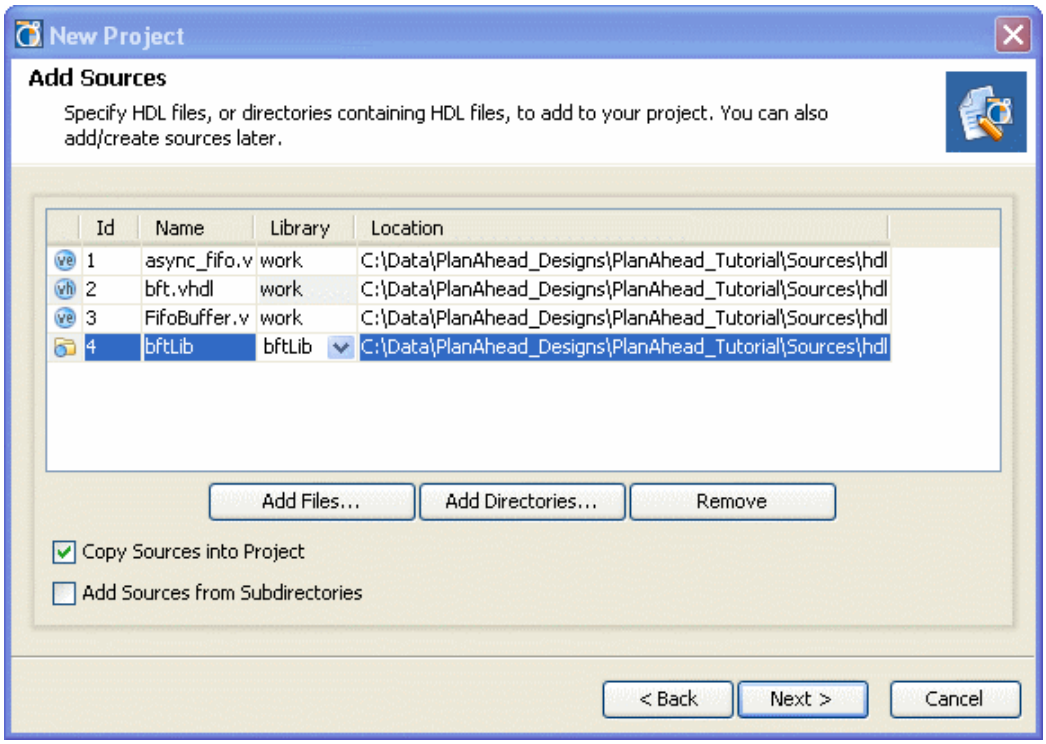

Figure 5: Selecting Sources to Add to the Project

1-3-8. When done, click **Next**

The Constraints Files page opens.

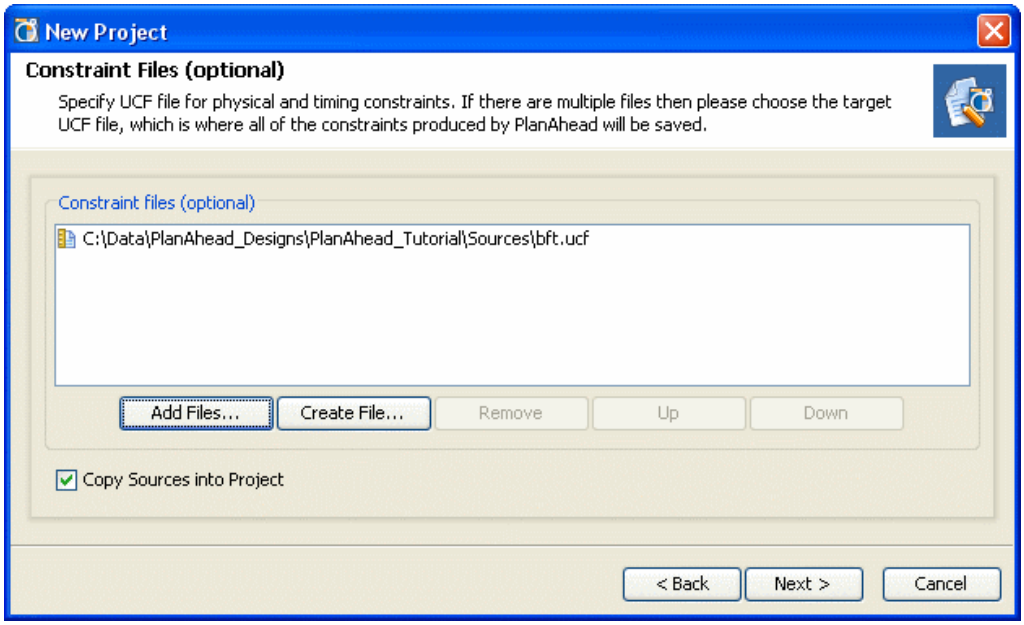

Figure 6: Constraint Files Page of the New Project Wizard

1-4. Add a constraint file.

1-4-1. Select the **Add Files** button and browse to select the following directory: ***<Extract_Dir>*/PlanAhead_Tutorial/Sources/bft.ucf**.

1-4-2. Click **Next**.

The Default Part page opens (Figure 7).

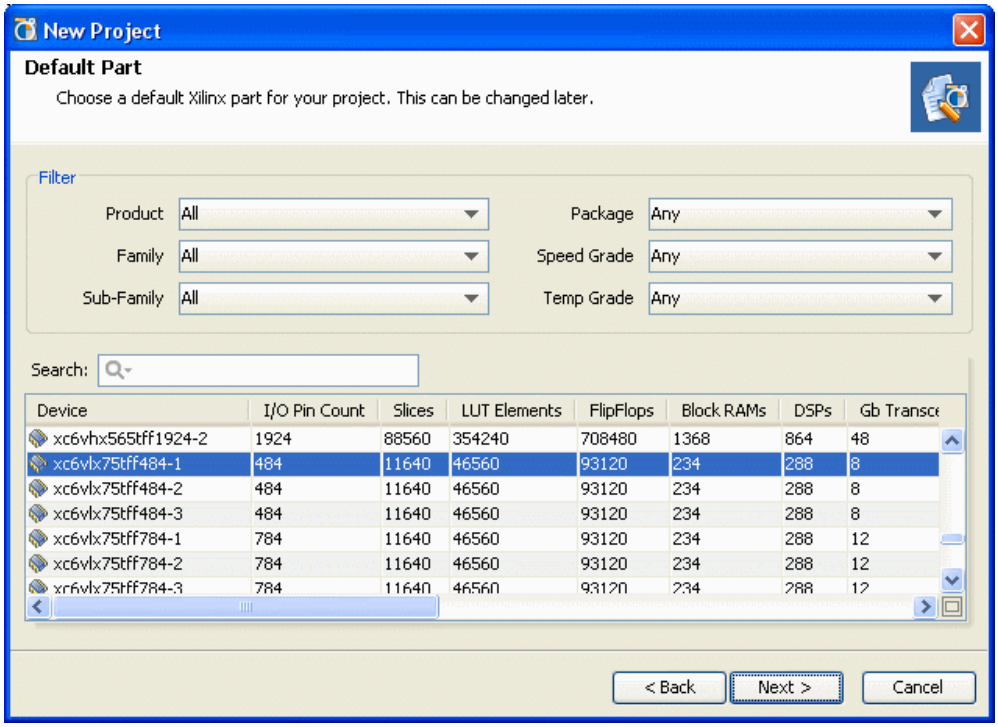

Figure 7: Selecting a Family and Default Part

1-5. Select a default part.

1-5-1. Select the **xc6vlx75tff484-1** device and click **Next**.

1-5-2. Review the New Project Summary page, and click **Finish**.

The PlanAhead environment opens.

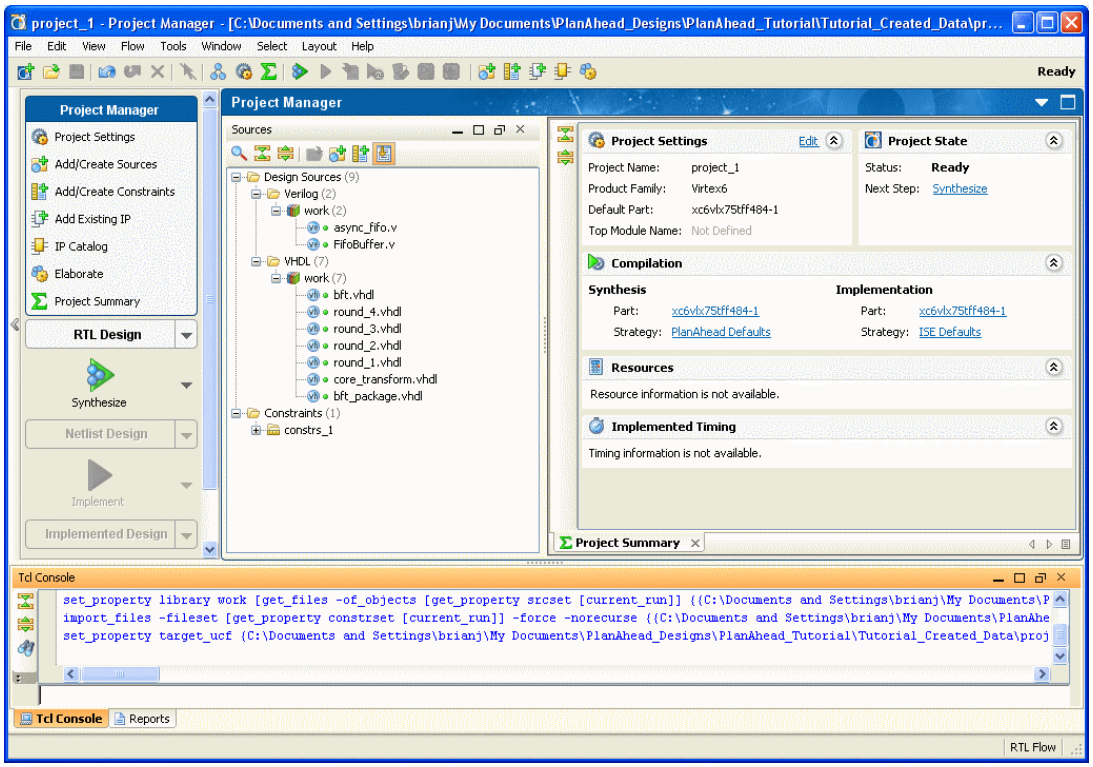

Figure 8: The PlanAhead Environment

Step 2:Using the Sources View and the RTL Editor Step 2

The PlanAhead software allows different file types to be added as design sources including Verilog, VHDL, and NGC format cores. The files display by category in the Sources view. An RTL Editor is supplied to create or develop RTL sources.

2-1. Explore the Sources view and Project Summary.

2-1-1. Examine the information in the Project Summary. More information displays as the design progresses.

2-1-2. Examine the Sources view.

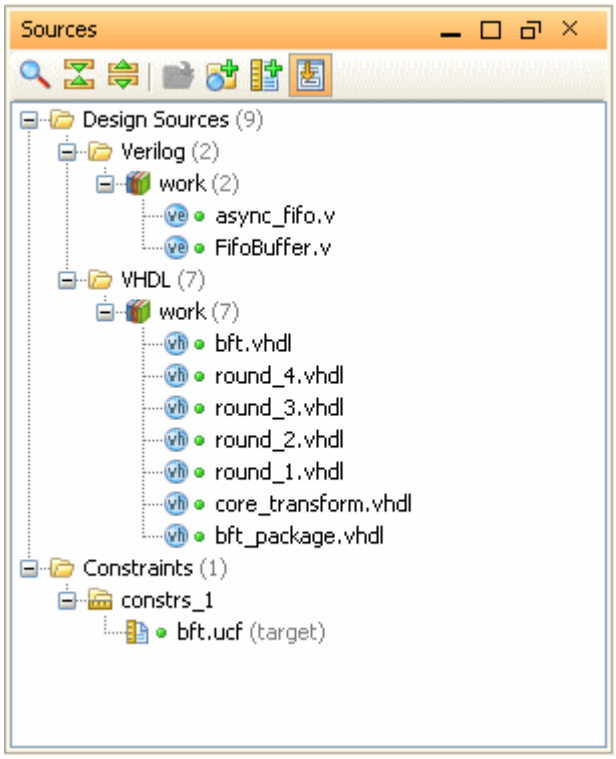

Figure 9: Viewing Sources

Notice the Design Sources are grouped by file type. The Library folders help keep track of VHDL source files.

2-2. Explore the Sources view commands and RTL Editor.

2-2-1. Select one of the VHDL sources in the Sources view.

2-2-2. Right-click to review the commands available in the Sources view popup menu.

2-2-3. Select **Open File** and use the scroll to browse the text in the RTL Editor.

Alternately, you could double-click on source files in the Sources view to open them in the RTL Editor.

2-2-4. With the cursor in the RTL Editor, right-click and select **Find in Files**. The Find in Files dialog box displays.

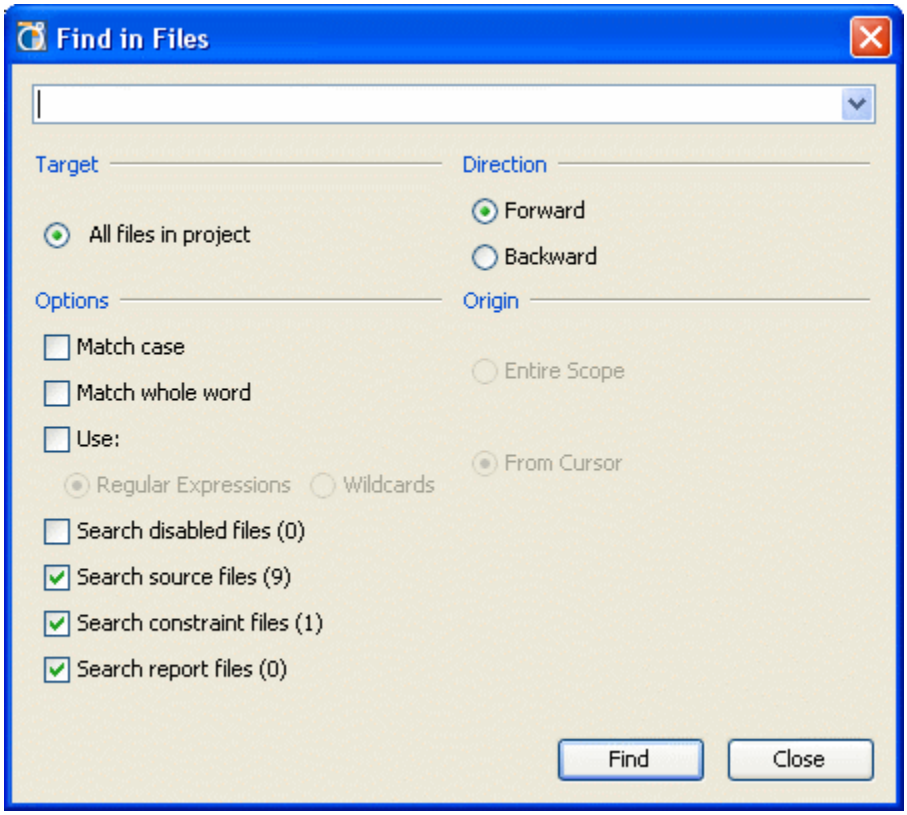

Figure 10: Using the Find in Files Command

2-2-5. Type `clk` and click **Find**.

The Find in Files view displays in the messaging area at the bottom of the PlanAhead environment.

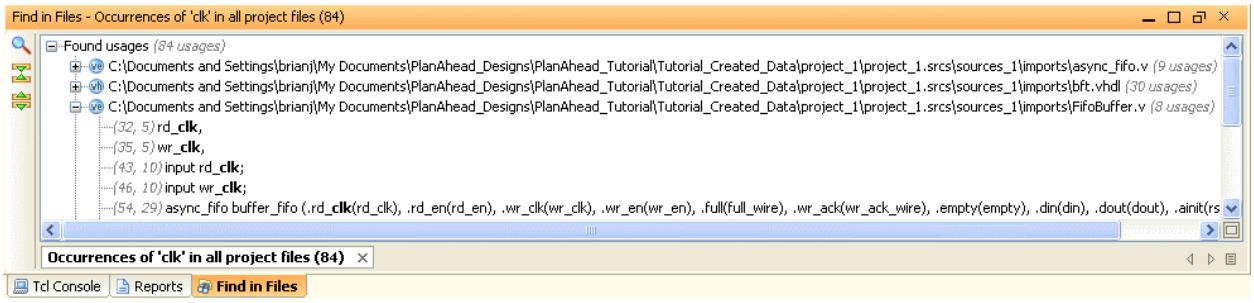

Figure 11: Viewing the Find in Files Results

2-2-6. In the Find in Files view, expand and select one of the occurrences of clk and notice that the RTL Editor now displays the file and occurrence.

2-2-7. Close the Find in Files – Occurrences view.

2-2-8. Close each of the open RTL file tabs in the RTL Editor.

***Note*:** The PlanAhead software also includes an RTL analysis and IP customization environment. This environment is covered in the PlanAhead *RTL Design and IP Generation with CORE Generator* tutorial. You can click the RTL Design button in the Flow Navigator to quickly explore the features. The RTL design is elaborated first which enables various analysis views including an RTL Netlist, Schematic, Graphical Hierarchy, and estimated resource statistics. The views do a “cross-select”, which allows you to debug and optimize the RTL.

Note: The Xilinx IP Catalog provides access to the Xilinx Core Generator software tool to generate IP. You can sort and search the Catalog in a variety of ways. IP can be customized, generated and instantiated. There are also several RTL DRCs to check for areas to improve performance or power on the RTL.

Step 3: Synthesizing the Design Step 3

PlanAhead enables one or more synthesis runs to be configured, launched, and monitored, either sequentially or simultaneously.

The Synthesize command configures and launches a single run which is the basic flow used in this Tutorial. It can be accessed in the Flow Navigator view on the left side of the PlanAhead Environment.

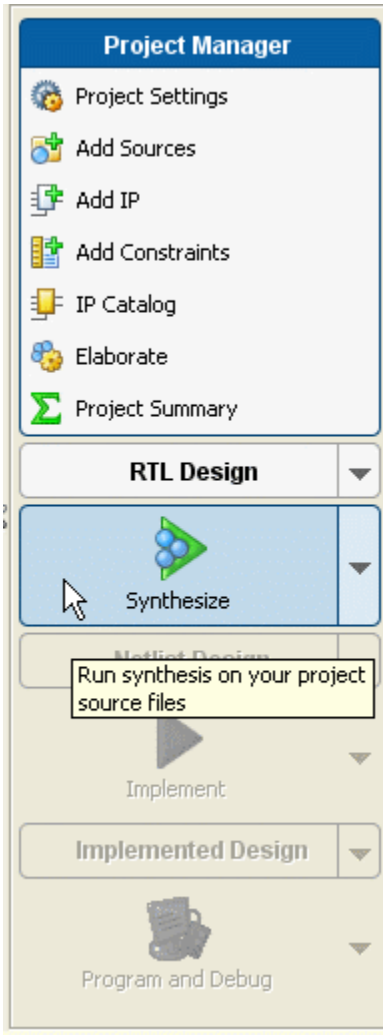

Figure 12: Flow Navigator

The Flow Navigator launches all major design compilation processes including synthesis, implementation and generate bitstream.

It also enables you to open the compiled RTL Design, the synthesized Netlist Design or the Implemented Design results.

3-1. Explore Synthesis options, launch synthesis, and monitor a run.

3-1-1. In the Flow Navigator, expand the drop-down menu next to the **Synthesize** button and select **Synthesis Settings.**

The Synthesis Settings dialog box opens.

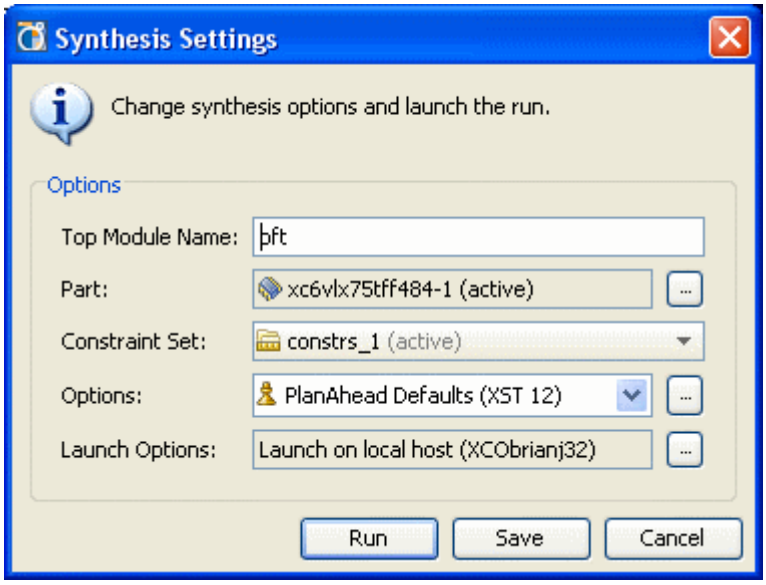

Figure 13: Synthesis Settings Dialog Box

3-1-2. Click the **Top Module Name** field and type **`bft`** .

3-1-3. Use the default Part and Constraint Set.

3-1-4. Select the Options browser icon to display the Synthesis Options dialog box.

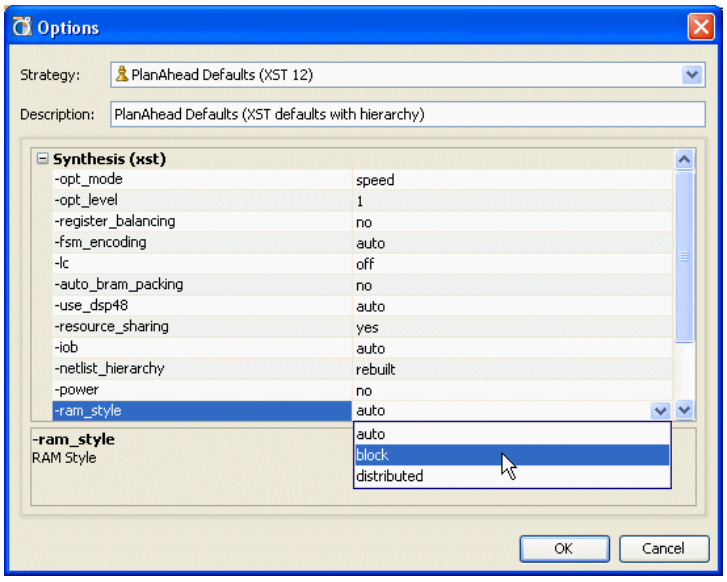

Figure 14: Synthesis Options Dialog Box

3-1-5. Review the available options.

3-1-6. Select the **Strategy** drop-down menu, review the available Synthesis Strategies, and click **Cancel**.

3-1-7. Select the Launch Options browser icon to open the Specify Launch Options dialog box.

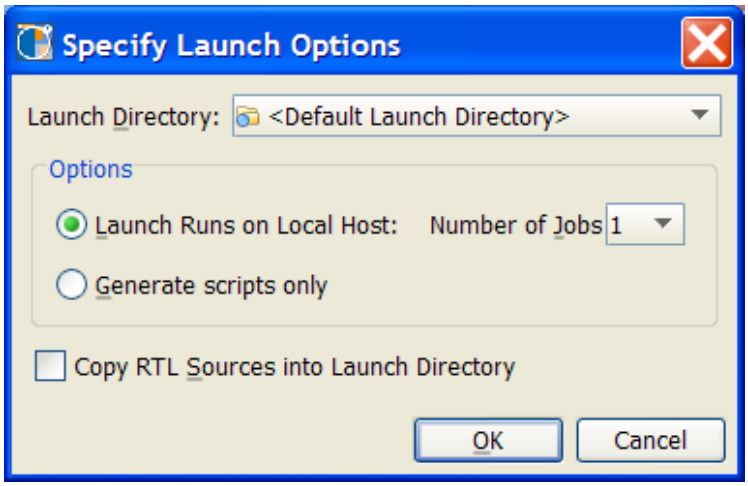

Figure 15: Selecting Synthesis Launch Options

3-1-8. Review the options, select the **Launch Runs on Local Host,** and click **OK**.

3-1-9. In the Synthesis Settings dialog box click **Run** to launch the run.

Notice the Status bar in the upper right corner displays `Synthesizing (XST)` which indicates that synthesis is now running.

The Compilation Log view displays the output messages from the ISE commands while the Compilation Messages view displays a filtered list of Warnings and Errors. Clicking on the Synthesis messages in the Compilation Log view will open the RTL file and display the corresponding line of RTL code that it is referencing.

3-2. Opening the Netlist Design.

3-2-1. Allow the synthesis run to complete and then click **Open Netlist Design** in the Synthesis Completed dialog box.

3-2-2. If prompted, click **Yes** to close the RTL Design (only if you opened it).

The PlanAhead Design Planner environment displays with the synthesized netlist, target part and active constraint set applied.

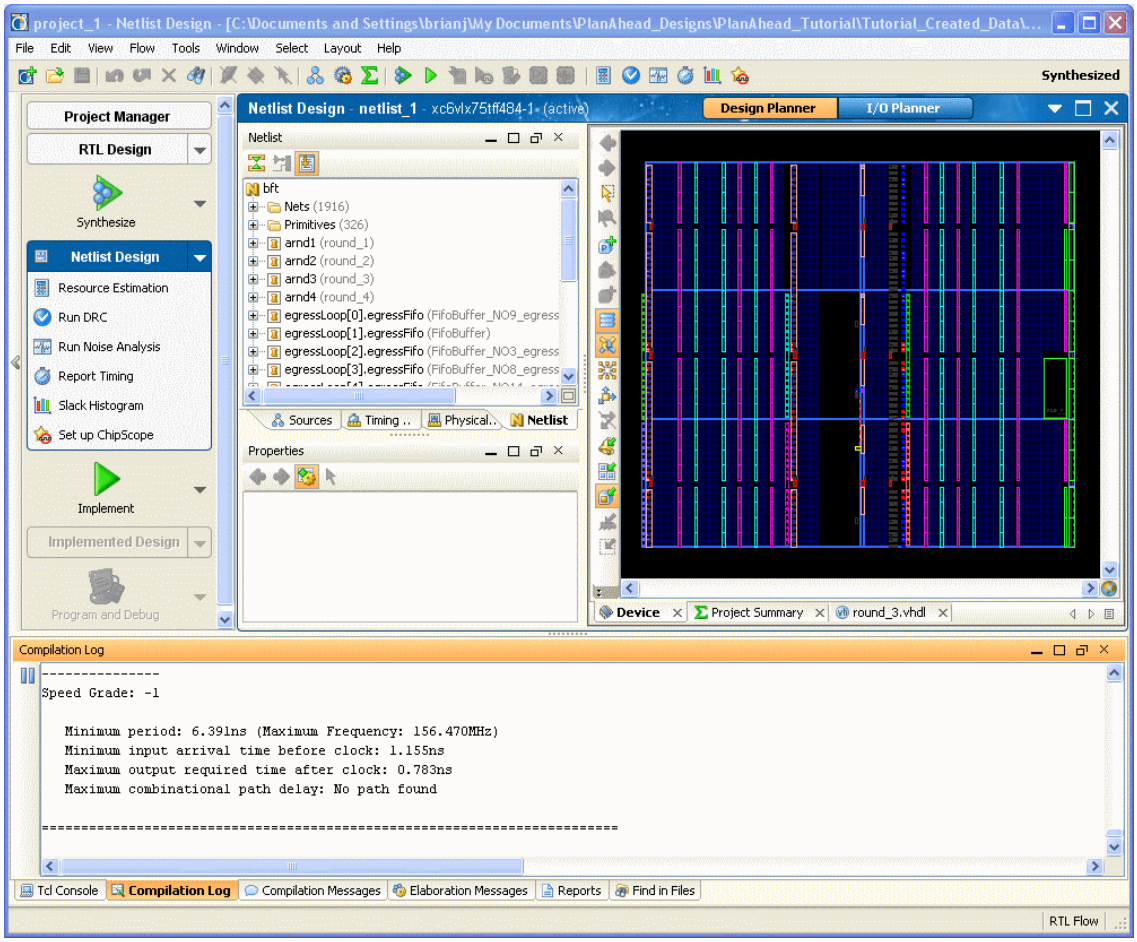

Figure 16: Opening the Netlist Design

Select the **Netlist Design** button in the Flow Navigator to open the Netlist Design environment.

PlanAhead provides a powerful design analysis and floorplanning environment to explore and experiment with the design. Using the PlanAhead analysis and floorplanning environment, you can experiment with various devices, timing constraints, or placement constraints. These capabilities are covered in other PlanAhead tutorials.

3-2-3. Examine the various views and information presented.

There are two view layouts available to help you perform different design tasks. The I/O Planner provides views to enable I/O pin exploration and constraint assignment. The Design Planner provides views to analyze the logic in the design and apply constraints.

3-2-4. Click the **I/O Planner** button in the Netlist Design view banner at the top of the PlanAhead environment.

Figure 17: Opening the I/O Planner View Layout

3-2-5. Examine the various views and information presented.

3-2-6. Click the **Design Planner** button in the Netlist Design view banner.

You can close the Netlist Design environment once your analysis and constraint definition completes. This helps preserve system memory and avoids having multiple editing environments open simultaneously. The Close button in the view banner or the pull down menu on the Netlist Design button in the Flow Navigator can be used to close the Netlist Design. We'll leave it open for the purposes of this tutorial.

3-3. View the XST report log file.

3-3-1. Click the **Reports** view tab at the bottom of the PlanAhead environment.

3-3-2. Double-click the **XST Report** to view the XST report in the Workspace.

3-3-3. Scroll through the XST report to examine it.

3-3-4. Close the XST report by clicking the **X** button in the Workspace tab.

Step 4: Implementing the Design Step 4

PlanAhead provides the flexibility for experimenting with implementation options. Multiple implementation Strategies can be applied to multiple runs to find the best performing results.

4-1. Explore Implementation options, launch implementation, and monitor a run.

4-1-1. In the Flow Navigator, expand the drop-down menu next to the Implement button and select **Implementation Settings**.

The Implementation Settings dialog box opens.

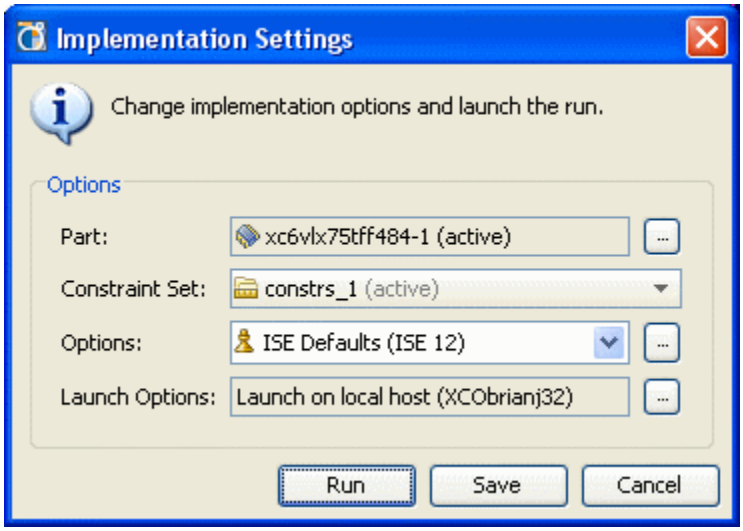

Figure 18: Implementation Settings Dialog Box

4-1-2. Use the default Part and Constraint Set.

4-1-3. Select the Options browser icon to display the Implementation Options dialog box.

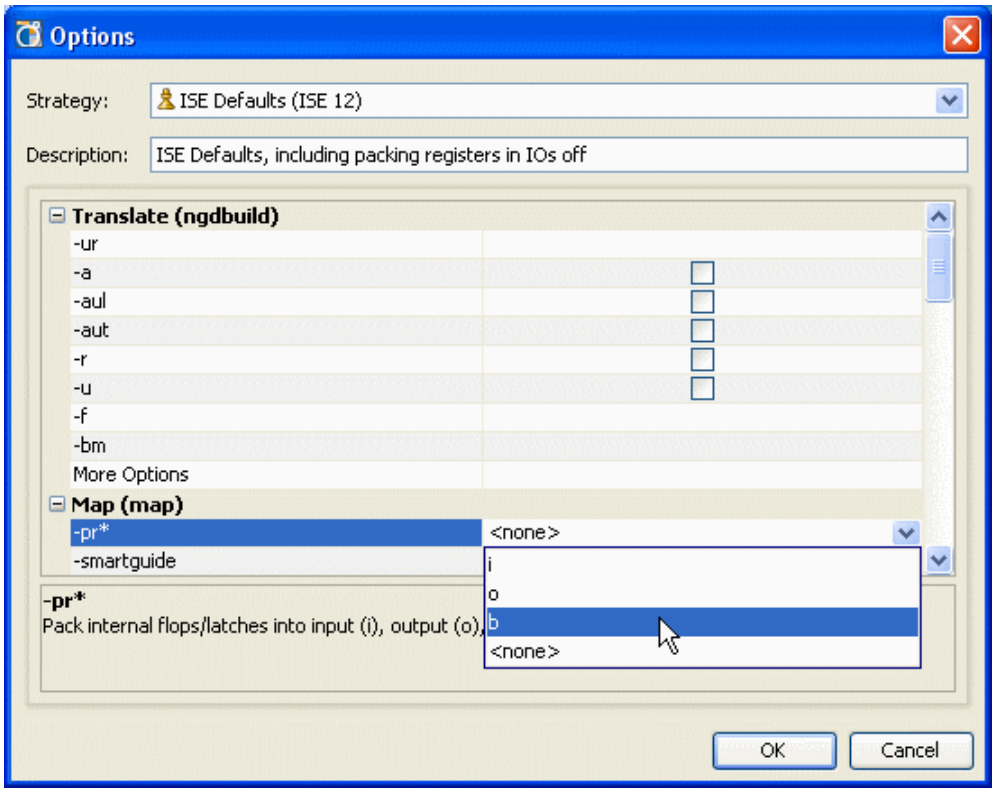

Figure 19: Implementation Options Dialog Box

4-1-4. Review the available options. Select the **Strategy** drop-down menu, review the available Implementation Strategies, and click **Cancel**.

4-1-5. Accept the Launch setting to **Launch Runs on Local Host**.

4-1-6. In the Implementation Settings dialog box, click **Run** to launch the run.

Notice the Status in the upper right corner displays `Implementing (Ngdbuild)` which indicates that ISE implementation is now running.

The Compilation Log view displays the output of the ISE commands while the Compilation Messages view displays a filtered list of Warnings and Errors.

4-1-7. After the Run completes, select the **Open Implemented Design** option in the Implemented Design dialog box.

4-1-8. Click **Yes** to close the Netlist Design before opening the Implemented Design.

Step 5: Analyzing the Results Step 5

PlanAhead enables placement and timing results to be imported quickly for analysis from any of the completed runs. PlanAhead imports placement and displays it in the form of “unfixed” LOC placement constraints. The *trce* timing results display in the Timing Results view.

Refer to other PlanAhead tutorials for more information about Design Analysis and Floorplanning.

5-1. Open the Implemented Design and briefly examine the results.

The PlanAhead environment displays with the Implemented Design loaded (Figure 20).

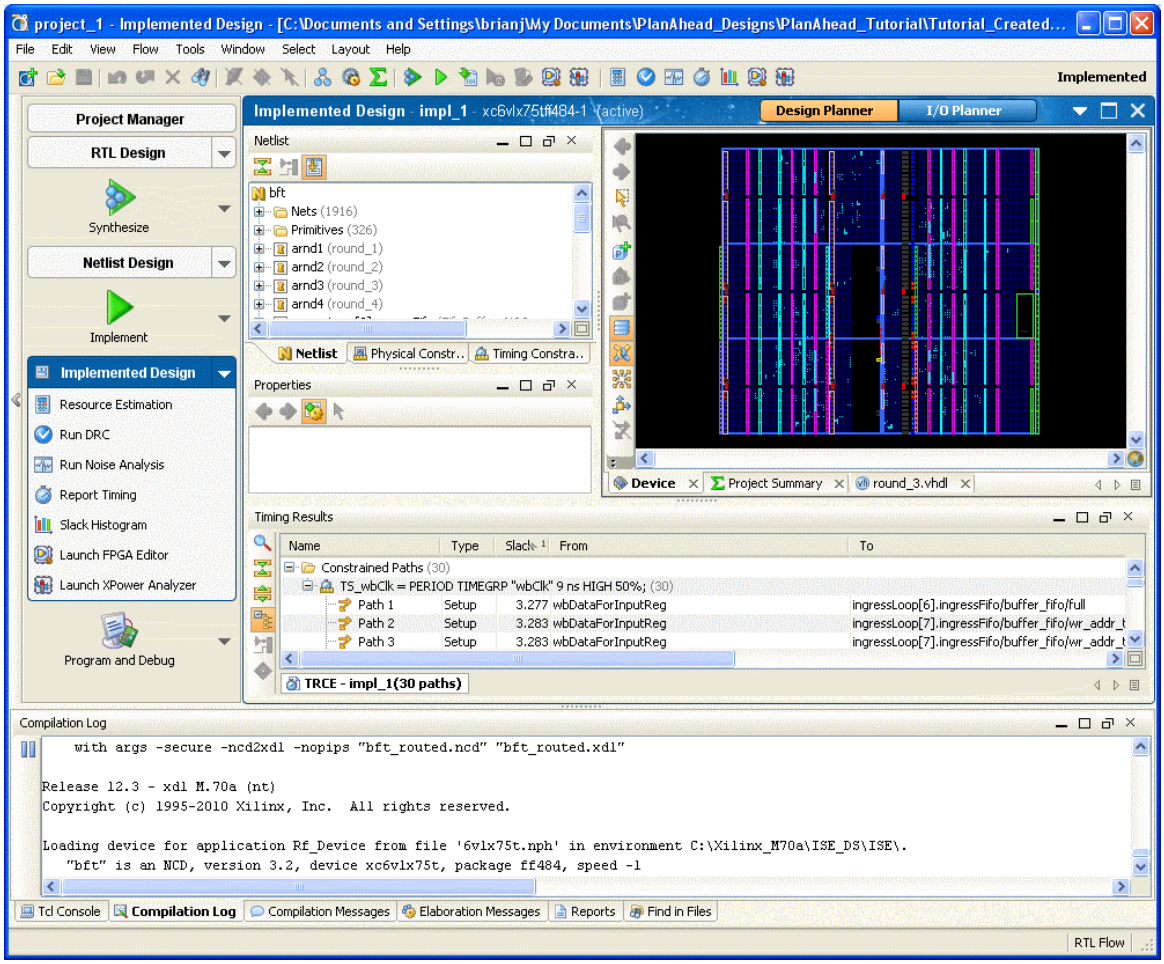

Figure 20: Opening the Implementation Results

Selecting the Implemented Design button in the Flow Navigator also opens the Implemented Design environment.

Notice the placement is imported into the Device view and the `trce` timing results are displayed in the Timing Results view. Your results might differ from the figure above.

5-1-1. Select the Reports tab and double-click on the MAP Report to view the Map report in the Workspace. Scroll through the Map report to examine it.

5-1-2. Close the Map report by clicking the **X** button in the Workspace tab.

5-1-3. In the Device view select the Hide/Show I/O Nets button  to turn on the I/O connectivity.

5-1-4. In the Device view select the Hide/Show I/O Nets button  to turn off the I/O connectivity.

5-1-5. In the Timing Results view, select the top timing path.

The path is highlighted in the Device view and the logic objects on the path are selected in other views.

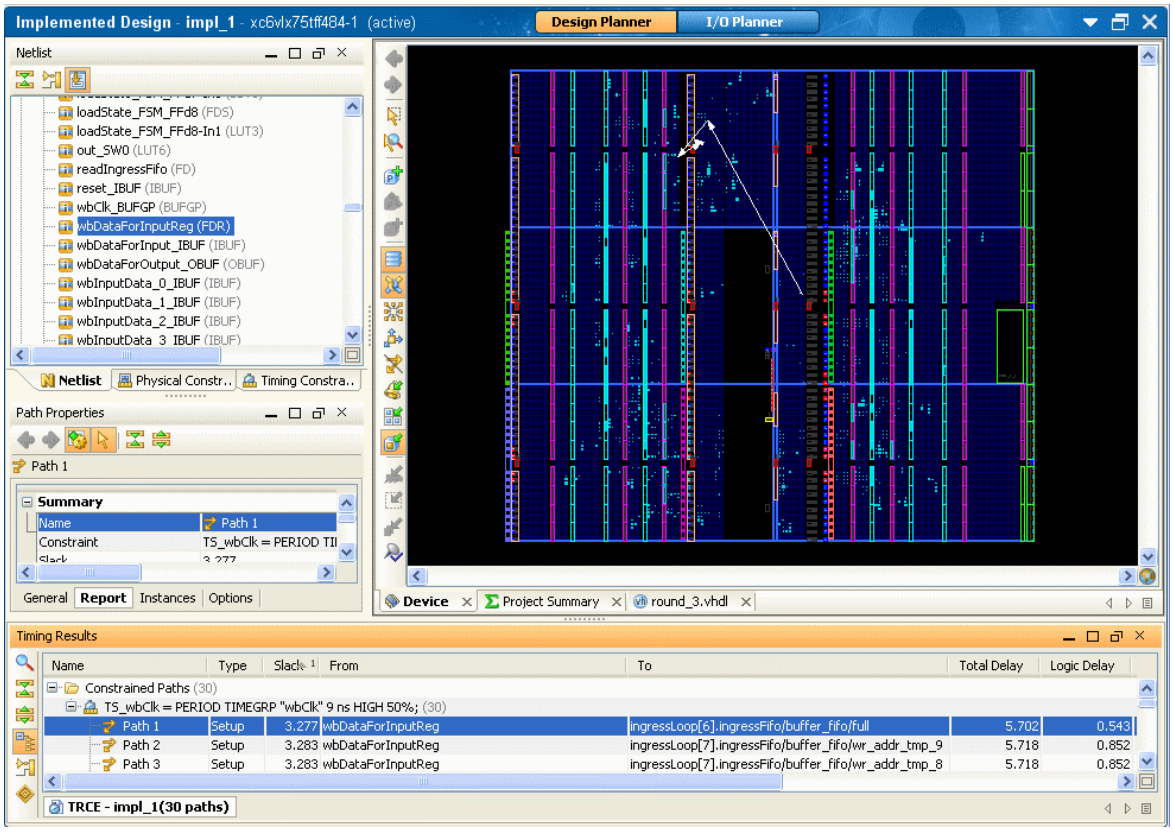

Figure 21: Highlighting Timing Paths from the Implementation Results

5-1-6. In the Path Properties view banner, select the Maximize button. 

The Path Properties view is displayed full screen (Figure 22).

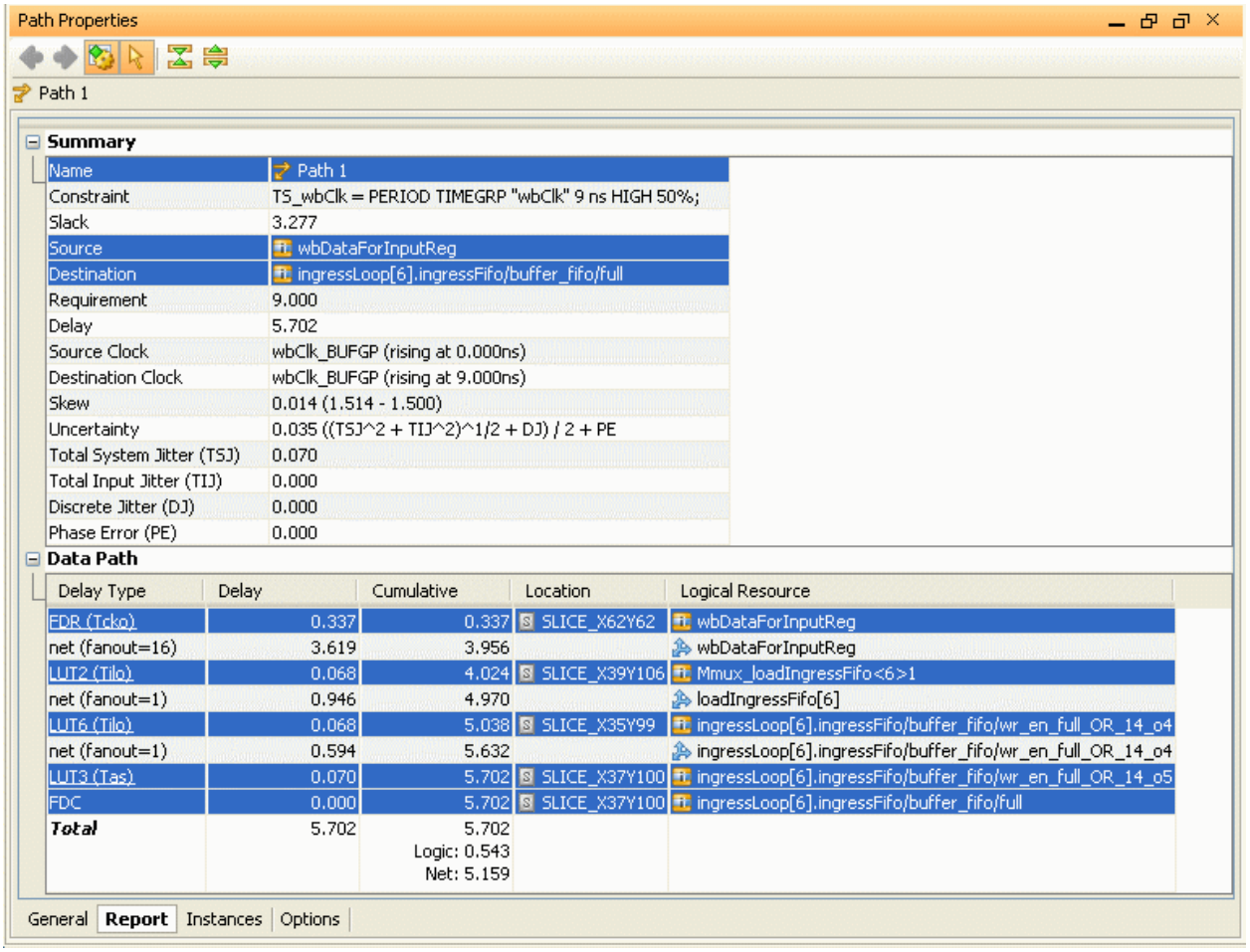

Figure 22: Viewing Path Properties

Notice the Path Properties report looks very similar to the trce report. Selecting any of the links selects the logic object or site.

5-1-7. Select the Restore button in the Path Properties view banner to bring the view back to the original location.

5-1-8. In the Timing Results view, select the Schematic command from the view toolbar or popup menu.

The Schematic view opens (Figure 23).

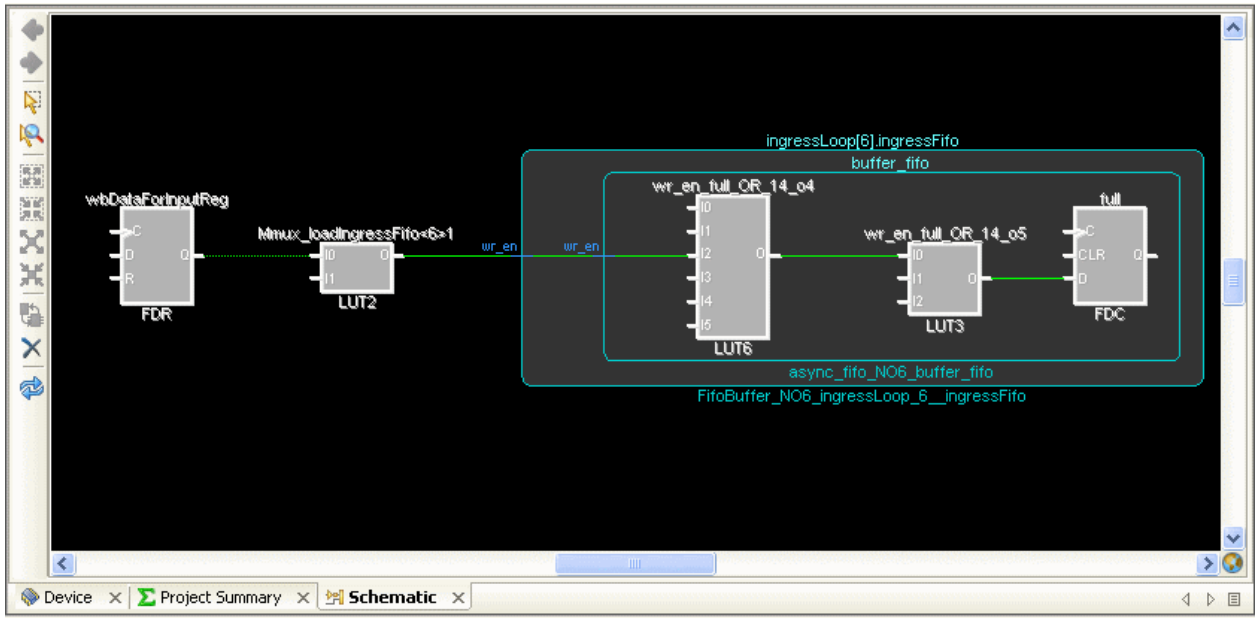

Figure 23: Viewing Timing Paths in the Schematic

Refer to other PlanAhead tutorials for more information about Design Analysis and Floorplanning.

Step 6: Creating the Bitstream File Step 6

6-1. Run the Generate Bitstream command to create a bit file for the design.

6-1-1. In the Flow Navigator, click the **Program and Debug** button to expand the menu and select **Generate Bitstream**.

The Run Bitgen dialog box opens.

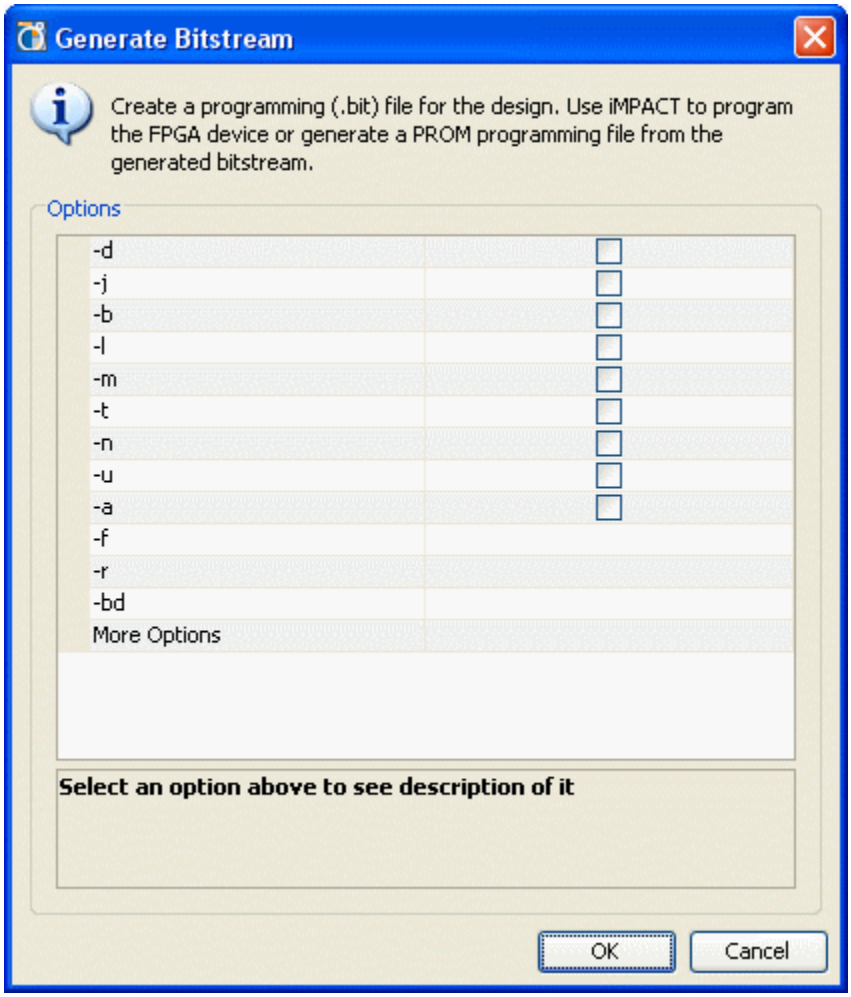

Figure 24: Generating Bitstream File

6-1-2. Select **OK** or **Cancel**.

6-2. Review the Project Summary for the Implemented Design.

6-2-1. Select the Project Summary view tab and review the information presented.

6-2-2. Close PlanAhead by selecting **File > Exit,** click **Yes** to save, and **OK**.

Conclusion

In this tutorial, you used a small PlanAhead RTL project to step quickly through the basic PlanAhead design flow. You started by creating an RTL project, and exploring RTL sources in the RTL editor. You then reviewed the various synthesis run options, ran synthesis, and imported the results by opening the Netlist design. You explored implementation options, and ran implementation. You monitored run results and viewed command report files. You then imported run results, and analyzed a timing path. Finally, you created a bitstream file.