Virtex-5 FXT FPGA Design Tools Known Issues

XTP032 (v1.0) March 31, 2008

This document describes known issues in the ISE® Design Suite 10.1 related to Virtex®-5 FXT FPGA features. If you are experiencing a problem in designing for the Virtex-5 FXT FPGA that is not documented here, please open a WebCase and submit a test case (if necessary) to reproduce the issue:

http://www.xilinx.com/support/clearexpress/websupport.htm.

Virtex-5 FXT FPGA-Related ISE Design Suite 10.1 Known Issues

- If using Synplify for design synthesis, Synplify v8.9 along with a patch must be used for Virtex-5 FXT support in ISE 10.1. See Xilinx Answer 30458.
- Xilinx Power Estimator (XPE) support for Virtex-5 FXT devices will be available in XPE 10.1 on April 15, 2008.
- Xilinx Power Analyzer (XPA) support for Virtex-5 FXT devices will be added in the ISE 10.1 Service Pack 2 release. See Xilinx Answer 30479.
- FXT-specific components will be added to the Software Libraries Guide coinciding with the ISE 10.1 Service Pack 2 release. Please see the Virtex-5 FXT FPGA User Guides for implementation information.
- When building a Virtex-5 FXT FPGA system in EDK with an SGMII or 1000Base-X PHY interface, a patch must be installed. See Xilinx Answer 30235.
- When connecting with GDB to PPC440, “Error: No Data on the Socket” occurs. Work-arounds are available. See Xilinx Answer 30550.
- See Xilinx Answer 30577 for Virtex-5 GTX RocketIO™ Wizard v1.2 Release Notes and Known Issues.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/31/08	1.0	Initial Xilinx release.