

Xilinx Power Estimator User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/05/07	1.0	Initial Xilinx release.
05/04/09	2.0	Added information to describe the XPE spreadsheets for the 11.1 release of ISE.
06/24/09	3.0	Updated with information to describe the XPE spreadsheets for the 11.2 release of ISE, and added references to Spartan-6 and Virtex-6 FPGAs.

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About This Guide

This document describes how to use the Xilinx Power Estimator (XPE) to arrive at realistic power consumption estimates for your design.

This guide also presents:

- Tool features that make design data entry, capture, and storage convenient,
- A detailed description of the various spreadsheet tabs that are a part of the tool, their purpose and usage, and
- Simple example circuits to illustrate usage of the tool.

Additional Resources

- To download the XPE spreadsheets, see the Power Solutions webpage on the Xilinx website at:
<http://www.xilinx.com/power>
- To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:
<http://www.xilinx.com/support>
- The following are especially pertinent to the subject of this User Guide.
 - ◆ WP353: *Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE)*
 - ◆ *Test Boards for Area Array Surface Mount Package Thermal Measurements*
 - ◆ Descriptions of the resources available in an FPGA can be found under **FPGA Device Families** at <http://www.xilinx.com/documentation>.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File →Open
	Keyboard shortcuts	Ctrl+C
Italic font	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = {on off}
Vertical bar	Separates items in a list of choices	lowpwr = {on off}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name loc1 loc2 ... locn;</i>

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details.
<u>Blue, underlined text</u>	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Xilinx Power Estimator User Guide

Introduction

The Xilinx Power Estimator (XPE) spreadsheet is a power estimation tool typically used in the pre-design and pre-implementation phases of a project. XPE assists with architecture evaluation and device selection and helps in selecting the appropriate power supply and thermal management components which may be required for your application.

XPE considers your design's resource usage, toggle rates, I/O loading, and many other factors which it combines with the device models to calculate the estimated power distribution. The formulas used for calculations in the program are based on intended behavior of various digital circuits. The device models are extracted from measurements, simulation, and/or extrapolation.

The accuracy of XPE is dependent on two primary components:

- Inputs you enter into the tool
- Device data models integrated into the tool

For accurate estimates of your application, enter realistic information which is as complete as possible. Modeling a certain aspect of the design over conservatively or without sufficient knowledge of the design can result in unrealistic estimates. Some techniques to drive the XPE to provide worst-case estimates or typical estimates are discussed in this document.

XPE is a preimplementation tool for use in the early stages of a design cycle or when the RTL description is incomplete. After implementation, the XPower Analyzer (XPA) tool (available in the ISE® Design Suite software) can be used for more accurate estimates and power analysis. For more information about XPA, see the XPower Analyzer Help.

XPE is a spreadsheet, so all Microsoft Excel functionality is fully retained in the writable or unprotected sections of the spreadsheet. XPE has additional functionality oriented to ease of use. The drop-down menus and the comment-enabled cells are helpful features to inform and guide you.

Getting Started with XPE

Opening XPE

1. XPE requires a licensed version of Microsoft Excel 2003 or later to be installed.
2. Download the latest available spreadsheet for your targeted device. The XPE spreadsheets are available here:
<http://www.xilinx.com/power>.
3. Make sure your Microsoft Excel settings allow macro executions. XPE uses several macros built into the XPE spreadsheet.
 - ◆ **Microsoft Excel 2003** - By default, the macro security level is set to High, which disables macros. To change the macro security level, follow these steps (actual menu names will vary with language of Microsoft Excel):
 - a. On the Tools menu, point to **Macro** and click **Security**.
 - b. In the Security dialog box, click the **Security Level** tab.
 - c. Select **Medium**, then click **OK**.
 - d. Open or, if already open, reopen the XPE spreadsheet.
 - e. When prompted whether to enable or disable macros, click **Enable Macros**.
 - ◆ **Microsoft Excel 2007 or Windows Vista** - The following steps are required:
 - a. From the Microsoft Office button select **Excel Options**.
 - b. In the Options dialog, click on **Trust Center**.
 - c. In the Trust Center dialog, click on **Trust Center Settings** and select the **Macro Security** tab.
 - d. Select **Enable all macros**, then click **OK**.
 - e. Open or, if already open, reopen the XPE spreadsheet.

Minimum Required User Input

Power estimation for programmable devices like FPGAs is a complex process, since it is highly dependent on the amount of logic in the design and the configuration of that logic. To produce accurate estimates, the power estimation process requires accurate input values, such as resource utilization, clock rates, and toggle rates. To use this tool to its minimum capability with reasonable accuracy, you need the following:

- A target device-package combination
- A good estimate of resources you expect to use in the design (for example, flip-flops, look-up tables, I/Os, block RAMS, DCMs, etc.)
- The clock frequency or frequencies for the design
- An estimate of the data toggle rates for the design

This minimum data is necessary but not sufficient to provide accurate estimates that aid an optimal choice of power supplies, regulators, and optional thermal solutions.

XPE Calculations and Results

XPE uses your design and environmental input, then combines this information with the device data model to compute and present an estimated distribution of the power in the targeted device.

XPE presents multiple views of the power distribution.

- **Static vs. Dynamic Power** - Static or Quiescent power represents the power drawn when the device is powered and programmed and there is no switching activity. This includes transistor leakage, power consumed internally, and power dissipated in external termination resistors. Dynamic power is the additional power consumed or sourced by the FPGA when the user logic is active. This description is typical for an FPGA technology based on CMOS SRAM transistors. By choosing the **Maximum** or **Typical** values for **Process**, worst-case or nominal power can be estimated.

Both the reported static and dynamic power estimates are modeled to account for temperature and voltage sensitivity. Ambient temperature and regulated voltage on the system can be keyed into the appropriate cells provided for the purpose.

- **Power by Voltage Supplies** - This view is useful to select the appropriate voltage supply sources since XPE breaks out the expected current per voltage source required. This view includes both off-chip and on-chip dissipated power.
- **Power by User Logic Resources** - For each type of user logic in the design, XPE reports the expected power. This allows you to experiment with architecture, resources, and implementation trade-off choices in order to remain within the allotted power budget.
- **Thermal Power** - XPE lets you enter device environment settings and reports thermal properties of the device for your application, such as the expected junction temperature. With this information you can evaluate the need for passive or active cooling for your design.

The following sections provide more details on how to enter settings and review results.

Definitions/Terminology

Supported Device Families

Separate spreadsheets are available depending on the targeted architecture.

Low Cost FPGA families:

- Spartan[®]-6 and Spartan-3A - This spreadsheet includes all sub-families (Spartan6 Low Power, Spartan-3AN, and Spartan-3A DSP)
- Spartan-3E
- Spartan-3

High Performance FPGA families:

- Virtex[®]-6 and Virtex-5 - This spreadsheet includes all sub-families (Virtex-6 Lower Power)
- Virtex-4

Note: Download spreadsheets from <http://www.xilinx.com/power>.

Note: Pre-design power estimation for CPLD and other architectures is described in the Power Solutions webpage on the Xilinx website (<http://www.xilinx.com/power>).

Device Model Accuracy

The accuracy of the characterization data existing in the tool is reflected by accuracy designations in the **Release** tab of XPE. For most FPGAs, the accuracy designation is also displayed in the **Summary** tab. The accuracy designations are Advance, Preliminary, and Production.

Advance

The data integrated into XPE with this designation is based primarily on measurements and characterization data made on early production devices. A set of widely used device resources are included in the characterization. Characterization data is limited to these few blocks. This data is typically available within a year of product launch. Although the data with this designation is considered relatively stable and conservative, some under-reporting or over-reporting might occur. Advance data accuracy is considered lower than the Preliminary and Production data.

Preliminary

The data integrated into XPE with this designation is based on complete early production silicon. Almost all the blocks in the device fabric are characterized. Data for most of the dedicated blocks like TEMAC and PCIe block are also characterized and integrated into the XPE. The probability of accurate power reporting is improved as compared to Advance data.

Production

The data integrated into XPE with this designation is released after enough production silicon of a particular device family member has been characterized to provide full power correlation over numerous production lots. Characterization data for all blocks in the device fabric is included.

Toggle Rates

A less intuitive step is to model the toggle rates for the various sections of the design or estimate an average toggle rate for the entire design.

- For synchronous paths, toggle rate reflects how often an output changes relative to a given clock input and can be modeled as a percentage between 0–100%. The max data toggle rate of 100% means that if the clock frequency is 100 MHz, a data toggle rate of 100% equates to a data frequency of 50 MHz. This convention stems from an assumption that a net with a 100% toggle rate toggles every active edge of a clock whose frequency is specified. This means that the LSB of a 16-bit counter toggles every clock cycle and the MSB toggles every 32,768th clock cycle.
- For non-periodic or event-driven state machine designs, toggle rates cannot be easily predicted. An effective method of estimating average toggle rates for a given design is to segregate the different sections of the design based on their functionality and estimate the toggle rates for each of the sub-blocks. An average toggle rate can then be arrived at by calculating the average for the entire design. Most logic-intensive designs work at around 12.5% average toggle rate, which is the default toggle rate setting in XPE. For a worst- case estimate, a toggle rate of 20% can be used. Average toggle rates greater than 20% are not very common. Arithmetic-intensive modules of a design seem to take toggle rates of up to 50%, which is representative of the absolute

worst case. An example of this would be a Multiply-Accumulate operation. It is also common to model toggle rate for random input data at 50%.

Note: Data toggle rate should be scaled by the Clock Enable rates. If data toggle rate is modeled at 50% but the synchronizing clock is enabled 50 percent of the time, the resulting toggle rate should be 25%.

To appreciate what 100% toggle rate means, think of a constantly enabled toggle flip-flop (TFF) whose data input is tied High. The T-output of this flip-flop toggles every clock edge. Very few designs could possibly have an average toggle rate that high (100%).

Fanout

Fanout defined in XPE is similar to the fanout reported by the synthesis tool and can differ from the fanout reported by the implementation tool. This difference is expected because fanout will vary with placement and packing of the logic.

- In XPE fanout represents the number of loads or logic elements the considered element is connected to (LUTs, flip-flops, block RAM, I/O flip-flops, distributed RAM, and shift registers).
- In the implementation tool (ISE PAR Report), fanout is the number of SLICES the considered net is routed to. A SLICE typically contains multiple logic elements and users generally do not control packing of the different elements into SLICES. For XPE, algorithms will estimate this packing before calculating the power.

User Interface

XPE has these spreadsheet tabs:

- The **Summary** tab lets you enter and edit all device and environment settings. This tab also displays a summary of the power distribution and provides buttons to import data into XPE and globally adjust settings.
- Other tabs allow you to enter usage and activity details for the different resource types available in the targeted device (for example, IO, Block RAM (BRAM), and Multi-Gigabit Transceivers (MGTs)).

Tip: XPE is intended to be intuitive to the novice spreadsheet-user. For information about a cell in the spreadsheet, move the mouse over the comment indicators (red triangle at the top right corner of the title cells) to read the relevant notes for the intended use (see [Figure 1](#)).

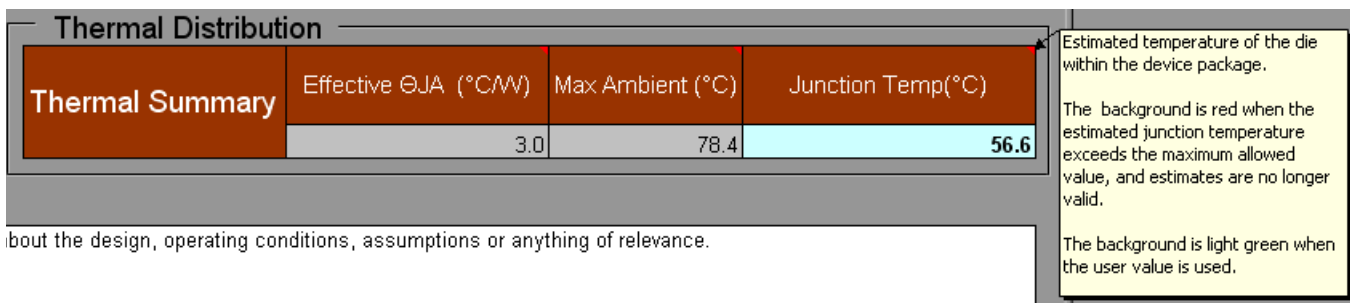


Figure 1: Comment Indicators and Comment

The XPE Toolbar

To make data entry into the tool easier, XPE supports importing data from different sources and allows settings to be changed globally. The toolbar is shown in [Figure 2](#).



Figure 2: XPE Toolbar

Import from ISE

When portions of the design have been implemented in ISE, you can use this button to import the exact resource count from ISE to get a more accurate power estimation of the total design. The imported MAP report fills in the XPE spreadsheet with device and resource count information reported by the MAP implementation stage.

Note: After import you must set clock frequencies, configuration, rates, and other usage information on each XPE tab. The clock, logic, DSP, and GT Tabs will have fanout and counts on a single line. The I/O and BRAM tabs are populated based on unique configuration. You may therefore need to add additional rows and adjust the counts to group by clock domain, module, or other functional grouping. Refer to White Paper [WP353: Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator \(XPE\)](#).

Note: Route-thru LUTs reported by MAP are not counted since their power is accounted for in the XPE interconnect model.

Note: Currently, only a single MAP report may be imported into XPE.

Import from XPE

Use the **import from XPE...** button when starting a new design which reuses previous IP blocks or when updating the design information into the latest spreadsheet version available. Clicking this button allows you to copy the contents of one XPE spreadsheet into another XPE spreadsheet.

Note: When the import is complete, make sure to verify and adjust the imported data if appropriate.

Note: You may need to open both the original and the new spreadsheets for the import function to succeed.

Advanced Options

You can force certain values which normally are calculated by XPE to perform worst case analysis. [Figure 3](#) shows these options. Entering values in the advanced option turns the background color of the affected cells in the **Summary** tab to light green. For most application there is no need to modify these settings.

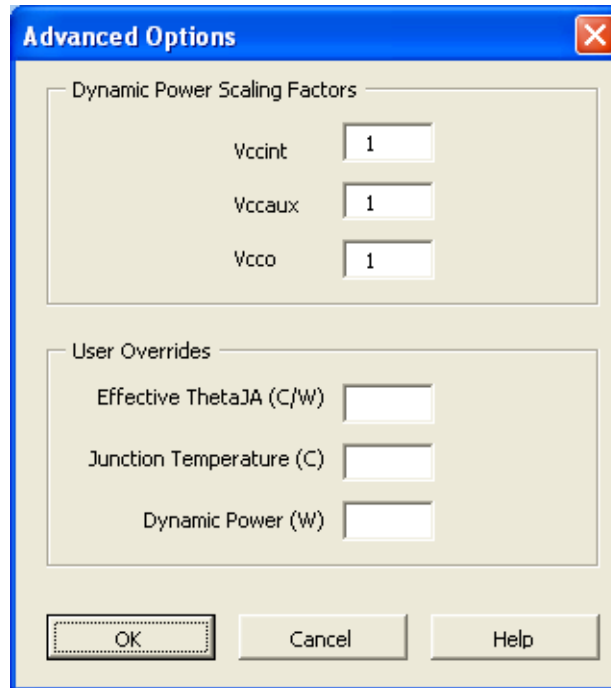


Figure 3: Advanced Options

The use model for each option is:

- **Dynamic Power Scaling Factors**

In this field you can enter a coefficient to scale the dynamic power on the Vccint, (dynamic), Vccaux, or Vcco power rails. This may be useful to enter margin when selecting a voltage regulator or cooling properties. This coefficient is applied on the dynamic power reported in the **Summary** tab and is also applied to the total power reported on the other tabs (where applicable). This option is recommended for advanced users only.

- **Effective ThetaJA (C/W)**

This coefficient defines how power is dissipated from the FPGA to the environment. Typically this option is calculated by XPE, taking into account, among other things, the different environment parameters in the **Settings** panel of the **Summary** tab. Entering a value in this field will override XPE calculations. Use this option if you have calculated this parameter value by simulations. You may also want to use this feature to factor out environmental parameters when analyzing power differences with another spreadsheet in which environment settings have been set differently.

- **Junction Temperature (C)**

This field forces the value of the device junction temperature. XPE then adjusts the ambient temperature to meet the specified junction temperature. This option could be used when you need to work backward from a known or assumed worst case junction temperature and define the minimum environment that would ensure this temperature is not exceeded.

- **Dynamic Power (W)**

This option forces the dynamic power to a specific value. This option may be useful when design logic content is not known at all. You can set a specific dynamic power

and work backwards using the options in the **Environment** section of the **Summary** tab to estimate which device and environment can support the power budget.

Reset to Defaults

The **Reset to Defaults** button resets all user settings to their default values, except for values in the **Device** selection table.

Set Toggle Rate

To set the default toggle rate that applies to the entire design, click the **Set Toggle Rate...** toolbar button on the **Summary** tab. The value is then propagated to all applicable spreadsheet tabs automatically. To learn more about toggle rates, refer to the section, [“Toggle Rates”](#).

Set Default Clock

To set the default clock rate that applies to the entire design, click on the **Set Default Clock...** toolbar button on the **Summary** tab. The value is then propagated to all applicable spreadsheet tabs automatically. To learn more about toggle rates, refer to the section [“Toggle Rates”](#).

XPE Cell Color-Coding Scheme

To simplify data entry and review, the XPE cells are color coded. A description of the spreadsheet’s color-coding scheme is provided in [Table 1](#).

Table 1: XPE Cell Color-Coding Scheme

Cell Color	Cell Use	Comment
White	Allows user to enter data	Writable/Editable. Rounded to 1 decimal place.
Grey	Displays a calculated value	Read / Write Protected. Cannot be edited or written into.
Cyan	Displays a summary value	Read-only
Light Green	User override of cells normally calculated by XPE	
Orange	Flags a warning. Indicates that a resource is not available.	Writable / Editable
Red	Flags an error. Examples of errors are: <ul style="list-style-type: none"> A resource limit in the device has been exceeded. The limits of a device specification (for example, junction temperature) have been exceeded. 	Error can be corrected by editing other cells in XPE.

Summary Tab

The **Summary** tab is the default tab on launch and allows you to enter all device and environment settings. On this page the tool also reports estimated power from a typical or worst case process. It also shows a power-rail-wise and block-wise breakdown of power consumption (see [Figure 4](#)).

Note: The Spartan-3, Spartan-3E and Virtex-4 spreadsheets have a slightly different layout for this tab. The description of the different user settings and data presented in this view is, however, applicable to these spreadsheets.

XILINX XPower Estimator (XPE) - 11.2
Virtex®-5, Virtex®-6

Buttons: Import from ISE..., Import from XPE..., Advanced Options..., Reset to Defaults, Set Toggle Rate..., Set Default Clock...

Settings

Device	
Family	Virtex-6
Part	XC6VLX240T
Package	FF784
Grade	Commercial
Process	Typical
Speed Grade	-1

Environment	
Ambient Temp (°C)	50.0
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom ΘSA (°C/W)	5.2
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom ΘJB (°C/W)	2.8
Board Temperature	

ISE	
Optimization	None

Characterization	
Advance Data:	Jun. 5, 2009

Power Distribution

Supply Summary		Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Source	Voltage			
V _{CCINT}	1.00	2.383	0.501	1.883
V _{CCAUX}	2.50	0.137	0.002	0.135
V _{CC0 3.3}	3.30	0.000	0.000	0.000
V _{CC0 2.5}	2.50	0.033	0.031	0.002
V _{CC0 1.8}	1.80	0.000	0.000	0.000
V _{CC0 1.5}	1.50	0.000	0.000	0.000
V _{CC0 1.2}	1.20	0.000	0.000	0.000
MGTAV _{CC}	1.00	0.057	0.057	0.000
-		-	-	-
MGTAV _{TT}	1.20	0.068	0.068	0.000
-		-	-	-

On-Chip Power (W)	
CLOCK	0.085
LOGIC	0.280
IO	0.095
BRAM	0.054
DSP	0.036
	-
MMCM	0.000
GT	0.172
TEMAC	0.000
PCIE	0.000
	-
Leakage (W)	2.225
Total (W)	2.948

Supply Power	Total (W)	Dynamic (W)	Quiescent (W)
	2.948	0.722	2.225

Thermal Distribution

Thermal Summary	Effective ΘJA (°C/W)	Max Ambient (°C)	Junction Temp(°C)
	3.0	76.1	58.9

Comments

This area is for the user to enter any comments about the design, operating conditions, assumptions or anything of relevance.

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[XPower Estimator User Guide](#)

Navigation: Summary | CLOCK | LOGIC | IO | BRAM | DSP | MMCM | GTX | TEMAC | PCIE | User | Graphs | Release

Figure 4: Summary Tab (Virtex-6) - Adjust Settings and Display Power Results

Settings Panel

Use the **Settings** panel to specify the exact device targeted and all the part environment settings which influence device power consumption. This panel varies slightly depending on the targeted device. A Virtex-6 example is presented in [Figure 5](#).

Settings	
Device	
Family	Virtex-6
Part	XC6VLX240T
Package	FF784
Grade	Commercial
Process	Typical
Speed Grade	-1
Environment	
Ambient Temp (°C)	50.0
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom Θ_{SA} (°C/W)	5.2
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom Θ_{JB} (°C/W)	2.8
Board Temperature	
ISE	
Optimization	None
Characterization	
Advance Data: Jun. 5, 2009	

Figure 5: Settings Panel (Virtex-6)

The sections in the **Settings** panel are:

- **Device**

Select the smallest device which meets your requirements.

Note: Larger devices exhibit higher quiescent power consumption.

- **Environment**

For XPE to report the estimated junction temperature it needs to understand how the device logic is configured and activated. It also needs a description of the device environment. The information of how heat can be transferred into the surrounding air (Θ_{SA}) or PCB (Θ_{JB}) affects the device junction temperature. If these parameters are known enter them; otherwise, select from the different drop down menus the

environment settings closest to your specific project. This will help to indirectly determine Effective Θ_{JA} .

For more details about the thermal parameters of the Xilinx Power Estimator, please refer to Chapter 3: Thermal Management & Thermal Characterization Methods & Conditions in the *Device Package User Guide* (UG112).

- **ISE**

ISE settings are available to focus the synthesis and implementation tools towards minimizing dynamic power. Specify in this area whether these settings are used and their expected effect. The levels are:

- ◆ **None** - Design implemented without any power optimization settings.
- ◆ **Typical** - Design implemented with power optimization and average improvement results expected.
- ◆ **Worst Case** - Design implemented with power optimization and least improvement results expected.

- **Characterization**

This section provides information regarding the accuracy of XPE device data models. Refer to the “[Device Model Accuracy](#)” section for details.

- **Power mode**

This setting allows you to review the estimated power for the different active and power down modes of the device. **Power Mode** is available for some device families (see [Figure 6](#)).

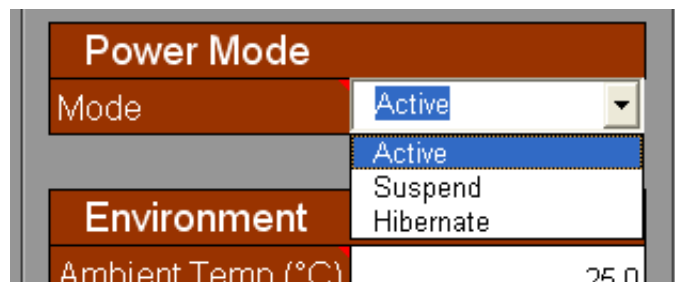


Figure 6: Power Mode Options (Spartan-6)

Power Distribution Panel

The **Power Distribution** panel displays the device estimated power in three different forms to enable detailed power analysis (see [Figure 7](#)).

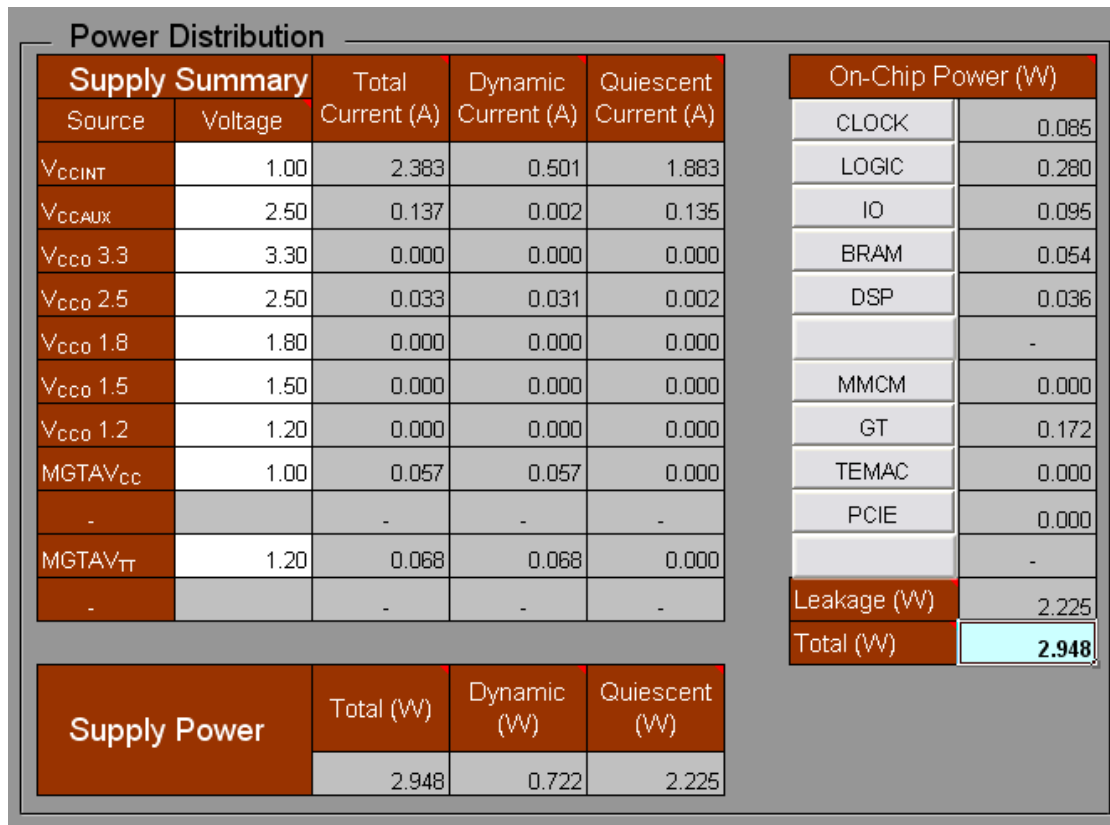


Figure 7: Power Distribution Panel (Virtex-6)

The sections in the **Power Distribution** panel are:

- **Supply Summary**

The **Supply Summary** table is organized by voltage rails. You can adjust individual voltages within the supported range and XPE will calculate and display the total current required. This information can be used to size or review voltage supply components, such as regulators.

Multiple power supplies are required to power an FPGA. For logic resources typically available in Xilinx FPGAs, [Table 2](#) presents the voltage source that typically powers them. This table is provided only as a guideline because these details may vary across Xilinx device families.

Note: FPGAs containing MGTs (Multi Gigabit Transceivers) have MGT-specific power supplies. For information, see the applicable MGT [User Guide](#).

Table 2: **FPGA Resources and the Power Supply that Typically Powers Them**

Power Supply	Resources Powered
V _{CCINT}	<ul style="list-style-type: none"> All CLB resources Most configuration SRAM cells All routing resources Entire clock tree, including all clock buffers Block RAM DSP blocks (DSP48, DSP48A, DSP48E)⁽¹⁾ All input buffers Logic elements in the IOB (ILOGIC/OLOGIC)⁽¹⁾ ISERDES/OSERDES⁽¹⁾ PowerPC™ processor⁽¹⁾ Tri-Mode Ethernet MAC⁽¹⁾ DCM (minor)
V _{CCAUX}	<ul style="list-style-type: none"> IODELAY/IDELAYCTRL⁽¹⁾ Differential Input buffers V_{REF}-based, single-ended I/O standards, e.g., HSTL18_I Clock Managers (DCM, PLL, PMCD)⁽¹⁾ Some Configuration memory
V _{CCO}	<ul style="list-style-type: none"> All output buffers Some input buffers Digitally controlled impedance⁽²⁾

Notes:

1. These resources are available only in certain device families. Refer to the appropriate data sheets and user guides for more information.
2. V_{CCO} in bank 0 (V_{CCO_0} or V_{CCO_CONFIG}) powers all I/Os in bank 0 as well as the configuration circuitry. See the applicable [Configuration User Guide](#).

• **Supply Power**

The **Supply Power** table displays the estimated total power across all voltage sources. Information is broken out between **Quiescent** and **Dynamic** power. The table includes all power required by the internal logic along with external power eventually sourced by the device, depending on the design IO configurations.

The quiescent and dynamic power are reported for the entire device and both are added up in the **Total** power box.

• **On-Chip Power**

The **On-Chip Power** table presents the total power consumed within the device. It includes quiescent, leakage and dynamic power and the total is broken out by resource type. This view can help determine the amount of power being consumed and dissipated by the device. It also helps identify potential areas in the design where power optimization techniques could be used to meet the targeted power budget.

Thermal Distribution Panel

The **Thermal Distribution** panel (see [Figure 8](#)) presents:

- the calculated device junction temperature,
- the maximum ambient temperature in which the device can operate without exceeding the maximum junction temperature specified in the device datasheet,
- the calculated Effective Thermal Resistance (**Effective Θ_{JA}**). This coefficient defines how heat is transferred from the die to the environment. The value is calculated from the settings entered in the **Environment** panel. If you have run simulations of the environment you may also override this value by clicking on the **Advanced Options** toolbar button.

This view helps review the need and sizing of the device cooling strategy.

Thermal Distribution			
Thermal Summary	Effective Θ_{JA} ($^{\circ}\text{C/W}$)	Max Ambient ($^{\circ}\text{C}$)	Junction Temp($^{\circ}\text{C}$)
	3.0	76.1	58.9

Figure 8: Thermal Distribution Panel (Virtex-6)

Clock Tab

An important factor in dynamic power calculation is the load capacitance that needs to be switched by each net in the design. Some of the factors in determining the loading capacitance are fanout, wire length, etc. With clocks typically having higher fanouts, the capacitance and therefore the power associated with clock nets can be significant and is thus reported in a separate worksheet tab (see [Figure 9](#)).

Clock Tree Power				
Name	Frequency (MHz)	Type	Fanout	Power (W)
No Power	0.0	Global	0	0.000
		Global	0	0.000
Static Power	0.1	Global	0	0.018
		Global	0	0.000
Dynamic + Static Power	100.0	Global	0	0.042
		Global	0	0.000
Global Utilization	6.3%	Total		0.060
Regional Utilization	0.0%			

Figure 9: Clock Tree Power Example (Virtex-5)

- Buffer **Type** Column

Xilinx devices have different types of buffers capable of driving the clock routing structures and these types are modeled within XPE. Refer to the applicable [Device User Guide](#) to select the appropriate buffer type.

[Figure 9](#) shows the **Global** type as an example.

- Clock **Fanout** Column

The number of synchronous elements driven by this clock.

Note: Because of its buffered interconnect structure, the clock tree has two components, a dynamic component and a static component. If the clock's frequency is zero, the dynamic power is also zero. Every clock net has a minimum, frequency-independent, fanout-insensitive static power component. This static power from enabling the clock tree can be seen by entering a small clock frequency value signifying that global buffers have been instantiated but have no loads (Fanout = 0).

Logic Tab

The **Logic** tab (see [Figure 10](#)) is used to account for the number of CLB resources, including LUTs, SRLs, LUT-based RAMs, and flip-flops estimated for use in the design. By implementing the pre-existing blocks that constitute a design, it is possible to accurately estimate resource utilization for the bulk of a design. Along with a designer's prior experience with Xilinx FPGA designs, these resource utilization estimates help to predict the logic power, which is typically the larger share of the dynamic power consumed in any design.

Note: If the design has already been implemented in the ISE tools, use the **Import From ISE** button to automatically import resource information into XPE. Refer to "[Import from ISE](#)" for details.

The default setting for **Toggle Rate** (12.5%) and **Average Fanout** (3) is based on an average extracted from a suite of real-world Xilinx customer designs. In the absence of a better estimate for your specific design, Xilinx recommends using the default setting.

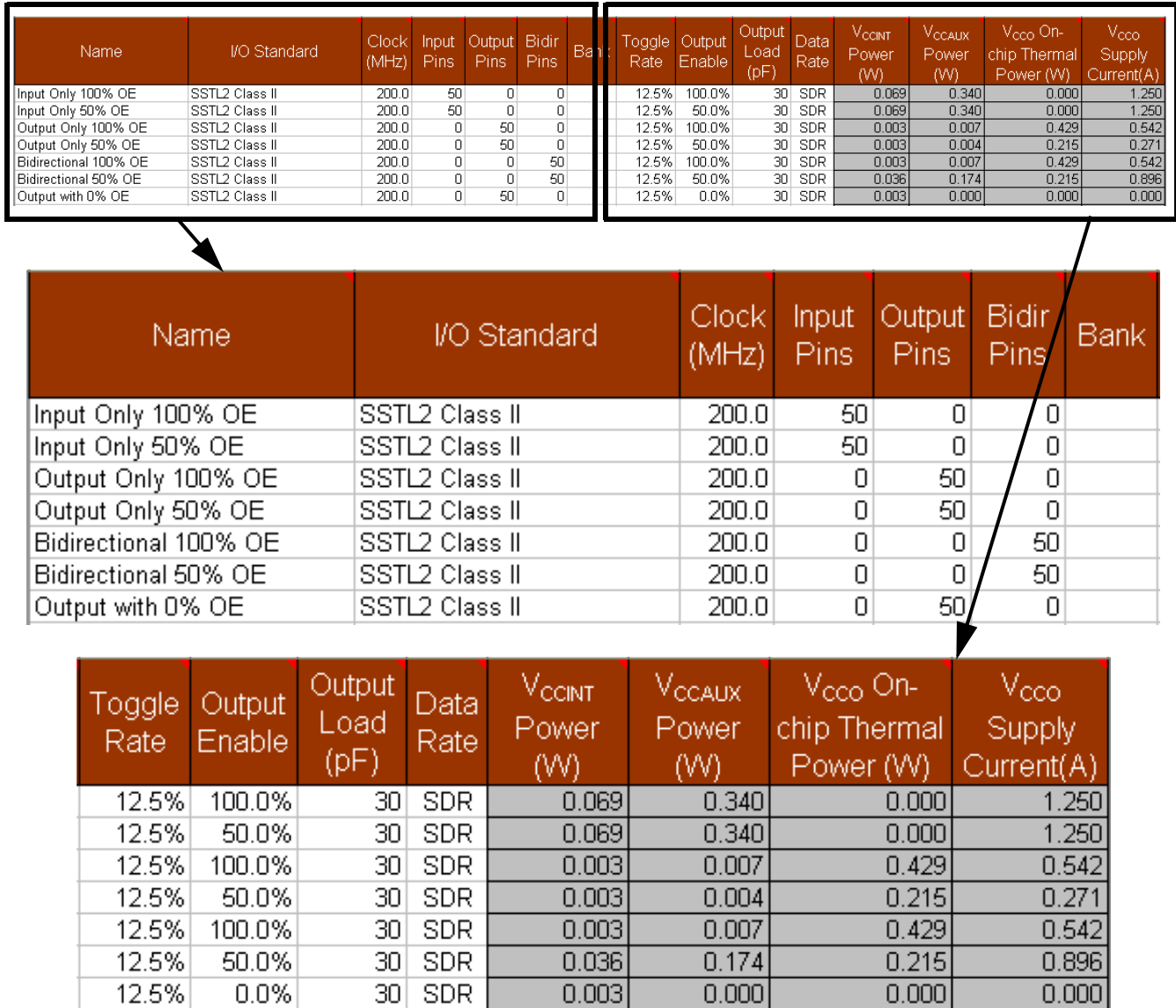


Figure 11: I/O Tab - Effect of Output Enable Rate on Power Estimates for Inputs, Outputs, and Bidirectional I/Os (Virtex-5)

- **I/O Standard and I/O Termination Columns**

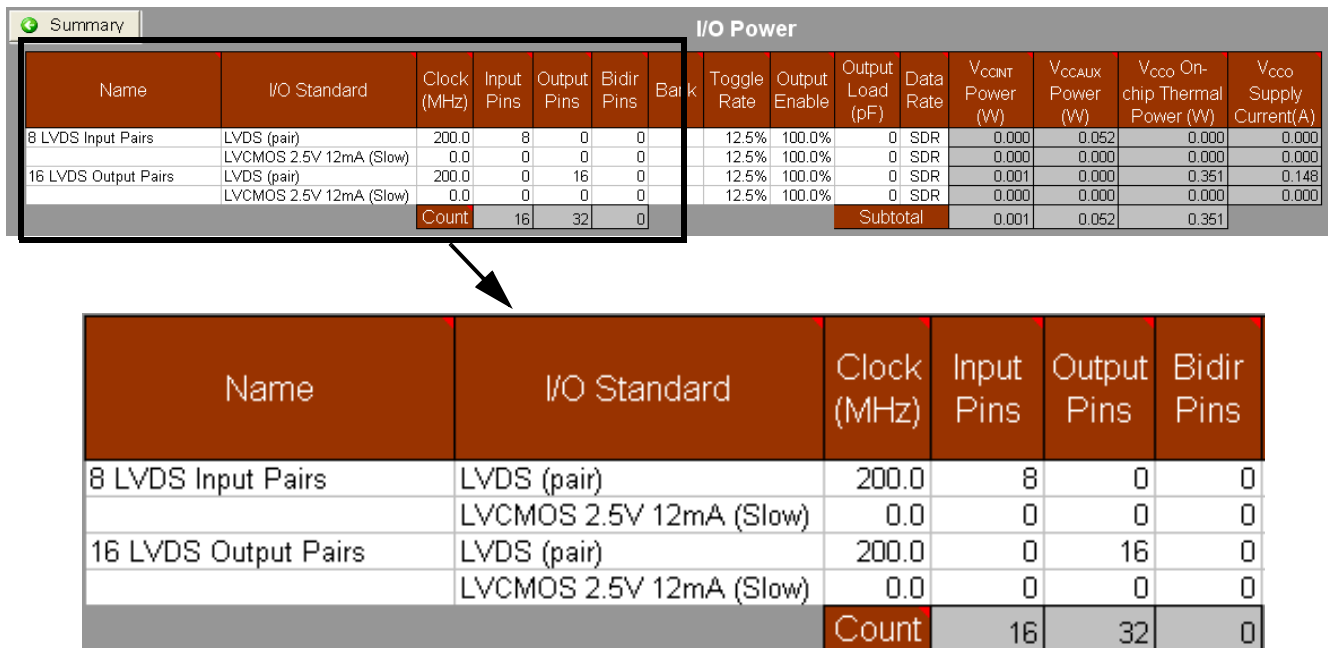
Different I/O standards have different termination requirements. A significant proportion of I/O power can be accounted for through I^2R loss in these terminations. I/O standards such as HSTL and SSTL require terminations to V_{TT} which can be an independent or derived power supply from V_{CCO} . The V_{CCO} supply current reported by XPE assumes that these terminations are as required by the I/O standard and that V_{TT} is derived from V_{CCO} . Refer to the applicable *User Guide* (listed in “Additional Resources”) for specific terminations recommended.

Some I/O standards (especially those that involve open drain drivers) can contribute no appreciable power draw from the V_{CCO} supply that powers the driver while drawing power from the receiver’s V_{CCO} . These drivers can potentially contribute only to the I^2R power loss rather than drawing any current from the driver’s V_{CCO} rail. As these I/Os contribute purely to the junction temperature estimate, XPE

additionally reports V_{CCO} on-chip thermal power which is only used in predicting junction temperature for the design.

XPE calculates the portion of V_{CCO} dissipated on-chip for thermal considerations. It also calculates the required supply current including current drawn into off-chip termination resistors.

For differential I/O standards such as LVDS, DIFF_HSTL, etc., enter the number of pairs of differential pins. For example, to model 8 LVDS input pairs (16 pins), enter 8 into the corresponding cell in **Input Pins** column. [Figure 12](#) shows a portion of an I/O Tab showing a differential pair count entry.



I/O Power														
Name	I/O Standard	Clock (MHz)	Input Pins	Output Pins	Bidir Pins	Bank	Toggle Rate	Output Enable	Output Load (pF)	Data Rate	V_{CCINT} Power (W)	V_{CCAUX} Power (W)	V_{CCO} On-chip Thermal Power (W)	V_{CCO} Supply Current (A)
8 LVDS Input Pairs	LVDS (pair)	200.0	8	0	0		12.5%	100.0%	0	SDR	0.000	0.052	0.000	0.000
	LVC MOS 2.5V 12mA (Slow)	0.0	0	0	0		12.5%	100.0%	0	SDR	0.000	0.000	0.000	0.000
16 LVDS Output Pairs	LVDS (pair)	200.0	0	16	0		12.5%	100.0%	0	SDR	0.001	0.000	0.351	0.148
	LVC MOS 2.5V 12mA (Slow)	0.0	0	0	0		12.5%	100.0%	0	SDR	0.000	0.000	0.000	0.000
Count									Subtotal		0.001	0.052	0.351	

Name	I/O Standard	Clock (MHz)	Input Pins	Output Pins	Bidir Pins
8 LVDS Input Pairs	LVDS (pair)	200.0	8	0	0
	LVC MOS 2.5V 12mA (Slow)	0.0	0	0	0
16 LVDS Output Pairs	LVDS (pair)	200.0	0	16	0
	LVC MOS 2.5V 12mA (Slow)	0.0	0	0	0
Count			16	32	0

Figure 12: I/O Power Tab - Differential Pair Count Entry

- **Toggle Rate** Column

Toggle rates for I/Os are typically in the range of 10 -15%. The default setting is 12.5%. The most conservative or worst-case I/O power estimates can be reasonably modeled using toggle rates of 30 -35%.

Block RAM Tab (BRAM)

To accurately set Block RAM parameters in XPE, a good understanding of device resources and configuration possibilities is recommended. This information is available in the BRAM section of the device family [Device User Guide](#). If implementation details for the block RAM are known, follow the guidelines described in the “[For Better Accuracy](#)” section. Otherwise, refer to “[Preliminary BRAM Estimates](#)”.

Note: Distributed RAM/ROM and SRL usage should be specified in the “[Logic Tab](#)”.

- **Enable Rate** column

The **Toggle Rate**, **Enable Rate**, **Clock** frequency, and number of **BRAMs** also should first be specified in the **BRAM** tab. Then use the **Enable Rate** to specify the percentage of time during which the block RAM ports are enabled for reading and/or writing. To save power, the RAM enable can be driven Low on clock cycles when the block RAM

is not used in the design. BRAM **Enable Rate**, together with **Clock** rate, are important parameters that must be considered for power optimization.

- **Write Rate** column

The **Write Rate** represents the percentage of time that each block RAM port performs write operations. The read rate is understood to be 100% – write rate.

[Figure 13](#) illustrates the effect of block RAM configuration modes and bit widths on power estimates.

Preliminary BRAM Estimates

If the exact block RAM types and modes to be used in the design are unknown, the best approach is to determine how many kilobytes of memory are needed in the design and use the appropriate number of basic 18k True dual-port RAMs. If the data width of memory access is known, select this from the drop-down menu for each port. Depth and width are the two most important characteristics of a memory.

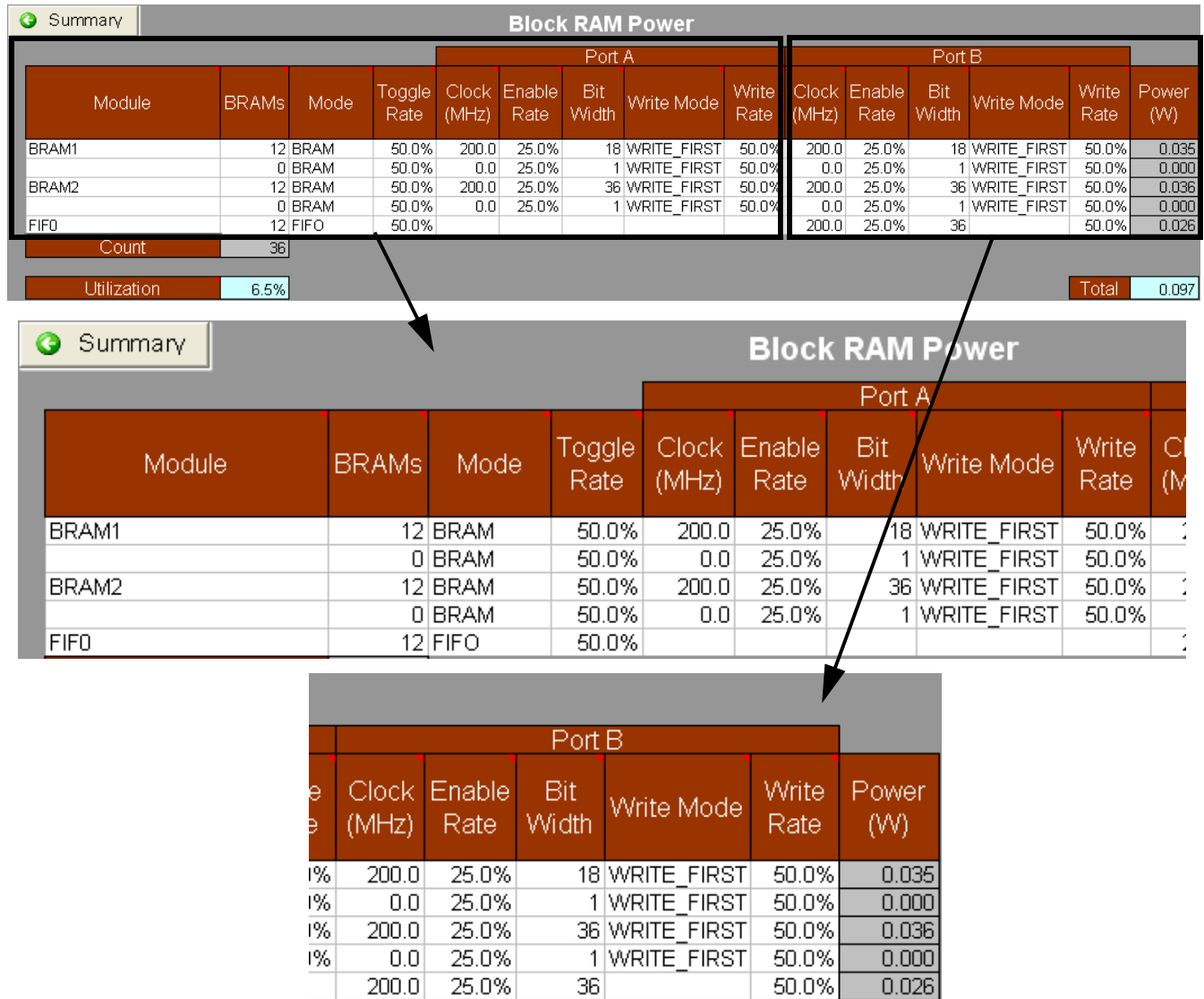


Figure 13: Block RAM Tab - Effect of Block RAM Configuration Modes and Bit Widths on Power Estimates (Virtex-5)

For Better Accuracy

If the breakdown of the memory usage of your design is known, the XPE spreadsheet allows you to specify which block RAM modes are being used. The **Mode** column has selectable values from a drop down menu that lists the different ISE primitive names and modes of the block RAM. Depending on the target family, this includes:

- **BRAM** - Simple dual-port or True dual-port Block RAM,
- **FIFO** - Dedicated built-in FIFO,
- **CASC (pair)** - Cascaded block RAM blocks (built from two RAM blocks),
- **ECC** - When the block RAM is configured in ECC mode.

In True dual-port mode the following data write mode options are available:

1. **WRITE_FIRST** – The port will first write to the location and then read out the newly written data.
2. **READ_FIRST** – The old data is first read out and then the new data is written in. This mode effectively allows 4 operations per clock cycle (saving power or resource utilization) – as the old data can be read out and replaced with new data on the same clock cycle of each port.
3. **NO_CHANGE** – When a Write happens the block RAM outputs remain unchanged.

Clock Management Resource Tabs (DCM, PMCD, PLL, MMCM)

Xilinx FPGA families have different clock generation and management capabilities. To enter information in these tabs, first review the *Device User Guide* to understand how to parameterize these resources in XPE. Depending on the step in the project development cycle you may or may not already know all the clocking details for your design. Enter what is known or can be estimated first, then later you can always reopen and complete the spreadsheet as design details become available.

Figure 14 shows a sample clock management resource tab (the **PLL Power** tab).

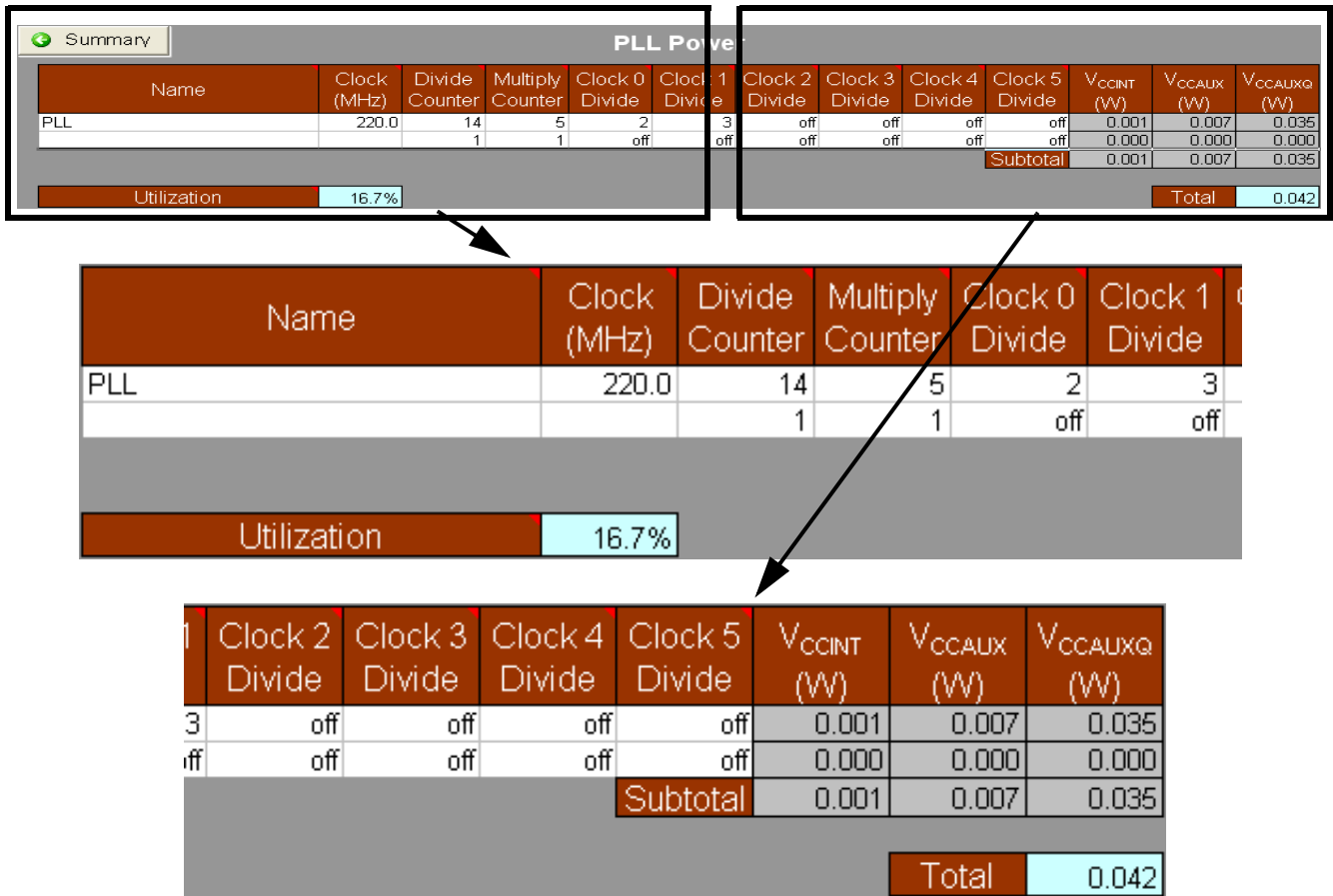


Figure 14: PLL Power Tab (Virtex-5)

DSP Tab (MULT, DSP48, DSP)

Xilinx FPGA families have different Digital Signal Processing (DSP) blocks with different capabilities. To enter information in these tabs first review the [Device User Guide](#) to understand the parameters in the DSP tab.

Tips:

- For random input data, a good **Toggle Rate** approximation for DSP operations is 50%. Clock enable rate must be factored into the data toggle rate, for example, if random data (50% data toggle rate) is input into the DSP slice and the slice is clock-enabled only 50% of the time, then the data toggle rate should be scaled by the CE rate such that the data toggle rate becomes 25% (50% x 50%). see [Figure 15](#) for a Virtex-5 example.
- For families which have a register within the multiplier (MREG), using this pipeline register helps lower dynamic power.

Name	DSP Slices	Clock (MHz)	Toggle Rate	MREG Used?	MULT Used?	Power (W)
DSP Random	10	100.0	50.0%	Yes	Yes	0.018
DSP Default TR	10	100.0	12.5%	Yes	Yes	0.005
DSP Max Frequency	10	500.0	12.5%	Yes	Yes	0.023
DSP No MREG	10	100.0	12.5%	No	Yes	0.005
Count	40					
Utilization	31.3%					
Total						0.050

Figure 15: DSP48E Power Tab (Virtex-5) - Effect of Clock, Toggle Rate, and MREG on Power Estimates

Multi-Gigabit Transceiver Tabs (MGT, GT, GTP, GTX)

Different Xilinx FPGA families have Multi-Gigabit Transceivers (MGT), which are very high performance serial I/Os. Transceivers typically use separate voltage supplies for the PCS, PMA and termination. To understand each family MGT capabilities and how to enter settings within XPE refer to the applicable [Transceiver User Guide](#).

To simplify data entry, drop-down menus are provided with parameter preferred or required values. [Figure 16](#) shows an example Virtex-5 FX70T design.

GTX_DUAL Power												
Name	GTXs	Data Rate (Gb/s)	Operational Mode	Data Path	TX O/P	VCO (GHz)	V _{CCINT} Power (W)	MGTAV _{CC} Power (W)	MGTAV _{CCPLL} Power (W)	MGTAV _{TTTX} Power (W)	MGTAV _{TTRX} Power (W)	
	4	3.20	Transceiver	10	500	3.2	0.080	0.234	0.154	0.104	0.097	
	4	6.50	Transceiver	10	800	3.25	0.163	0.236	0.156	0.109	0.097	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
		3.20	Transceiver	10	800	1.6	0.000	0.000	0.000	0.000	0.000	
Count	8						0.243	0.470	0.310	0.213	0.194	
Utilization	100.0%						Total	1.429				
Unused GTX_DUALs	Grounded											

Figure 16: GT Power Tab (Virtex-5) Illustrating Data Rate and Power Estimates

EMAC and TEMAC Tabs

Different Xilinx device families contain Tri-Mode Embedded Ethernet Media Access Controller (MAC) blocks, which are used in Ethernet applications. The Ethernet MACs are paired within a TEMAC block, share a common host and DCR interface, but are independently configurable to meet all common Ethernet system connectivity needs. Refer to the applicable EMAC *User Guide* for a detailed description of the block capabilities and configuration.

In XPE, you need only enter the EMAC operating clock frequency (See Figure 17). You typically need to know the mode and operating speed to obtain the correct clock frequency.

TEMAC Power		
Name	Core Clock (MHz)	Power (W)
1Gbps_Ethernet	125.0	0.019
		0.000
		0.000
		0.000
Utilization	25.0%	0.019

Figure 17: TEMAC Power Tab (Virtex-5)

PCIE Tab

Different Xilinx device families have Integrated Endpoint Block for PCI Express® designs (integrated Endpoint block). For detailed PCIE information, refer to the applicable PCIE [User Guide](#) and enter in XPE the settings which correspond to your application.

Summary					PCI Express Power				
Name	Core Clock (MHz)	User Clock (MHz)	Number of Lanes	Power (W)					
PCI Express	250.0	62.5	2	0.309					
			1	0.000					
			1	0.000					
			1	0.000					
Utilization		33.3%			Total		0.309		

Figure 18: PCIE Power Tab (Virtex-5)

PPC405 and PPC440 (PowerPC) Tabs

Some Xilinx FPGA families contain high-performance PowerPC® microprocessor embedded blocks.

For power estimation, these blocks are represented in a separate tab within XPE. Details for each PowerPC's settings are available in the applicable [Device User Guide](#). Typically you can provide the processor main clock frequency along with details of the processor local bus, memory and eventual DMA controllers. [Figure 19](#) presents a Virtex-5 example.

Note: Selecting **Maximum** for the **Process** in the **Summary** tab of XPE will estimate the worst case power consumption of the processor embedded block.

Summary								PPC440 Power							
Name	PPC440 Clock (MHz)	Interconnect Clock (MHz)	DMA 0 Clock (MHz)	DMA 1 Clock (MHz)	DMA 2 Clock (MHz)	DMA 3 Clock (MHz)	Power (W)								
PPC440	250.0	125.0	125.0				0.414								
							0.000								
Utilization		50.0%						Total		0.414					

Figure 19: PPC440 Power Tab (Virtex-5)

Conclusion

The ability to estimate power consumption in a design is imperative for efficient part selection, board design and system reliability.

The Xilinx Power Estimator tool with its up to date power models and ease of use features is meant to guide and simplify design utilization entry. Although gathering FPGA utilization data may seem difficult in the early design development phases, with a little thought and using XPE, accurate power estimations can be derived. XPE simplifies device selection and helps parallel development of the FPGA logic and the Printed Circuit Board.

