Course Description
This course demonstrates how to use the Vivado® Design Suite to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow.
This course covers both the tool flow and mechanics of successfully creating a PR design. It also describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications.

Level – FPGA 4  
Course Duration – 1 day  
Price –  
Course Part Number – FPGA-PR-ILT  
Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need of partial reconfiguration techniques  
Prequisites  
- Essentials of FPGA Design course  
- Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints course  
- Advanced Tools and Techniques of the Vivado Design Suite course  
- Working HDL knowledge (VHDL or Verilog)  
Software Tools  
- Vivado Design or System Edition 2015.1 with PR license  
Hardware  
- Architecture: 7 series FPGAs*  
- Demo board: Kintex®-7 FPGA KC705 board  
* This course focuses on the 7 series architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:  
- Build and assemble a Partially Reconfigurable system  
- Define PR regions and reconfigurable modules with the Vivado Design Suite  
- Generate the appropriate full and partial bitstreams for a PR design  
- Identify how Partial Reconfiguration affects various silicon resources, including block RAM, IOBs, fabric, and MGTs  
- Implement a Partial Reconfiguration system using the following techniques:  
  - Direct JTAG connection  
  - Floorplanning  
  - Timing constraints and analysis

Course Outline
- Course Introduction  
- Partial Reconfiguration Methodology  
- Demo: Partial Reconfiguration Flow  
- Partial Reconfiguration Tool Flow  
- Lab 1: Partial Reconfiguration Flow  
- Partial Reconfiguration Design Recommendations  
- Lab 2: Floorplanning  
- Partial Reconfiguration Bitstreams  
- Managing Timing

Lab Descriptions
- Lab 3: Partial Reconfiguration Timing Analysis and Constraints

Lab Descriptions
- Lab 1: Partial Reconfiguration Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- Lab 2: Floorplanning – Illustrates how to create efficient Pblocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.

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