Designing with the Virtex-5 Family

Course Specification

Course Description

Interested in learning how to effectively utilize Virtex®-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed Essentials of FPGA Design and Designing for Performance, this course focuses on understanding as well as designing into several of the resources found in this popular device.

Topics covered include a Virtex-5 FPGA overview, the CLB, DCM and PLL, global and regional clocking techniques, memory, DSP and arithmetic logic, and source-synchronous resources. The resources available in the LXT and SXT platforms (EMAC, the PCI Express® architecture, and GTP transceivers) are also discussed. In addition, you will learn about the resources included in the TXT and FXT platforms (GTX transceivers and the PowerPC® processor). A combination of modules and labs allow for practical hands-on application of the principles taught.

Prerequisites
- Essentials of FPGA Design course
- Designing for Performance course

Software Tool
- Xilinx ISE® Design Suite: System Edition 11.1

Hardware
- Architecture: Virtex-5 FPGA*
- Demo board: None*

*This course focuses on the Virtex-5 architecture. Check with your local Authorized Training Provider for specifics or other customizations.

Course Outline

- Introduction
- Virtex-5 FPGA Overview
- CLB Resources
- Clocking Resources
- Lab 1: Clocking Resources
- I/O Resources
- Memory Resources
- XtremeDSP Solution Resources
- Lab 2: DSP48E Resources
- Virtex-5 LXT, SXT, FXT, and TXT FPGA Overview
- Lab 3: (Optional) DSP48E Resources

Level – FPGA 3
Course Duration – 1 day
Course Part Number – V5-21000-11-ILT

Who Should Attend? – For those who have taken the Essentials of FPGA Design and Designing for Performance courses.

Register Today

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