VIVA23000-ILT (v1.0)

Course Description
This course offers detailed training on the Vivado™ software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

Level – FPGA 3
Course Duration – 2 days
Course Part Number – VIVA23000-ILT
Who Should Attend? – FPGA designers with intermediate knowledge of HDL and FPGA architecture, and some experience with the Xilinx Vivado Design Suite

Prerequisites
- Essentials of FPGA Design course or equivalent knowledge of FPGA architecture features; the Vivado software flow; basic FPGA design techniques; basic clock, input, and output timing constraints, and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Optional Videos
- Basic HDL Coding Techniques (parts 1 and 2)*
- Power Estimation*

Software Tools
- Vivado System Edition 2012.2

Hardware
- Architecture: 7 series FPGAs**
- Demo board: None**

* Go to www.xilinx.com/training and click the FPGA Design link under Online Training to view these videos.
* This course focuses on the 7 series architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:
- Use good alternative design practices to improve design reliability
- Increase performance by utilizing FPGA design techniques
- Describe the details of Vivado IDE database objects
- Identify Tcl commands for interacting with the database
- Apply complete Xilinx design constraints (XDC), including timing exceptions, false paths, and multi-cycle path constraints
- Utilize static timing analysis (STA) to analyze timing results
- Pinpoint design bottlenecks by using appropriate timing reports
- Apply advanced I/O timing constraints to meet performance goals
- Describe different synthesis options and how they can improve design performance

Course Outline
Day 1
- Review of Essentials of FPGA Design
- FPGA Design Techniques
- Accessing the Design Database
- Lab 1: Vivado IDE Database

Day 2
- Static Timing Analysis and Clocks
- Lab 2: Vivado Clocks

Lab Descriptions
- Lab 1: Vivado IDE Database – Explore the Vivado IDE database using Tcl commands. Use the Tcl Console to evaluate and enter IOB properties.
- Lab 2: Vivado IDE Clocks – Create complete XDC constraints for the clocking resources in a design. Implement the design and use the available clocking reports to verify results.
- Lab 3: I/O and Timing Exceptions – Create I/O timing constraints for a source-synchronous design and make path-specific timing constraints and false path constraints. Evaluate timing reports to determine the ability of the tools to meet timing objectives.

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