



RFSoc Frequency Planner Quick Start Guide

Version 2.1
July 2023

Content

[Revision History](#)

[Overview](#)

[General Assumptions, Conventions, and Limitations](#)

[Signal Power Calculations](#)

[GUI Overview](#)

[DAC Simulation Quick Start](#)

[ADC Simulation Quick Start](#)

[PLL Simulation Quick Start](#)

[Export Time Domain Samples](#)

[Advanced Menu Options](#)

[Export Config to Vivado Preset](#)

[Other Usage Notes and Tips](#)

[Important Legal Notices](#)

Revision History

Version	Date	Changes
1.0	Dec 22, 2021	Initial Release
2.0	April 20, 2022	Enabled DAC power measurement to show 5 digits
		Fixed sampling rate tooltip content
		Increased DPD 5th order and 7th order by 5dB
		Added PLL simulation tab
		Fixed DAC DUC bypassed mode HD2/HD3 location
		Added filter response overlay to all blocks with filtering
		Added additional tooltips to most fields and blocks
		Changed ADC DSA and RF power input relationship
		Added external PLL requirement warning for DAC Fs outside internal PLL range
		Enhanced data saturation error messaging and Fs outside device range warning
		Added 'real/cplx' indicator to each of the DAC and ADC stages
		Changed usage notes to quick start guide pdf
2.1	July 15, 2023	Added NZ lines to ADC RF input spectrum
		Added Custom input signals for ADC and DAC, and ability increase # of carriers from 4 to 16
		Added feature to export time domain data for each of the DAC or ADC sub blocks
		Added feature to export tcl file for Vivado RFDC IPI preset/configuration
		Made all input signals coherent
		Fixed some minor bugs and cosmetics
		Added combined frequency response plot for Inv-Sinc and DAC's Sinc response

Overview

- ▶ The RFSoc Frequency Planner is made available by AMD for RFSoc device users to simulate high-level behavior of the RF Data Converters to assist in choosing a suitable frequency plan and device configuration for the target use case.
- ▶ It does not model the analog performance of the data converters; the performance metrics such as HD2/3, NSD, etc., are intended to be inputs from the user. Default values are provided for ease of getting started.
- ▶ Only impairments typically applicable to frequency planning are included.
- ▶ It is not intended to reflect or guarantee precise RF performance of the Data Converters. For specific device specification please refer to the datasheet and associated documentation for the device at <https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html>.
- ▶ The simulated result is an approximate prediction of the data converter behavior; this in turn allows the user to run through various configuration scenarios quickly.
- ▶ It's highly recommended that the user validate the configuration of choice with the actual hardware. This can be carried out with the various RFSoc evaluation boards offered by AMD Xilinx.
- ▶ The three main features of the Frequency Planner are
 - to visualize location of signals and impairments of the data converters in the time and frequency domain for optimal selection of sampling rate and operating band placement.
 - to examine the signal level and characteristics of each sub-block of the data converter tile for proper signal scaling in the system.
 - to estimate the internal PLL phase noise performance with a given phase noise performance of the reference oscillator input.

General Assumptions, Conventions, and Limitations

- ▶ All digital filters in the DAC and ADC digital processing blocks use the same filter coefficients as in the actual hardware; the blocks include:
 - For DAC: P/Q Resampler, DUC Interpolation, Image Reject Filter, and Inverse Sinc.
 - For ADC: DDC Decimation, and P/Q Resampler.
- ▶ Signal level units are always in dBFS (dB full scale) for digital signal and dBm for analog RF signal.
 - For DAC: All blocks are in dBFS except for the DAC output, which is in dBm.
 - For the ADC: All blocks are in dBFS except for the ADC input, which is in dBm.
 - See [Signal Power Calculations](#) slide for detail calculation methods.
- ▶ Signal source for ADC and DAC are generated with bandlimited AWGN except for CW tones.
 - Band limited signals are not standards specific; they are generated with random data for each run / update.
 - BW (bandwidth) should be set to 0 for CW (continuous wave) tones.
 - The minimum supported signal bandwidth is 5MHz, maximum bandwidth is 85% of input Nyquist bandwidth. Small signal bandwidth will require longer run time. Smaller RBW for the spectrum plot (resolution bandwidth) will also lengthen the run time.
- ▶ Computer Monitor with 1080P resolution (with 100% scaling) or better is recommended for best user experience.
- ▶ PLL phase noise simulation result is for typical value only. Result over PVT will be in a banded range. Consult your local AMD Xilinx FAE for PVT characterization report of internal PLL performance.

General Assumptions, Conventions, and Limitations

- ▶ All sampling rates and frequency units are in Msps or MHz unless otherwise noted.
- ▶ DAC output only supports frequency domain and CCDF plot, time plot is not applicable. Use the Inverse Sinc stage output to view the time plot instead.
- ▶ CCDF of the DAC RF output is computed on the complex RF envelope of the signal, which has a 3dB PAR reduction from the real digital signal from the Inverse Sinc stage prior.
- ▶ Power measurement is only valid for the DAC output stage under the DAC panel. It's valid for all stages under the ADC panel.
- ▶ NSD is always added to the signal, regardless of the Enable status; however, the value can be changed.

Signal Power Calculations

▶ dBFS (dB Full Scale) convention for DAC

- Both RMS (root mean squared) and peak power are calculated for each digital block outputs X_{out} , and always referenced to a full scaled complex CW. The formula used is as follows.
 - $Power_{rms}(dBFS) = 20 * \log_{10} \left(rms \left(\frac{X_{out}}{2^{15}} \right) \right)$
 - $Power_{peak}(dBFS) = 20 * \log_{10} \left(\max(abs \left(\frac{X_{out}}{2^{15}} \right)) \right)$
- A complex CW $X_{out}(N) = 2^{15} * e^{2 * \pi * i * \frac{f_c}{f_s} * N}$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = 0dBFS$
- A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = -3dBFS$ and $Power_{peak} = 0dBFS$

▶ dBFS (dB Full Scale) convention for ADC

- Keeping with ADC full scale convention, blocks with real output (i.e., ADC Core, QMC), full scale is referenced to a full scaled real CW signal and calculated as follows.
 - $Power_{rms}(dBFS) = 20 * \log_{10} \left(rms \left(\frac{X_{out}}{2^{15} * \sqrt{\frac{1}{2}}} \right) \right)$
 - $Power_{peak}(dBFS) = 20 * \log_{10} \left(\max(abs \left(\frac{X_{out}}{2^{15} * \sqrt{\frac{1}{2}}} \right)) \right)$
 - A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = +3dBFS$
 - Note that the Peak power of a CW has positive dBFS value (+3dBFS) due to this convention
- Digital blocks with complex output (i.e., Mixer, DDC, etc.), the calculation for power in dBFS is the same as that for the DAC.
 - A complex CW $X_{out}(N) = 2^{15} * e^{2 * \pi * i * \frac{f_c}{f_s} * N}$ has $Power_{rms} = 0dBFS$ and $Power_{peak} = 0dBFS$
 - A real CW $X_{out}(N) = 2^{15} * \cosine \left(2 * \pi * \frac{f_c}{f_s} * N \right)$ has $Power_{rms} = -3dBFS$ and $Power_{peak} = 0dBFS$

Quick Start for each panel

GUI Overview

The screenshot shows the AMD Xilinx RFSoc Frequency Planner GUI. The interface is divided into several sections:

- Left Panel:** Contains 'RFSoc Family' (set to RFSoc DFE) and 'Device PN' (ZU67DR). Below this is 'Device Info' with read-only fields for DACs, ADCs, and impairments. At the bottom is a 'Time Plot' showing a CCDF distribution plot of PAR (dB) vs. Probability (%).
- Top Panel:** Features 'Tab selection for converter type or PLL' (DAC, ADC, PLL) and 'Blocks available in RFSoc DFE' (DPD, P/Q Resampler, CFR, NCO, Mixer, QMC, IMR Mode, Inverse Sinc, DAC Core).
- Center Panel:** Displays 'Input signal source, up to 4 component carriers, not part of the hard IP'. It includes a table for carrier parameters (FREQ(M), BW(M), Pwr(dB), Enable) and a table for channel power measurements (Fc, BW, Pwr (dBm)).
- Right Panel:** Shows 'Status and error message' (Updating DAC Complete) and 'Channel power measurement' table.
- Bottom Panel:** Displays a 'Frequency domain plot of stage/block output' (DAC Output Spectrum) showing Amplitude (dBm) vs. Frequency (MHz). It includes a legend for HD2, HD3, PLL, 2Fs, Stat, and Filter.

Annotations with arrows point to specific features:

- Tab selection for converter type or PLL
- Blocks available in RFSoc DFE
- Input signal source, up to 4 component carriers, not part of the hard IP
- Click to Start or Update Simulation
- Status and error message
- Channel power measurement
- RMS and Peak power stats for each block output
- Block for each stage of the hardened data converter tile
- Plot trace on/off viewing option
- Frequency domain plot of stage/block output, click on stage to select its output to be displayed
- RFSoc family and device selection
- Device info, read only
- Device impairments, default values for reference only, user should change the values to better reflect what's being used.
- Time domain plot or Peak to Average (PAR) distribution plot

DAC Simulation Quick Start

1. Select RFSoc Device of choice:

RFSoc Family: RFSoc DFE
Device PN: ZU67DR

2. Edit or confirm existing impairment values for the DAC column.

Spec	DAC	ADC	Enable
NSD[dBm/Hz]	-165	-152	<input checked="" type="checkbox"/>
HD2[dBc]	-65	-65	<input checked="" type="checkbox"/>
HD3[dBc]	-70	-70	<input checked="" type="checkbox"/>
TIS[dBc]	NaN	-85	<input checked="" type="checkbox"/>
OIS[dBFS]	NaN	-85	<input checked="" type="checkbox"/>

3. Enter Input data sampling rate and desired RMS power level.

- Select DUC enable/disable option; input Sampling rate is the same as DAC sampling rate for DUC bypassed
- Modulated signal typically has 10 to 12dB PAR (peak to average ratio); single CW tone has 0dB PAR.

Input Fs Msp: 491.62
Rms Pwr dBFS: -15
DUC Enable:

4. Configure the baseband input signal in the signal composition table

- Supports up to 4 component carriers (CC); at least one CC must be enabled.
- Enter carrier frequency Fc in MHz, signal bandwidth in MHz (0 for CW), and relative power in dB for each CC.
- Baseband composite signal total instantaneous bandwidth should be < Nyquist BW (Fs for cplx, Fs/2 for real).

	FREQ(M)	BW(M)	Pwr(dB)	Enable
CC0	0	100	0	<input checked="" type="checkbox"/>
CC1	75	50	-3	<input type="checkbox"/>
CC2	-75	50	-3	<input type="checkbox"/>
CC3	150	100	0	<input type="checkbox"/>

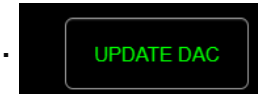
5. Configure each of the DAC stages with the desired setting (see PG269 for details of each stage)

- If RFSoc DFE device is selected, CFR, P/Q, and DPD blocks are enabled for use
 - The CFR block and DPD block used here are not the same as the AMD Xilinx IP. They are very simple models provided to enable signal power level and frequency spectrum planning only. See tooltips for more info.
 - The CFR block allows the user to reduce the PAR of the signal by specifying a target PAR value. Not all target values are achievable due to the simplicity of the model. Best effort is used.
 - The DPD block simulates signal expansion in the time and frequency domain of a typical DPD function. It simply adds IMD3 and IMD5 to the signal; level of the IMD's in dBc can be adjusted by the user to fine tune the amount of spectrum expansion from the DPD. Note that the PAR of the output signal will generally increase to resemble that of a Gaussian bandlimited signal; user cannot predefine the exact output PAR value.
 - Both blocks have adjustable output gain for further fine tuning the signal level at each of the stages.

DAC Simulation Quick Start

6. Ensure that all stages have valid sampling rate for the chosen device after configuration change. Invalid sampling rates will be shown in red. It is possible to run the simulation with invalid sampling rates, but not recommended.

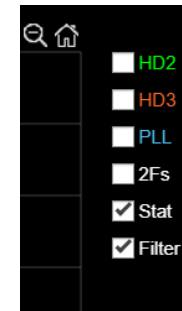
7. Press 'UPDATE DAC' to start/update simulation with the selected configuration.



8. Check 'Status' bar for any error or warning messages.

9. Simulation output is now updated on the 2 plots; below are some options after the update is done.

- Select or deselect each of the trace options next to the Output Spectrum plot to view location and signal level of each of the impairments.
- Click on any of the stages to view the output of the stage
- Check 'Stat' to view RMS and Peak power at the output of each stage (see snippet on right)
- Check 'Filter' to view the filtering response of an applicable filter stage (see snippet on right)
- Configure the Power Measurement and Click on the box to measure channel power for the DAC output
- Go to File → Save Configuration to save a copy of the current configuration. The DAC, ADC, and PLL will all be saved.



ADC Simulation Quick Start

1. Select RFSoc Device of choice:

RFSoc Family	RFSoc DFE
Device PN	ZU67DR

2. Edit or confirm existing impairment values for the ADC column.

Spec	DAC	ADC	Enable
NSD[dBm/Hz]	-165	-152	<input checked="" type="checkbox"/>
HD2[dBc]	-65	-65	<input checked="" type="checkbox"/>
HD3[dBc]	-70	-70	<input checked="" type="checkbox"/>
TIS[dBc]	NaN	-85	<input checked="" type="checkbox"/>
OIS[dBFS]	NaN	-85	<input checked="" type="checkbox"/>

3. Enter Input Sampling rate of the ADC and desired RMS power level at ADC Core output.

- Select fast (Dual) or slow (Quad) ADC if device has both types; select DDC enable/disable option.

ADC Fsamp Msp	2949.12	DDC Enable
Rms Pwr dBFS	-12	Quad ADC

4. Configure the RF input signal in the signal configurator table

- Supports up to 4 component carriers (CC); at least one CC must be enabled
- For valid ADC support use case, only carriers in the same Nyquist zone should be enabled.
- Enter RF carrier frequency F_c in MHz, signal bandwidth in MHz (0 for CW), and relative power in dB for each CC.
- Composite signal total instantaneous bandwidth should be $<$ Nyquist BW (F_s for cplx, $F_s/2$ for real).

	FREQ(M)	BW(M)	Pwr(dB)	Enable
CC0	3800	100	0	<input checked="" type="checkbox"/>
CC1	3500	100	0	<input type="checkbox"/>
CC2	1900	20	0	<input type="checkbox"/>
CC3	4900	50	0	<input type="checkbox"/>

5. Configure each of the ADC stages with the desired setting (see PG269 for details of each stage)

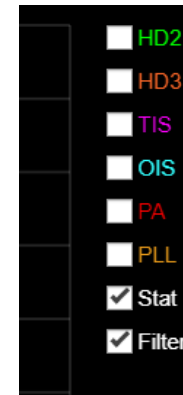
6. Ensure that all stages have valid sampling rate for the chosen device after configuration change. Invalid sampling rates will be shown in red. It is possible to run the simulation with invalid sampling rates, but not recommended.

7. Press 'UPDATE ADC' to start/update simulation with the selected configuration.



ADC Simulation Quick Start

8. Check 'Status' bar for any error or warning messages
9. Simulation output is now updated on the 2 plots; below are some options after the update is done.
 - Select or deselect each of the trace options next to the Output Spectrum plot to view location and signal level of each of the impairments.
 - Click on any of the stages to view the output of the stage
 - Check 'Stat' to view RMS and Peak power at the output of each stage (see snippet on right)
 - Check 'Filter' to view the filtering response of an applicable filter stage (see snippet on right)
 - Configure the Power Measurement and Click on the box to measure channel power for any of current active ADC stage
 - Go to File → Save Configuration to save a copy of the current configuration. The DAC, ADC, and PLL will all be saved.



PLL Simulation Quick Start

1. Select RFSoc Device of choice:

RFSoc Family	RFSoc DFE
Device PN	ZU67DR

2. Click on PLL Panel then select Converter Type (ADC and DAC PLL settings are slightly different).

Converter Type
<input type="radio"/> DAC
<input type="radio"/> ADC

3. Enter desired converter sampling rate and RF frequency at which the phase noise is evaluated.

Sampling Rate	9830.4
RF Carrier Freq	1000

1. Note that AMD Xilinx datasheet and characterization report of internal PLL defaults RF Carrier Frequency to 1000MHz, unless otherwise noted.

4. Enter input reference oscillator frequency, and its phase noise at the different offsets.

5. Enter R divider value, incorrect entry will be auto changed to a valid one. Typically, value of 1 is used. See datasheet DS926 for valid range.

6. Press 'UPDATE PLL' to start/update simulation with the selected configuration.



7. Check for 'Status' bar for any error or warning messages.

8. Simulation output is now updated on the main plot. 4 traces are plotted to show the various noise contributions.

- PLL PN – this is the noise from the phase locked loop (including PFD, charge pump, dividers, 1/f flicker, loop filter).
- Ref Osc PN - this is the noise contributed from the input reference oscillator
- VCO PN – this is the noise contributed from the VCO
- Total PN – this is the final output phase noise of the PLL output, scaled to the desired RF frequency (default is 1GHz)
- The total PN result is also tabulated at various common offsets in the table on the right.
- The results in the table can also be copied to the PLL impairment table for ADC and DAC simulation use.

RF Out Phase Noise	
100Hz	-103.66
1kHz	-112.86
10kHz	-120.22
100kHz	-126.94
1MHz	-132.16
10MHz	-149.69
100MHz	-161.75

Copy to Impairment Table

Export Time Domain Samples

- ▶ The time domain samples for each of the sub blocks can be exported
 - Supported file formats include matlab (.mat), text (.txt), and tdms (.tdms)
 - .mat file will include 2 variables data_real and data_imag
 - .txt file will include 2 columns separated by comma, first column is the real part of the signal, second column is the imaginary part. If the signal is real, then the imaginary data will be all zeros.
 - .tdms file will include 2 groups, first group contains the sampling rate in MHz; 2nd group contains in the I/Q data. The format is compatible with the tdms format used in AMD's RFDC Evaluation User Interface software.
 - Exported data can be are always in 16bit signed format. All samples will be exported.
 - To export time domain samples
 - Select "Time Plot" option on the left panel plot
 - Update either the DAC or ADC to generate data for each of its sub-blocks
 - Click on a sub-block of interest
 - Select File → Export Time Domain Samples from the Menu
 - Select File Type and type and enter output file name

Advanced Menu Options

▶ Add CC to DAC

- Increment the number of component carriers by 1 to the DAC signal table, up to a maximum of 16 total. Restore default button will reset the table to 4 CCs.

▶ ADD CC to ADC

- Increment the number of component carriers by 1 to the ADC signal table, up to a maximum of 16 total. Restore default button will reset the table to 4 CCs.

▶ Custom DAC Signal

- User provided input signal to the DAC. CFR and DPD blocks will be disabled for this mode. Both .mat and .txt files are supported. The file format is the same as that exported by the tool. See tooltips for additional information on the data format and length requirements.

▶ Custom ADC Signal

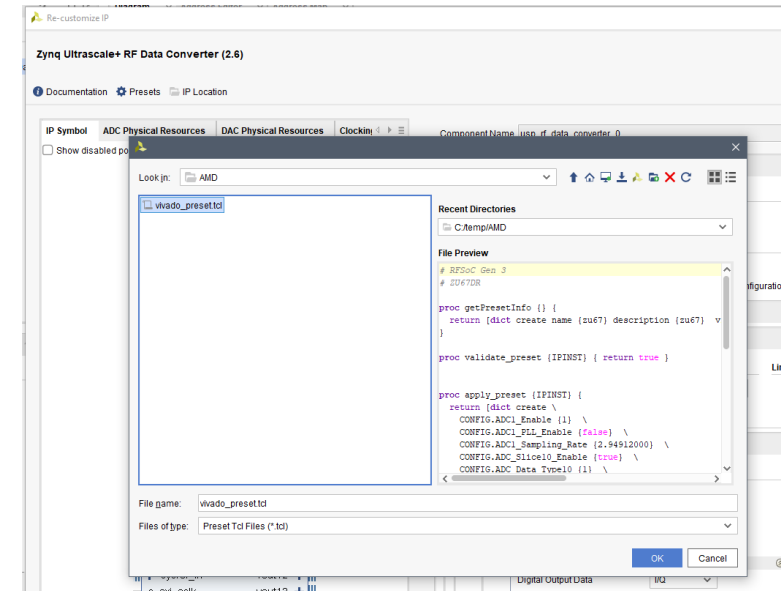
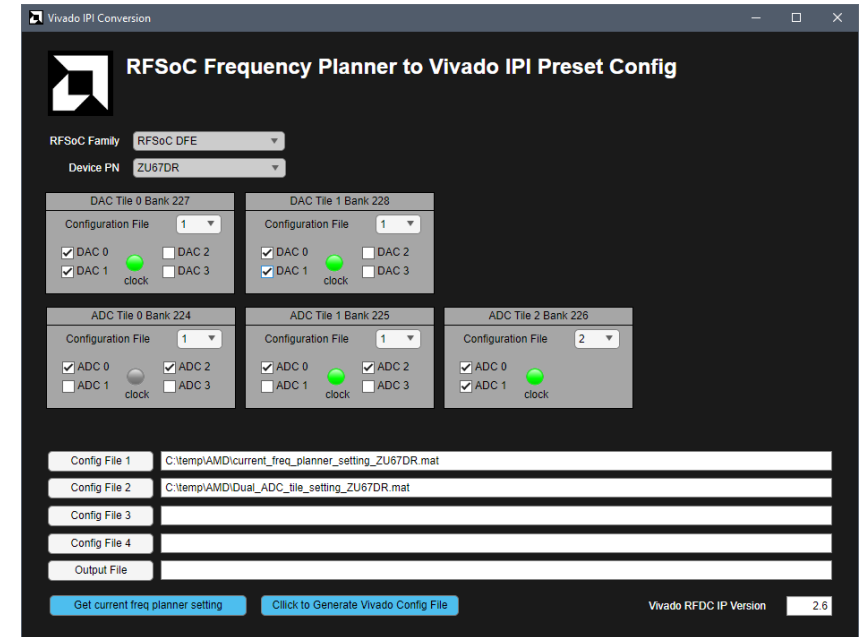
- User provided input signal to the ADC digital processing blocks. Since the input to the ADC is analog RF signal it is not possible to capture that in a digital file. Instead, the user signal should represent data at the output of the ADC core. Impairments are then added to the input signal and processed through the DDC/Mixer data-path. Both .mat and .txt files are supported. The file format is the same as that exported by the tool. See tooltips for additional information on the data format and length requirements. TIS spurs option is not available for custom ADC signals.

Export Config to Vivado Preset

- ▶ Settings for the DAC and ADC can be saved under File → Save Configuration. A saved configuration in turn can be used to generate Vivado IP Preset file to auto configure the RFSoc IP in Vivado IP wizard.
 - A Preset file for Vivado IP is a tcl script that auto configures a particular IP to a predefined setting. The IP in this case is the RF Data Converter.
- ▶ The preset export tool in the frequency planner generates a tcl script based on saved configuration file assigned to each of the DAC or ADC tiles.
 - Each DAC or ADC tile can choose from 1 of 4 possible configuration files
 - The current frequency planner setting can be used as one of the configuration files. Upon clicking on 'Get current freq planner setting' button the tool will generate a configuration file and save it to C:\temp\AMD\current_freq_planner_setting_ZUxxDR.mat. This file is then used as Config File 1.
 - Each frequency planner configuration file contains a specific setting for the DAC and for the ADC
 - The PLL setting in the configuration file does not get used. The Vivado Preset generated will always set the PLL to be disabled. User must fine tune the final PLL/clocking distribution in Vivado after the preset is applied.
 - All channels within a tile will get the same setting. Unchecked channels in each tile will be disabled.
- ▶ A green clock lamp in the tile indicates the tile has an input clocking port where a reference clock or a RF sampling clock can be provided externally. An 'off' clock lamp means the tile requires a clock to be distributed from another tile.
- ▶ The preset tcl file will be written to the "Output File" target. If no output file target is provided the tool will generate the output file to C:\temp\AMD\vivado_preset_ZUxxDR.tcl

Export Config to Vivado Preset Usage

- ▶ File → Export Config to Vivado Preset to open the export tool, as shown in figure on the right.
- ▶ Select RFSoc Family and Device Part Number
 - Corresponding types of DAC and ADC tiles corresponding to the part number will be populated
- ▶ Select 1 of 4 Configuration Files for each tile
- ▶ Select each of the channels within the tile to be enabled
- ▶ Select the configuration file name and path for each of the 4 Config Files. Config files not used can be left empty.
- ▶ Select the Output file target. A default is used if not selected.
- ▶ Ensure the Vivado RFDC IP Version is correct. It should be 2.6 as of the date of this current tool release. The version # can be found in Vivado RF Data Converter IP.
- ▶ Press “Click to Generate Vivado Config File’ to complete the process.
- ▶ The output file is now ready to be used in Vivado, see snippet on the right.



Other Usage Notes and Tips

- Configurations can be saved, loaded, and shared.
- Configuration files are only backward compatible for minor revisions of the tool, for instance
 - Version 2.0 and 2.x configuration files are compatible with each other.
 - Version 1.0 and 2.0 configuration files are not compatible with each other.
- Software versions are installed in difference folders, thus older version will not be overwritten.
 - More than 1 instance of the software can be running concurrently, for same version or difference versions.
- Software Help is generally done with tooltips; hover mouse over block to view
- Any changes to the ADC/DAC configuration and RBW (resolution bandwidth of power spectrum plot) requires an 'Update' to get new results.
 - Changes to other plot options do not need a new 'Update', simply click on the stage of interest to view the changes in plot option selection.
- Trace of the various digital filters are scaled to the signal level for ease of viewing, it does not represent the actual gain of the filter.
- The NCO Frequency value for the Mixers (ADC and DAC) does not use the same convention as that in the RFSoc API, this is done for ease of use. Below is the equation used for the mixer. See tooltip for more detail.
 - $$X_{out}(N) = X_{in}(N) * \exp(2 * \pi i * i * \frac{F_{NCO}}{F_{samp}} * N)$$
- Some values outside the specification of the selected device may be allowed for simulation to run for the purpose of hypotheticals. Invalid values will still be flagged. User should be cautious on what's realizable with the device.

Other Usage Notes and Tips

- Both DAC and ADC simulation supports up to 16 CC's (component carriers), some use cases include
 - Two CW tones, one at each edge of the desired band. This can be used to check some of the filtering artifacts and alias.
 - One wanted modulated signal and one high level CW. This can be used to examine the receiver blocker situation.
 - 2 different signal on either side of DC. This can be used to visualize spectral inversion at different stages of the signal chain.
 - Signals from different RF bands into the ADC to see how the alias of one band affects another; useful for co-location deployments.
- On the DAC panel, CFR, P/Q, and DPD blocks are always bypassed if 'DUC Bypass' Datapath is selected. This is only applicable to RFSoc DFE device. Other devices do not have these blocks.
- Click 'Restore default' for any of the panels in case the tool is stuck in some unknown / invalid configuration; then begin changing the configuration to the one desired.
- NSD, HD2, HD3, TIS, and OIS levels can be changed to make the plots and traces visually stand out for ease of identification, and experiment with hypotheticals.
 - Example, setting the ADC NSD to -174 will prevent the noise floor from masking the location of the HD2 and HD3 components of the ADC. This is especially usefully for bandlimited signals.
- IMD3 is not modelled in the tool as the location of the IMD3 products are evident, mostly inside the wanted band, and not really an exercise for frequency planning.

Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of AMD Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, AMD Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) AMD Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of AMD Xilinx products in such critical applications, please refer to AMD Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm>

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.



Thank You

Disclaimer and Attribution

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale. GD-18

© Copyright 2021 Advanced Micro Devices, Inc. All rights reserved. Xilinx, the Xilinx logo, AMD, the AMD Arrow logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

