Example Zynq-7000 DDRC Address Map

Table 1 and Table 2 show the valid mapping settings from the physical, AXI address, to the bank (ba), row (r), and column (c) DDR addresses. The least significant bits of AXI address are consumed as the DQ width of the DDR interface. Each numbered cell (such as ba2), show the relevant DDR address bit that the register field on the left corresponds to, and the Internal Base for that field. Non-shaded cells represent valid address mappings. The prefix 'reg_ddrc_addrmap_' should be added for the full register field names.

Using an example system with details shown in Table 1, Table 2 shows an example address mapping from AXI address to the DDR addresses. This configuration orders the contiguous bits in a Row-Bank-Column configuration, with the most significant row as the most significant AXI address bit used by the DDR controller. Since the total DDR memory size is 1GB, note that there are no unused AXI address bits in this map, besides the upper 2 AXI bits used for other peripherals in the system.

Table 1: Example Address Map System Conditions

Example Condition	**Example Value**
Memory Type	DDR3
Memory Width Address Bits	2 (32-bit DQ)
Bank Address Bits	3
Row Address Bits	15
Column Address Bits	10
Register DRAM_addr_map_bank	0x00000777
Register DRAM_addr_map_col	0xfff00000
Register DRAM_addr_map_row	0xf666666

Table 2: AXI to DDR Address Bit Mapping

AXI Addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
row_b15 (1)								N/A																								
row_b14 (1)			r14																													
row_b13 (1)				r13																												
row_b12 (1)					r12																											
row_b2_11						r11	r10	r9	r8	r7	r6	r5	r4	r3	r2																	
row_b1																r1																
row_b0																	r0															
bank_b2 (1)																		ba2														
bank_b1																			ba1													
bank_b0																				ba0												
col_b11 (1)(2)																		N/A														
col_b10 (1)(2)																			N/A													
col_b9 (1)(2)																				N/A												
col_b8 (1)																					c9											
col_b7 (1)																						c8										
col_b6																							c7									
col_b5																								c6								
col_b4																									c5							
col_b3																										c4						
col_b2																											c3					
N/A (fixed)																												c2	c1	c0	w1	w0