Figure 1 Clocking mechanism for the OOB detect circuit:

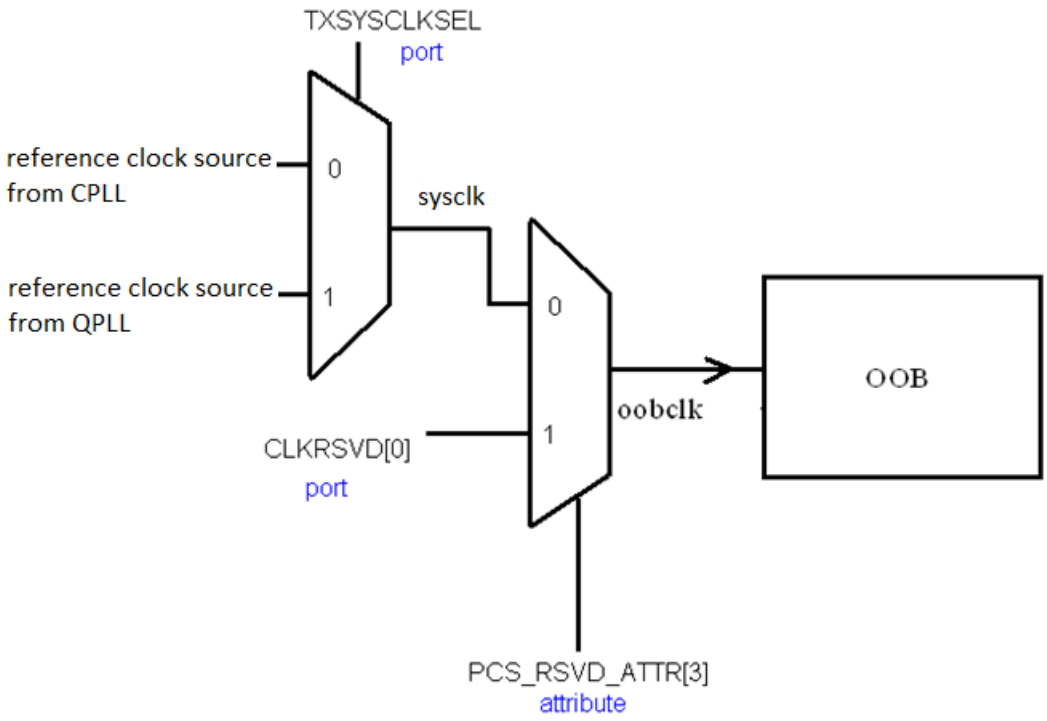

Figure 2 showing a simple toggle flip flop (shown below) may be used to divide the refclk. .

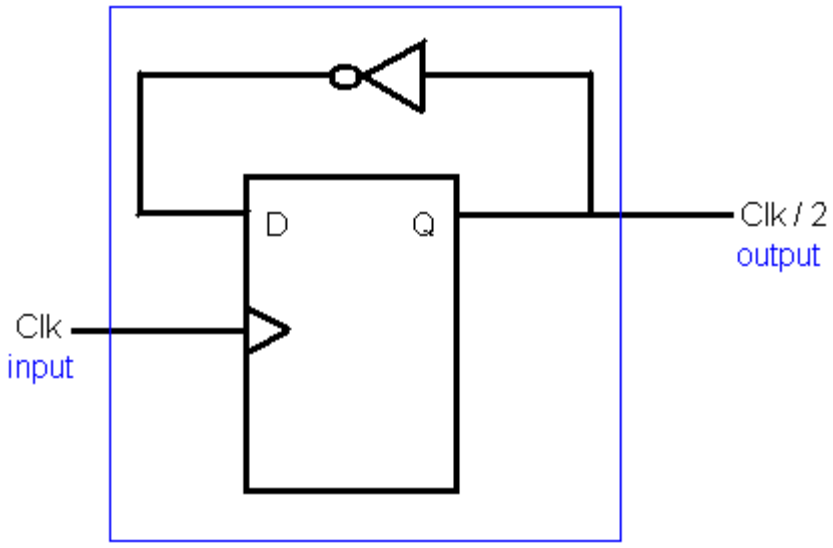

Figure3 showing how Cascading several divide by two circuits (as shown below) produces higher order clock dividers such as divide by 4 and divide by 8.

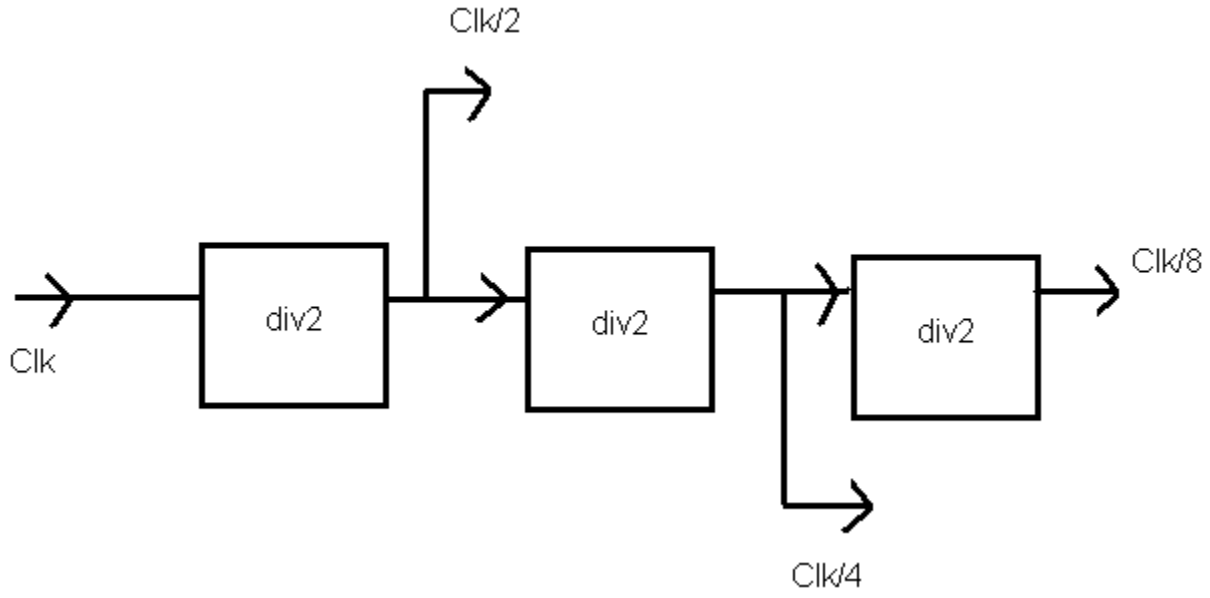

Figure 4 Flowchart to determine whether the RX is in Electrical Idle for the Protocols with linerates lessthan or equal to 1.5G

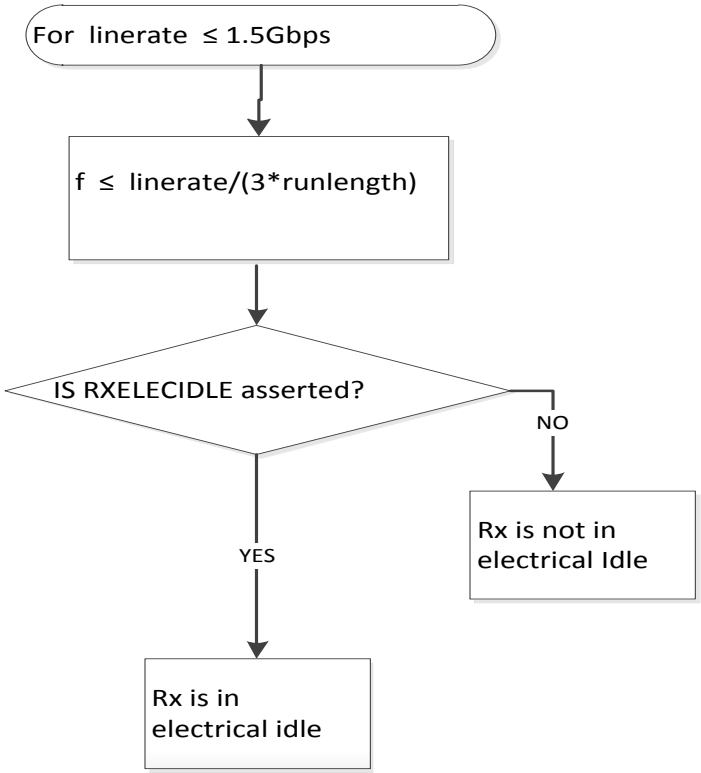

Figure 5 Flowchart to determine whether the RX is in Electrical Idle for SATA 3G or SATA 6G

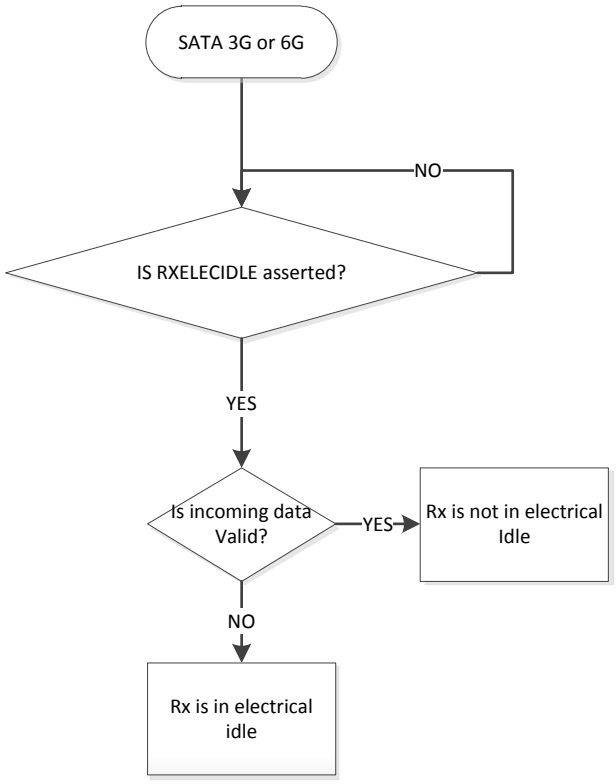

Figure 6 Flowchart to determine whether the RX is in Electrical Idle for the PCIE gen1

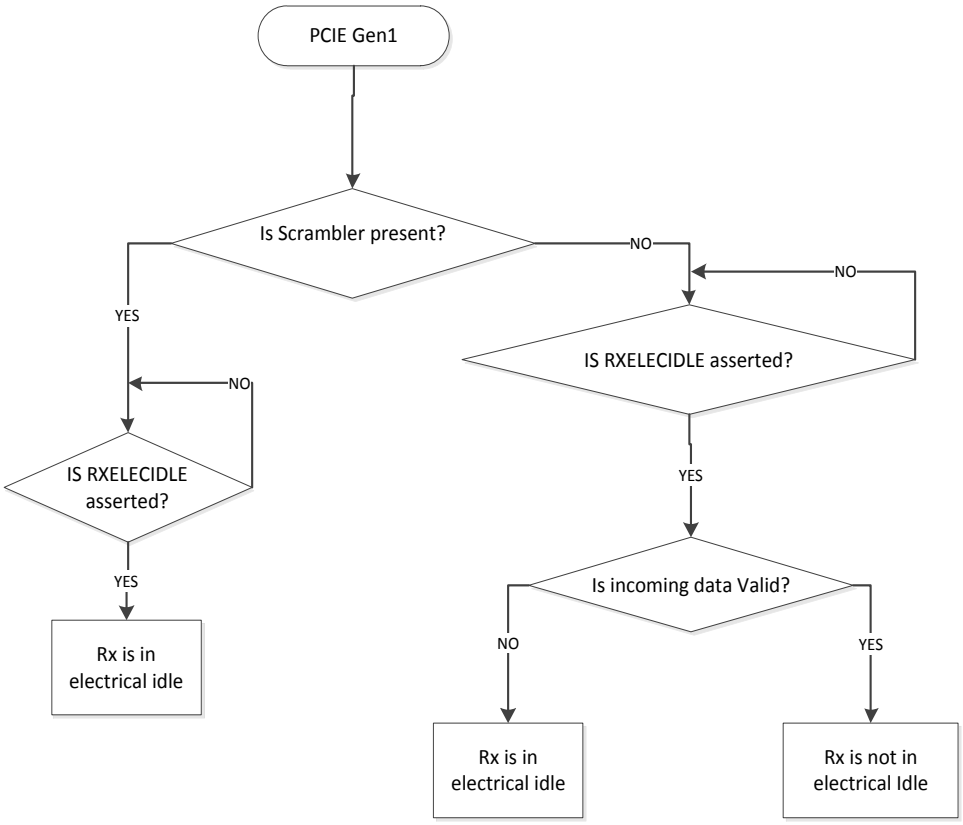

Figure 7 Flowchart to determine whether the RX is in Electrical Idle for the PCIE gen2

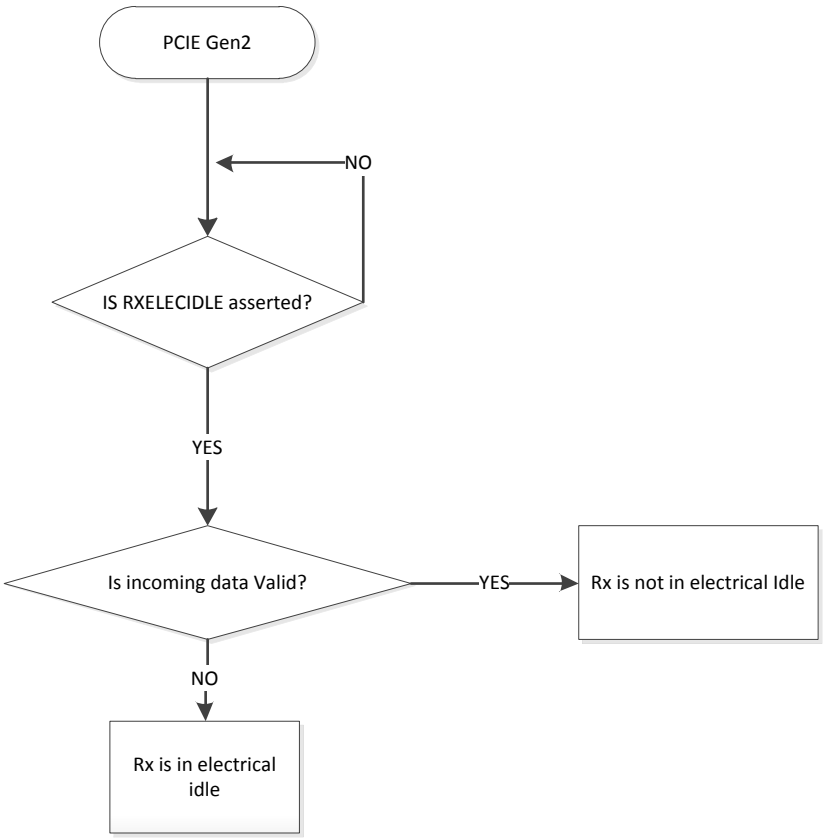

Figure 8 Flowchart for the entry electrical idle for RX for PCIE gen2 or Gen3

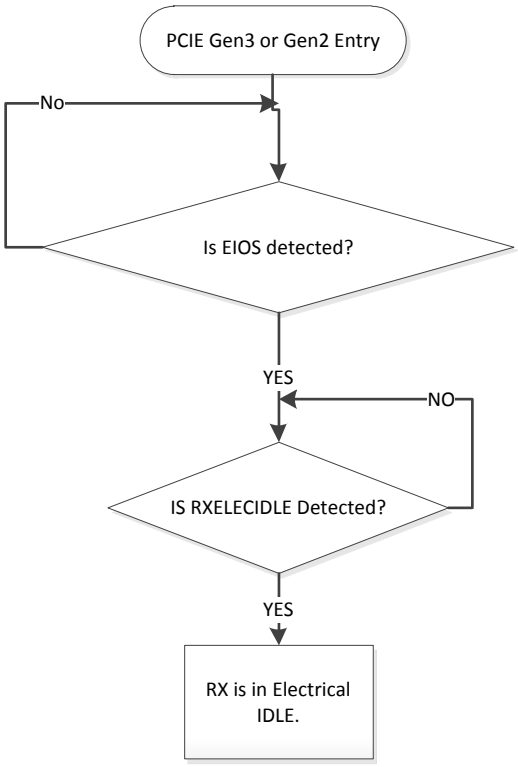

Figure 9 Flowchart for the exit from electrical idle for RX for PCIE gen2 or Gen3