Change log for MicroBlaze

Changes in v8.40.b, introduced in 14.4

14.4 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Removed support for qvirtex7l and virtex7l

Resolved issues:

- None

Known Issues / Limitations:

- None

14.4 - Changes in tool interface files (.mpd)

- None

14.4 - Changes in Tcl script files associated with core (.tcl)

- None

14.4 - Changes in documentation associated with core

- Chapter 3 - MicroBlaze Core Configurability:
  - Updated Table 3-18 to remove qvirtex7l and virtex7l.
- Chapter 5 - Instructions:
  - Updated LWX and SWX to document restrictions for subsequent instruction.

Changes in v8.40.b, introduced in 14.3

14.3 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Relocatable base vectors

Resolved issues:

- Avoid timing issues due to unused flip-flops connecting clock to data [CR<663376>]
  - Version that have this issue: v8.40.a
- Ensure that memory barrier waits for adjacent data cache access in all cases [CR<675207>]
  - Version that have this issue: v8.40.a

Known Issues / Limitations:

- None

14.3 - Changes in tool interface files (.mpd)

- Added C_BASE_VECTORS parameter

14.3 - Changes in Tcl script files associated with core (.tcl)

- None

14.3 - Changes in documentation associated with core

- Chapter 2 - Overview:
  - Updated v8.40 features in Table 1-1 Configurable Feature Overview.
- Chapter 2 - Registers:
  - Added v8.40.b to MicroBlaze release version code in PVR.
- Chapter 2 - Privileged Instructions:
  - Added effect of C_BASE_VECTORS to description.
- Chapter 2 - Reset, Interrupts, Exceptions, and Break
  - Added effect of C_BASE_VECTORS to description.
- Chapter 3 - MicroBlaze Core Configurability:
  - Added C_BASE_VECTORS parameter description to Table 3-17.

- Chapter 4 - Interrupt and Exception Handling
  - Added effect of C_BASE_VECTORS to description.
- Chapter 5 - Instructions:
  - Corrected MBAR pseudo-code.
  - Updated BRKI and BRALID descriptions with effect of C_BASE_VECTORS.
  - Corrected WIC notes.

Changes in v8.40.a, introduced in 14.2

14.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Sleep mode for power reduction

Resolved issues:

- Remove inadvertent dependence on C_USE_PCMP_INSTR for byte and halfword swap instructions [CR<662339>]
    - Versions that have this issue: v8.30.a
    - Can only occur when area optimization is not enabled

Known Issues / Limitations:

- None

14.2 - Changes in tool interface files (.mpd)

- Added ports Sleep, Wakeup, and Dbg_Wakeup

14.2 - Changes in Tcl script files associated with core (.tcl)

- None

14.2 - Changes in documentation associated with core

- Chapter 2 - Overview:
    - Added v8.40 features in Table 1-1 Configurable Feature Overview.
- Chapter 2 - Registers:
    - Added v8.40.a to MicroBlaze release version code in PVR.
- Chapter 2 - Debug and Trace
    - Added description of debug signals [CR<656143>]
- Chapter 3 - MicroBlaze Core Configurability:
    - Added ports Sleep, Wakeup and Dbg_Wakeup to Table 3-1.
- Chapter 5 - Instructions:
    - Updated MBAR description, including SLEEP instruction description and delay slot restriction

Changes in v8.30.a, introduced in 14.1

14.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Low-latency Interrupt Mode
- Support for qartix7, qartix7l, qkintex7, qkintex7l, qvirtex7, qvirtex7l, qzynq, and azynq families
- Byte and halfword swap instructions

Resolved issues:

- Ensure that MBAR is treated as a NOP when the data cache is not implemented (C_USE_DCACHE = 0).
    - Versions that have this issue: v8.20.b, v8.20.a, v8.10.a.
- Generate Instruction Bus Error exception correctly when an instruction read error occurs on M_AXI_IC.
    - Only occurs when C_INTERCONNECT is set to 2 and C_ICACHE_ALWAYS_USED is set to 1 with the cache turned off.
    - Versions that have this issue: v8.20.b, v8.20.a, v8.10.a, v8.00.b, v8.00.a.
- Directly use DSP48E1 for architectures that support it to avoid synthesis warning messages [CR<637301>].
    - Only applies when C_USE_HW_MUL is greater than 0 or C_USE_FPU is greater than 0.
    - Versions that have this issue: v8.20.b, v8.20.a, v8.10.a, v8.00.b, v8.00.a, v7.30.b, v7.30.a, v7.20.d, v7.20.c, v7.20.b.
- Fixed issue with interrupts taken twice for interrupted blocking GET, PUT, GETD, PUTD instructions.
    - Only occurs when area optimization is enabled, when C_INTERRUPT_IS_EDGE is set and when C_USE_EXTENDED_FSL_INSTR is enabled.
    - Versions that have this issue: v8.20.b, v8.20.a, v8.10.a, v8.00.b, v8.00.a, v7.30.b, v7.30.a, v7.20.d, v7.20.c, v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a.

Known Issues / Limitations:

- None

14.1 - Changes in tool interface files (.mpd)

- Added INTERRUPT bus with new ports Interrupt_Address and Interrupt_Ack to support low-latency interrupt mode.
- Changed parameter C_USE_INTERRUPT to add low-latency interrupt mode.

- Added AXI Stream interfaces to clock input [CR<640767>].
- Added parameter C_USE_REORDER_INSTR to allow disabling of reversed load, reversed store, and swap instructions.

14.1 - Changes in Tcl script files associated with core (.tcl)

- Set C_USE_INTERRUPT to support low-latency interrupt mode.

14.1 - Changes in documentation associated with core

- Chapter 2 - Overview:
  - Added v8.30 features in Table 1-1 Configurable Feature Overview.
- Chapter 2 - Registers:
  - Added v8.30.a to MicroBlaze release version code in PVR.
  - Added C_USE_REORDER_INSTR parameter in PVR 0.
  - Added new families in PVR.
- Chapter 2 - Virtual Memory Management:
  - Added information about behavior of unimplemented zones.
- Chapter 2 - Reset, Interrupts, Exception and Break:
  - Updated interrupt description with low-latency interrupt mode.
- Chapter 3 - MicroBlaze Core Configurability:
  - Added new ports Interrupt_Address and Interrupt_ack to Table 3-1.
  - Updated description of parameter C_USE_INTERRUPT in Table 3-15.
  - Added description of parameter C_USE_REORDER_INSTR in Table 3-15.
  - Added Table 3-16 to list supported families.
- Chapter 4 - Interrupt and Exception Handling
  - Updated interrupt description with low-latency interrupt mode.
- Chapter 5 - Instructions:
  - Added low-latency interrupt description to MSRSET, MTS and RTID.
  - Corrected description of PUT extended instructions to also include test.
  - Updated description of reversed load and reversed store instructions with effect of C_USE_REORDER_INSTR parameter.
  - Added description of SWAPB and SWAPH instructions

Changes in v8.20.b, introduced in 13.4

13.4 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Support for aartix7 and artix7l families

Resolved issues:

- Corrected recognition of virtex7l family [CR<639120>].

Known Issues / Limitations:

- None

13.4 - Changes in tool interface files (.mpd)

- None

13.4 - Changes in Tcl script files associated with core (.tcl)

- None

13.4 - Changes in documentation associated with core

- Chapter 2 - Registers:
  - Added v8.20.b to MicroBlaze release version code in PVR.
  - Added new families in PVR.
  - Clarified description of parameters C_ICACHE_ALWAYS_USED and C_DCACHE_ALWAYS_USED.
  - Document that C_ENDIANNESS can be overridden.
- Chapter 3 - MicroBlaze Core Configurability:
  - Added description of parameters C_ICACHE_ALWAYS_USED and C_DCACHE_ALWAYS_USED for AXI [CR<632879>].
  - Added new families in Table 3-15.
  - Clarified description of parameters C_ICACHE_ALWAYS_USED and C_DCACHE_ALWAYS_USED in Table 3-15.
- Chapter 5 - Instructions:

- Clarified GET, GETD, PUT, and PUTD behavior.

Changes in v8.20.a, introduced in 13.4

13.4 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- None

Known Issues / Limitations:

- None

13.4 - Changes in tool interface files (.mpd)

- Changed parameter C_ENDIANNESS to allow user override [CR<624380>]

13.4 - Changes in Tcl script files associated with core (.tcl)

- Added DRC to ensure that clocks connected to MicroBlaze and LMB cores are identical [CR<623467>]

13.4 - Changes in documentation associated with core

- None

Changes in v8.20.a, introduced in 13.3

13.3 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- None

Known Issues / Limitations:

- None

13.3 - Changes in tool interface files (.mpd)

- None

13.3 - Changes in Tcl script files associated with core (.tcl)

- Changed cache connection DRC to take lockstep slave into account
- Improved DRC message when cacheable segment size is less than cache size [CR<615417>]

13.3 - Changes in documentation associated with core

- Chapter 2 - Self-modifying Code
  - New chapter.
- Chapter 2 - Special Purpose Registers
  - Added mnemonics for parameters C_ENDIANNESS, C_PVR, C_USE_FPU, C_USE_HW_MUL, and C_USE_MMU [CR<615165>].
- Chapter 2 - Debug and Trace
  - Corrected debug feature description.
- Chapter 3 - CacheLink Signal Interface
  - Clarified when entire cache lines become valid with write-back cache.
- Chapter 3 - MicroBlaze Core Configurability:
  - Added mnemonics for C_USE_FPU [CR<615165>].
- Chapter 5 - Instructions:

- Improved MBAR description.

Changes in v8.20.a, introduced in 13.2

13.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Lockstep support for high integrity applications
- Support for qvirtex5, artix7 and zynq families
- Configurable use of FPGA primitives
- Data width 512 bits for AXI cache interconnects

Resolved issues:

- Corrected XCL read access protocol to avoid an incorrect repeated access in some cases [CR<591285>].
  - Can only occur when C_DCACHE_USE_WRITEBACK is set and C_INTERCONNECT is set to 1
  - Only affects systems using the XPS_MCH_EMC memory controller
  - Versions that have this issue: v8.00.b, v8.00.a
- Ensure that the LMB address strobe is always correctly asserted [CR<606664>]
  - Can only occur when area optimization is not enabled, when C_FAULT_TOLERANT is set, and C_DCACHE_USE_WRITEBACK is not set
  - Only occurs when a WDC instruction is immediately followed by an LMB memory load/store instruction
  - Versions that have this issue: v8.10.a
- Avoid stall when executing memory barrier instruction [CR<608836>]
  - Can only occur when area optimization is not enabled, PLBv46 interconnect is used, and C_DCACHE_USE_WRITEBACK is not set
  - Versions that have this issue: v8.10.a
- Corrected synthesis error when Branch Target Cache is set and MMU Protection is enabled [CR<612255>]
  - Versions that have this issue: v7.30.a, v7.30.b, v8.00.a, v8.00.b, v8.10.a

Known Issues / Limitations:

- None

13.2 - Changes in tool interface files (.mpd)

- Added parameter C_LOCKSTEP_SLAVE and lockstep ports
- Added parameter C_AVOID_PRIMITIVES for configurable use of FPGA primitives

13.2 - Changes in Tcl script files associated with core (.tcl)

- Set interconnects based on existing MicroBlaze instances, if any, when adding a new instance [CR<588251>]
- Added DRC to disallow use of PLBv46 with 7-Series or later families
- Added DRC to check lockstep slave parameters

13.2 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Added v8.20 features in Table 1-1 Configurable Feature Overview.
- Chapter 1 - Special Purpose Registers
  - Clarified description of Machine Status Register FSL bit [CR<608401>].
- Chapter 1 - Privileged Instructions
  - Added description of C_MMU_PRIVILEGED_INSTR usage.
- Chapter 1 - Instruction Cache:
  - Updated cache data width description to add 512 bits.
- Chapter 1 - Data Cache:
  - Updated cache data width description to add 512 bits.
- Chapter 1 - Fault Tolerance:
  - New chapter.
- Chapter 1 - Lockstep
  - New chapter.
- Chapter 2 - MicroBlaze I/O Overview:
  - Added ports for lockstep signals.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description
  - Clarified behavior of FSL_IN_Read signals with XCL2 protocol after starting burst read [CR<595953>].
- Chapter 2 - AXI4 Interface Description
  - Updated AXI data width description to add 512 bits.
  - Clarified parameters affecting read/write issuing [CR<608881>].
- Chapter 2 - Trace Interface Description
  - Added missing trace signals.
- Chapter 2 - Lockstep Interface Description:
  - New chapter.
- Chapter 2 - MicroBlaze Core Configurability:
  - Added parameters C_LOCKSTEP_SLAVE and C_AVOID_PRIMITIVES.
  - Updated AXI and cache data width parameters to add 512 bits.
- Chapter 3 - Stack Convention
  - Clarified calling convention.

Changes in v8.10.a, introduced in 13.1

13.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Count Leading Zeros (CLZ) instruction
- Memory Barrier (MBAR) instruction
- Stack overflow and underflow detection
- Parameter to allow AXI4-Stream/FSL instructions in user mode
- Added full support for virtex7 and kintex7 families

Resolved issues:

- Avoid reading incorrect data with simultaneous data cache invalidation with AXI interconnect [CR<582723>].
    - Can only occur when area optimization is enabled, C_DCACHE_USE_WRITEBACK is not set, and C_INTERCONNECT is set to 2
    - Versions that have this issue: v8.00.b, v8.00.a
- Ensure that data cache invalidation always takes effect before subsequent memory access [CR<582776>].
    - Can only occur when data cache is enabled when invalidated
    - Versions that have this issue: v8.00.a, 7.30.b, 7.30.a, 7.20.d, 7.20.c, 7.20.b, 7.20.a
- Fixed instruction stream prefetch to avoid fetching wrong instructions with AXI interconnect in rare cases [CR<582776>].
    - Can only occur when instruction cache streams are enabled, and C_INTERCONNECT is set to 2
    - Versions that have this issue: v8.00.b, v8.00.a

Known Issues / Limitations:

- None

13.1 - Changes in tool interface files (.mpd)

- Added parameter C_MMU_PRIVILEGED_INSTR to allow AXI4-Stream/FSL in user mode
- Added parameter C_USE_STACK_PROTECTION to activate stack underflow and overflow detection
- Added parameters and ports to support user signals on AXI cache interfaces

13.1 - Changes in Tcl script files associated with core (.tcl)

- Use AXI interconnect as default for new instances from 7 series target architectures
- Added DRC to check limitations of C_DCACHE_DATA_WIDTH and C_ICACHE_DATA_WIDTH
- Added DRC to disallow unreasonable cache sizes with C_DCACHE_FORCE_TAG_LUTRAM and C_ICACHE_FORCE_TAG_LUTRAM
- Automatically enable fault tolerance if ECC is enabled on an LMB BRAM controller
- Added DRC to check for correct LMB and LMB BRAM controller version when fault tolerance is enabled
- Added DRC to check that both or none of the LMB BRAM controllers use ECC

13.1 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Added v8.10 features in Table 1-1 Configurable Feature Overview.
- Chapter 1 - Instructions:
  - Added new CLZ and MBAR instructions to MicroBlaze Instruction Set Summary in Table 1-5.
- Chapter 1 - Registers:
  - Added Stack Protection Violation exception to ESR.
  - Added new Stack High and Stack Low registers.
  - Added C_USE_STACK_PROTECTION and C_MMU_PRIVILEGED_INSTR to PVR.
  - Added v8.10.a to MicroBlaze release version code in PVR.
  - Added new target architectures to PVR.
- Chapter 2 - MicroBlaze Core Configurability:
  - Added parameters C_USE_STACK_PROTECTION and C_MMU_PRIVILEGED_INSTR.
  - Added parameters and ports for user signals on AXI cache interfaces.
- Chapter 4:
  - Added new instructions CLZ and MBAR.
  - Updated MFS and MTS instructions with Stack High and Stack Low registers.
  - Corrected cycle count for WDC instruction.

Changes in v8.00.b, introduced in 12.4

12.4 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Parameters to enable use of AXI exclusive access with atomic load/store instructions

Resolved issues:

- Fixed cache fault tolerance to avoid inadvertent protection of distributed RAM [CR<573203>].
  - Can only occur when C_FAULT_TOLERANT is set to 1
  - Versions that have this issue: v8.00.a
- Fixed data cache stall when using AXI interconnect due to full write buffer [CR<574443>].
  - Can only occur when C_INTERCONNECT is set to 2 and C_AREA_OPTIMIZED is set to 1
  - Versions that have this issue: v8.00.a
- Ensure that debug watchpoints are not missed when directly followed by a branch [CR<576079>].
  - Can only occur when C_AREA_OPTIMIZED is set to 0
  - Versions that have this issue: v8.00.a, v7.30.b, v7.30.a, v7.20.d, v7.20.c, v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a
- Fixed issue with instruction cache streams rarely causing incorrect instruction sequences [CR<577823>].
  - Can only occur when C_ICACHE_STREAMS is set to 1
  - Versions that have this issue: v8.00.a, v7.30.b, v7.30.a
- Ensure that instruction cache is always correctly invalidated when using victim cache [CR<578267>].
  - Can only occur when C_ICACHE_VICTIMS is not set to 0
  - Versions that have this issue: v8.00.a, v7.30.b, v7.30.a
- Fixed stall due to LWX for AXI [CR<576826>].
  - Can only occur when C_M_AXI_DC_EXCLUSIVE_ACCESS is set to 1
  - Versions that have this issue: v8.00.a
- Avoid incorrect handling of data cache read accesses in rare cases when using AXI interconnect [CR<578518>].
  - Can only occur for Spartan 6
  - Can only occur when C_INTERCONNECT is set to 2 and C_DCACHE_USE_WRITEBACK is set to 1
  - Versions that have this issue: v8.00.a
- Changed AXI cache interfaces to not use thread IDs, to fix issue with out-of-order read access completion [CR<578941>].
  - Can only occur when C_INTERCONNECT is set to 2 and C_ICACHE_STREAMS is set to 1

    - Versions that have this issue: v8.00.a
- Prevent stall due to incorrect handling of data cache write data [CR<581314>].
    - Can only occur when C_INTERCONNECT is set to 2 and C_DCACHE_DATA_WIDTH are set to 1
    - Versions that have this issue: v8.00.a

Known Issues / Limitations:

- None

12.4 - Changes in tool interface files (.mpd)

- Changed default AXI protocol to AXI4LITE for C_M_AXI_IP and C_M_AXI_DP
- Allow use of instruction streams with AXI
- Added AXI4-Stream protocol parameters and renamed AXI4-Stream bus standard

12.4 - Changes in Tcl script files associated with core (.tcl)

- Select AXI4 protocol for C_M_AXI_DP when exclusive access used

12.4 - Changes in documentation associated with core

- Chapter 1 - Registers:
    - Added v8.00.b to MicroBlaze release version code in PVR.
- Chapter 2 - MicroBlaze I/O Overview:
    - Changed peripheral AXI bus interfaces, to indicate when AXI4-Lite is used.
- Chapter 2 - Advanced eXtensible Interface (AXI) Description:
    - Extended to cover AXI interface usage.
- Chapter 2 - MicroBlaze Core Configurability:
    - Added description of parameters to enable use of AXI exclusive access.
    - Added AXI4-Stream protocol parameters
- Chapter 4 - Instructions
    - Updated description of lwx and swx instructions for AXI exclusive access.

Changes in v8.00.a, introduced in 12.3

12.3 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- AXI interfaces added for peripherals and cache
- AXI stream interfaces added as alternative to FSL
- LMB bus upgraded to support error detection and correction
- Fault tolerant features: Protection of Instruction Cache, Data Cache, MMU, and Branch Target Cache Block RAMs
- Endianness selected according to bus interface: Little-endian for AXI and big-endian for PLBv46
- Reversed endian load/store instructions, and support for reversed endian MMU pages
- Parameters to force use of distributed RAM instead of Block RAM for cache tags
- Configurable cache width for AXI

Resolved issues:

- Fixed stream cache overwrite issue causing execution of incorrect instructions in rare cases [CR<567809>].
    - Can only occur when C_ICACHE_STREAMS is set to 1
    - Versions that have this issue: v7.30.a, v7.30.b
- Fixed stall due to instruction TLB miss for address with entry in Branch Target Cache [CR<567827>].
    - Can only occur when C_BRANCH_TARGET_CACHE is set to 1, and C_USE_MMU is set to 3
    - Versions that have this issue: v7.30.a, v7.30.b
- Fixed failure to invalidate instruction cache with WIC in some cases [CR<568393>]
    - Can only occur when C_ICACHE_VICTIMS is greater than 0
    - Versions that have this issue: v7.30.a, v7.30.b

Known Issues / Limitations:

- None

12.3 - Changes in tool interface files (.mpd)

- AXI interfaces and parameters added
- Fault tolerance parameter and error signal added
- Endianness parameter added
- Option to generate timing constraints added

12.3 - Changes in Tcl script files associated with core (.tcl)

- AXI interface design rule checks and parameter updates added
- Generate timing constraints for reset and interrupt signals when AXI is used

12.3 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Changed Figure 1-1 to add AXI interfaces.
  - Added v8.00 to Configurable Feature Overview in Table 1-1.
- Chapter 1 - Data Types and Endianness:
  - Added description of little endian data formats.
- Chapter 1 - Instructions:
  - Added reversed endian instructions lbur, lhur, lwr, sbr, shr, and swr.
- Chapter 1 - Registers:
  - Changed TLBHI to include description of reversed endian MMU pages.
  - Added v8.00.a to MicroBlaze release version code in PVR.
  - Changed PVR to add AXI.
- Chapter 1 - Pipeline Architecture:
  - Added description of Branch Target Cache Block RAM protection
- Chapter 1 - Memory Architecture:
  - Added AXI for memory access interface description.
  - Added description of MMU Block RAM protection.
- Chapter 1 - Hardware Exceptions:
  - Added AXI and handling of LMB errors to bus exception descriptions.
  - Added description of missed exceptions with fault tolerance enabled.
- Chapter 1 - Instruction Cache:
  - Added caching over AXI.
  - Added description of parameter to force use of distributed RAM for tags.
- Chapter 1 - Data Cache:
  - Added caching over AXI.
  - Added description of parameter to force use of distributed RAM for tags.
- Chapter 2 - MicroBlaze Core Configurability:
  - Added description of AXI.
- Chapter 2 - Overview:
  - Added AXI bus interfaces.
- Chapter 2 - MicroBlaze I/O Overview:
  - Added AXI bus interfaces.
  - Changed Figure 2-1 to add AXI interfaces.
  - Added AXI interface signals.
  - Added error signal.
- Chapter 2 - Advanced eXtensible Interface (AXI) Description:
  - New chapter.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description:
  - Added references to AXI.
- Chapter 2 - MicroBlaze Core Configurability:
  - Added parameters for fault tolerance and endianness.
  - Added parameters to force use of distributed RAM for cache tags.
  - Added parameters for AXI interfaces.
- Chapter 4 - Instructions

- Added description of stream AXI to get, getd, put, and putd instructions.
- Added description of reversed endian instructions lbur, lhur, lwr, sbr, shr, and swr.
- Clarified behavior of brki when used as software break [CR<567841>].

Changes in v7.30.b, introduced in 12.2

12.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Added Typical configuration to Configuration Wizard

Resolved issues:

- Ensure that software breakpoint instructions are ignored if invalid due to exceptions [CR<552376>].
- Corrected data corruption caused by data victim cache [CR<564312>].
    - Can only occur for Spartan 6.
    - Versions that have this issue: v7.30.a

Known Issues / Limitations:

- None

12.2 - Changes in tool interface files (.mpd)

- None

12.2 - Changes in Tcl script files associated with core (.tcl)

- None

12.2 - Changes in documentation associated with core

- Chapter 1 - Registers:
    - Added v7.30.b to MicroBlaze release version code in PVR.
- Chapter 1 - Reset, Interrupts, Exceptions, and Break:
    - Clarified edge sensitive interrupt behavior when interrupts are disabled [CR<549614>].

Changes in v7.30.a, introduced in 12.1

12.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- OPB interfaces removed
- Branch Target Cache (BTC)
- Configuration Wizard, replacing the current configuration dialog
- Cache performance improvements, including instruction cache stream buffers and victim caches

Resolved issues:

- Unused signals I_AddrTag and D_AddrTag removed [CR<454265>]
  - Versions that have this issue: All previous versions
- Avoid spurious memory access occurring in some cases when using RTED to leave Virtual Mode [CR<541326>].
  - Can only occur when the Memory Management Unit is used.
  - Versions that have this issue: v7.20.d, v7.20.c, v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Prevent execution from hanging when Inhibit Caching bit is set in a TLB entry [CR<548647>].
  - Can only occur when using write-back caches, when data cache is always used and when the Memory Management Unit is used.
  - Versions that have this issue: v7.20.d, v7.20.c, v7.20.b, v7.20.a

Known Issues / Limitations:

- None

12.1 - Changes in tool interface files (.mpd)

- OPB interfaces removed
- Unused signals I_AddrTag and D_AddrTag removed
- Added Branch Target Cache parameters
- Added Instruction Cache stream buffer and victim cache parameters
- Added Data Cache victim cache parameter

12.1 - Changes in Tcl script files associated with core (.tcl)

- Removed OPB design rule checks
- Added handling of Configuration Wizard

12.1 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Changed Figure 1-1 to remove OPB interfaces and add BTC.
  - Added v7.30 to Configurable Feature Overview in Table 1-1.
  - Added BTC and cache improvement parameters to Table 1-1.
- Chapter 1 - Registers:
  - Changed bit 31 in MSR to Reserved, and removed footnote.
  - Added v7.30.a to MicroBlaze release version code in PVR.
  - Changed PVR to remove OPB and add BTC parameters.
- Chapter 1 - Pipeline Architecture:
  - Added description of Branch Target Cache
- Chapter 1 - Memory Architecture:
  - Removed OPB for memory access interface description.
- Chapter 1 - Hardware Exceptions:
  - Removed OPB for bus exception descriptions.
- Chapter 1 - Instruction Cache:
  - Removed references to OPB.
  - Added sections describing stream buffers and victim cache.
- Chapter 1 - Data Cache:
  - Removed references to OPB.
  - Added section describing victim cache.
- Chapter 2 - Overview:
  - Removed OPB bus interfaces
- Chapter 2 - MicroBlaze I/O Overview:
  - Changed Figure 2-1 to remove OPB interfaces and add BTC.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description:
  - Removed references to OPB.
- Chapter 2 - MicroBlaze Core Configurability:
  - Removed OPB parameters.
  - Added BTC and cache improvement parameters.
- Chapter 4 - Updated latency values with BTC branch prediction.

Changes in v7.20.d, introduced in 11.4

11.4 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Avoid synthesis error for Spartan 3 with 64K cache sizes [CR<532062>].
  - Can only occur for cache sizes that do not fit in Spartan 3 devices.
  - Versions that have this issue: v7.20.c
- Added directive as work-around for tool issue, to ensure register file is not synthesised as BRAM [CR<534438>].
  - Can only occur for Spartan 3 and Virtex 4 families.
- Ensure that the DZO flag in MSR is always set for Divide Overflow [CR<534418>]
  - Can only occur when area optimization is not enabled, and when not using divide exception.
  - Versions that have this issue: v7.20.c, v7.20.b, v7.20.a
- Corrected Trace_Reg_Write to ensure that the signal is not set for WDC and WIC instructions.
  - Can only occur when area optimization is enabled, and when using caches.
  - Versions that have this issue: v7.20.c, v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Prevent data outside the cacheable range from being written to cache [CR<535252>].
  - Can only occur with C_DCACHE_USE_WRITEBACK set and when area optimization is not enabled.
  - Versions that have this issue: v7.20.c, v7.20.b, v7.20.a
- Ensure that MicroBlaze does not read incorrect data from Block RAM [CR<529810>]
  - Can only occur for Virtex 6 family
  - Versions that have this issue: v7.20.c, v7.20.b
- Corrected WDC instruction for writeback cache, to ensure that the correct cache line is always indicated [CR<536235>].
  - Can only occur with C_DCACHE_USE_WRITEBACK set, when using the Memory Management Unit and virtual mode is selected.
  - Versions that have this issue: v7.20.c, v7.20.b, v7.20.a
- Avoid reading incorrect data from data cache directly after disabling cache under rare circumstances [CR<536525>].
  - Can only occur with C_DCACHE_ALWAYS_USED and with C_DCACHE_LINE_LEN set to 8.
  - Versions that have this issue: v7.20.c, v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a

Known Issues / Limitations:

- None

11.4 - Changes in tool interface files (.mpd)

- None

11.4 - Changes in Tcl script files associated with core (.tcl)

- None

11.4 - Changes in documentation associated with core

- Chapter 1 - Registers:
  - Added v7.20.d to MicroBlaze release version code in PVR.
- Chapter 1 - Pipeline Architecture:
  - Added information about prefetch buffer handling with self-modifying code.
- Chapter 1 - Reset, Interrupts, Exceptions and Break:
  - Added description of exception priority.
- Chapter 4 - Improved description of WDC and WIC instructions, including corrections of pseudo code.

Changes in v7.20.c, introduced in 11.3

11.3 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected Trace_Jump_Taken to ensure that the signal is always generated when a jump occurs.
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that erroneous interrupt, break or exception can not not occur after reset [CR<521839>].
    - Versions that have this issue: v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Improved usable range of cache sizes with MMU enabled, to allow all available sizes.
    - Versions that have this issue: v7.20.b, v7.20.a, v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Removed INIT attributes to avoid warning messages in synthesis [CR<521455>].
    - Versions that have this issue: All previous versions

Known Issues / Limitations:

- None

11.3 - Changes in tool interface files (.mpd)

- None

11.3 - Changes in Tcl script files associated with core (.tcl)

- None

11.3 - Changes in documentation associated with core

- Chapter 1 - Registers:
    - Added v7.20.c to MicroBlaze release version code in PVR.
    - Corrected parameter name C_UNALIGNED_EXCEPTIONS [CR<518814>].
- Chapter 2 - MicroBlaze Core Configurability:
    - Corrected parameter name C_UNALIGNED_EXCEPTIONS [CR<518814>].

- Chapter 4: Corrected description of registers for XORI instruction [CR<523344>].

Changes in v7.20.b, introduced in 11.2

11.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Added full support for spartan6 and virtex6 families.

Resolved issues:

- Corrected erroneous instruction bus exception when writing TLB registers [CR<518606>].
    - Can only occur with C_ICACHE_ALWAYS_USED set to 1, when using the Memory Management Unit, instruction cache, and IPLB bus exception.
    - Versions that have this issue: v7.20.a

Known Issues / Limitations:

- None

11.2 - Changes in tool interface files (.mpd)

- None

11.2 - Changes in Tcl script files associated with core (.tcl)

- None

11.2 - Changes in documentation associated with core

- Chapter 1 - Registers:
    - Added v7.20.b to MicroBlaze release version code in PVR.
    - Added Spartan 6 and Virtex 6 to target architectures in PVR.
    - Added a section on Software Support for the Floating Point Unit [CR<498913>].
- Chapter 2 - MicroBlaze Core Configurability:
    - Added spartan6 and virtex6 to C_FAMILY.
    - Corrected EDK Tool Assignment for C_INTERRUPT_IS_EDGE and C_EDGE_IS_POSITIVE [CR<507335>].
    - Clarified that user can override EDK Tool Assignment for C_ICACHE_INTERFACE and C_DCACHE_INTERFACE.

Changes in v7.20.a, introduced in 11.1

11.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Writeback cache option
- Atomic memory access instructions LWX and SWX

Resolved issues:

- Improved data cache to handle the reception of of two cachelines back-to-back [CR<479952>].
    - This issue can not occur in any system with Xilinx Memory Controllers.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Corrected BTR which could get incorrect value when a a branch with a exception jumps to another branch [CR<479971>].
    - Can only occur when using exceptions.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected setting of EIP and EE in MSR for interrupt and FSL exception occurring simultaneously [CR<480637>].
    - Can only occur when using extended FSL instructions and FSL exception.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Corrected FSL GET instruction, which in some cases could return inconsistent data when preceded by a floating point, divide or load/store instruction [CR<496848>].
    - Can only occur when extended FSL instructions are not used.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that exception followed by a virtual address translation using the UTLB or a register access to MMU registers is always handled correctly [CR<497400>].
    - Can only occur when using FPU exception, integer divide exception or data bus exception. Can only occur when using the Memory Management Unit.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Prevent incorrect write to register after divide-by-zero [CR<497926>].
    - Only occurs if the instruction following the divide should not do a register write, such as a store instruction.
    - Can only occur with area optimization enabled and when integer divide exception is not used.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a
- Prevent fetching incorrect instruction, which could occur when disabling the instruction cache while a cache line was being read from memory [CR<502099>].
    - Can only occur when using instruction cache with C_ICACHE_ALWAYS_USED set to 1.
    - Versions that have this issue: v7.10.d, v7.10.c, v7.10.b, v7.10.a

Known Issues / Limitations:

- None

11.1 - Changes in tool interface files (.mpd)

- GUI_PERMIT qualification added to parameters not needed in MUI file
- Added parameter C_DCACHE_USE_WRITEBACK to select new writeback cache option
- Added parameters C_ICACHE_INTERFACE and C_DCACHE_INTERFACE to select XCL protocol
- Default value for C_FAMILY changed to virtex5
- Added ASSIGNMENT=REQUIRE to CLK port

11.1 - Changes in Tcl script files associated with core (.tcl)

- Clarified error message for non standard LMB slave
- Improved warning message formatting
- Changed from warning to error message for 2kB and 4kB cache size in Spartan3 and 3E families
- Added possibility to override 2kB and 4kB cache size error message for Spartan3 and 3E families
- Updated DRC for cache line length to handle MPMC dual XCL interface
- Added DRC to check that correct XCL protocol is used with writeback data cache
- Added DRC to check that connected Memory Controller can handle selected XCL protocol
- Added automatic update of C_DCACHE_INTERFACE to use correct XCL protocol with writeback data cache
- Removed check that CLK port is connected
- Reordered code to move system level DRC to SYSLEVEL_DRC_PROC [CR<500074>].

11.1 - Changes in documentation associated with core

- Chapter 1 - Overview: Added v7.20 in Table 1-1 Configurable Feature Overview, including new write-back cache feature.
- Chapter 1 - Instructions:
    - Added new LWX, SWX and WDC.FLUSH instructions to MicroBlaze Instruction Set Summary in Table 1-5.
    - New Semaphore Synchronization section, describing use of new LWX and SWX instructions.
- Chapter 1 - Registers:
    - Added description of division overflow handling, including changes in MSR and ESR.
    - Changed description of W bit in TLBLO to show use with write-back data cache.

    - Added v7.20.a to MicroBlaze release version code in PVR.
    - Added new configurable write-back data cache feature to PVR.
    - Removed Virtex-II Pro from target architectures in PVR.
- Chapter 1 - Memory Architecture: Added information about latency with write-back data cache.
- Chapter 1 - Reset, Interrupts, Exceptions, and Break:
    - Added note when LWX/SWX reservation bit is cleared.
    - Added description of division overflow.
- Chapter 1 - Instruction Cache: Removed requirement that the cache is disabled when WIC is executed.
- Chapter 1 - Data Cache: Added description of write-back and write-through caching policy in the data cache.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description
    - Changed description to reflect use of linear fetch order or critical word first.
    - Added description of new write burst encoding used with write-back data cache.
- Chapter 2 - MicroBlaze Core Configurability: Updated with changes introduced in MicroBlaze v7.20.
- Chapter 3 - Register Usage Conventions: Clarified compiler use of R18.
- Chapter 4:
    - Defined handling of LWX/SWX reservation bit by BRK and BRKI.
    - Changed description of IDIV to show the new handling of divide overflow.
    - Added new instructions LWX and SWX.
    - Clarified requirement on instruction preceding MFS.
    - Defined restriction on immediate value for MSRCLR and MSRSET when not using MMU.
    - Added definition of WDC.FLUSH and WDC.CLEAR used with write-back data cache.
    - Removed restriction that data and instruction caches must be disabled when using WDC and WIC, respectively.

Changes in v7.10.d, introduced in 10.1.3

10.1.3 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Added support for qvirtex4 and qrvirtex4 families.

Resolved issues:

- Corrected use of parameter C_RESET_MSR when only using XCL to access memory [CR<473377>].
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected debug stop handling to prevent instruction load to incorrect cache address [CR<474571>].
    - Can only occur when using the Memory Management Unit.
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Ensure that access of TLB register in virtual mode always work correctly [CR<477031>].
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Corrected PVR 3 to show 16 FSL links [CR<477032>].
    - Only occurs when using 16 FSL links.
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Prevent PID register from being incorrectly updated after an exception has occurred [CR<477033>].
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a
- Corrected write of ESR when an exception occurs in an RTED delay slot [CR<477145>].
    - Can only occur when using exceptions, and cannot occur in normal code, since RTED is not used with exceptions enabled.
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected data cache byte write handling for uncommon parameter settings [CR<477146>].
    - Can only occur with area optimization and 8-word cache lines.
    - Versions that have this issue: v7.10.c, v7.10.b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a

Known Issues / Limitations:

- None

10.1.3 - Changes in tool interface files (.mpd)

- None

10.1.3 - Changes in Tcl script files associated with core (.tcl)

- Added DRC to check that cache base address and size are a power-of-two.

10.1.3 - Changes in documentation associated with core

- Chapter 1 - Registers: Added v7.10.d to MicroBlaze release version code in PVR.
- Chapter 1 - Registers: Use 5 bits for number of FSL links in PVR.
- Chapter 1 - Registers: Added QPro Virtex-4 devices to target architectures in PVR.
- Chapter 1 - Data Cache: Clarified use of Block RAM with area optimization.
- Chapter 2 - MicroBlaze Core Configurability: Updated to add QPro Virtex-4 devices.
- Chapter 4 - Corrected description of destination register use for store instructions.

Changes in v7.10.c, introduced in 10.1.2

10.1.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Improved support for Virtex 5 hardware primitives.
- Only implement interrupt, break and non-maskable break handling if used, in order to reduce area.

Resolved issues:

- Prevent instruction read on wrong address for exception followed by return [CR<469875>].
  - Can only occur when using exceptions and when using the Memory Management Unit.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Ensure that carry is correct for branch followed by MSRSET [CR<469876>].
  - Can only occur with area optimization enabled. Can never occur in compiler generated code.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Prevent prefetched illegal instruction from interfering with interrupt handling [CR<470395>].
  - Can only occur when using exceptions and with area optimization enabled. Can never occur in normal code.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a
- Corrected generation of float compare result for NaN operands [CR<470931>].
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a, v4.00.b, v4.00.a
- Corrected destination register value when setting or clearing VMS bit [CR<471040>].
  - Can only occur when using the Memory Management Unit.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Ensure that first instruction after RTED always runs in User Mode [CR<471041>].
  - Only occurs if a multi-cycle instruction is in the RTED delay slot. Can only occur when using the Memory Management Unit.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Ensure that Floating Point Status bits are sticky [CR<471198>].
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a
- Prevent incorrect write of Floating Point Status at FPU exception [CR<471199>].
  - Can only occur when using FPU exception.
  - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Prevent prefetched instruction from erroneously clearing UMS bit [CR<471827>].
  - Can only occur when using exceptions and with Memory Management Unit enabled.

    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Ensure that first instruction after RTED always uses correct address [CR<471828>].
    - Only occurs if a multi-cycle instruction is in the RTED delay slot. Can only occur when using the Memory Management Unit.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Mirror write data correctly when using 128-bit data PLB connection [CR<471963>].
    - Can only occur when using 128-bit wide PLB.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Prevent execution from hanging when data cache is always used [CR<471976>].
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v7.10b, v7.10.a
- Ensure that external break is indicated on exception trace signals [CR<471982>].
    - Can only occur when area optimization is enabled and with exceptions enabled.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Always keep assertion of Ext_NM_BRK signal until it has been served [CR<471983>].
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected execution in both LMB and cacheable memory in virtual mode [CR<472027>].
    - Only occurs when running code from LMB in virtual mode. Can only occur when using the Memory Management Unit.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- Prevent prefetched instruction from invalidating first exception handler instruction [CR<472618>].
    - Can only occur when using exceptions and with area optimization disabled. The exception must occur immediately before a WIC or WDC instruction.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that Exception Status Register DIZ bit is always correctly set [CR<472619>].
    - Can only occur when using the Memory Management Unit.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a
- When debugging, safely stop/continue, step if exception, and allow user mode access [CR<472948>].
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v7.10b, v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a

Known Issues / Limitations:

- None

10.1.2 - Changes in tool interface files (.mpd)

- Added parameters to set if interrupt, break and non-maskable break are used.
- Added valid checks for FPU exception, FSL exception, and extended FSL instructions.

10.1.2 - Changes in Tcl script files associated with core (.tcl)

- Added procedures to update parameters for interrupt, break and non-maskable break.

10.1.2 - Changes in documentation associated with core

- Chapter 1 - Registers:
  - Clarified effect of changing bits in MSR.
  - Added explanation that bits in FSR are sticky.
  - Added note that TID field is only stored in PID when not in User Mode.
  - Added v7.10.c to MicroBlaze release version code in PVR.
  - Added Automotive Spartan devices to target architectures in PVR.
- Chapter 1 - Instruction Cache: Explained size and alignment restrictions for cacheable segment.
- Chapter 1 - Data Cache: Explained size and alignment restrictions for cacheable segment.
- Chapter 4:
  - Corrected sign extend in pseudocode for BRI and ORI.
  - Corrected operand order in pseudocode for FDIV.
  - Corrected table of floating point comparison operations, to show handling of quiet and signaling NaN.
  - Corrected description of NaN handling in pseudocode for FINT.
  - Clarified requirement on instruction preceding MFS.
  - Corrected bit assignment for MSRCLR and MSRSET instructions.
  - Added note to clarify requirement on the preceding instruction for the MSR value read by MSRCLR and MSRSET.
  - Added note to clarify restriction on instructions following MTS.

Changes in v7.10.b, introduced in 10.1.1

10.1.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected reading of PVR registers with MMU enabled [CR<467312>].
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a
- Removed warnings when using DSP48E to implement multiplication [CR<457940>].
- Handle MSR read correctly after an instruction changing MSR [CR<469027>].
  - Can never occur in compiler generated code.
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a, v4.00.b, v4.00.a
- Ensure that RTED is discarded when following an instruction causing an exception [CR<469028>].
  - Can only occur when using exceptions, and cannot occur in normal code, since RTED is not used with exceptions enabled.
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Prevent write to R0 for branches with linking [CR<469241>].
  - Cannot occur in normal code, since R0 is never written by a branch with linking.
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Block prefetched return instructions from setting virtual mode [CR<469248>].
  - Cannot occur in normal code, since these instructions are only used in real mode. Can only occur when using the Memory Management Unit.
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a
- Set MSR flags correctly for service call branch with exception in delay slot [CR<469516>].
  - Can only occur when using BRALID for the service call, which should not normally be done. Can only occur when using the Memory Management Unit.
  - Versions that have this issue: v7.10.a, v7.00.b, v7.00.a

Known Issues / Limitations:

- None

10.1.1 - Changes in tool interface files (.mpd)

- None

10.1.1 - Changes in Tcl script files associated with core (.tcl)

- Improved procedure that checks the connections made to the debug interface

10.1.1 - Changes in documentation associated with core

- Chapter 1 - Clarified MMU availability when area optimization is selected.
- Chapter 1 - Registers: Added v7.10.b to MicroBlaze release version code in PVR.
- Chapter 4:
    - Clarified behavior when changing the MSR IE, EIP or BIP bits using MSRCLR, MSRSET or MTS.
    - Added information that a synchronizing branch must follow an MTS instruction changing the MSR VM bit or PID.
    - Added note about when RTED should be used.

Changes in v7.10.a, introduced in 10.1

10.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Use Xilinx Cache Link (XCL) for all I- and D-Cache Memory Accesses

Resolved issues:

- Corrected erroneously data bus access when single stepping past a load or store instruction [CR<455208>].
  - Can only occur when using exceptions and with area optimization enabled.
  - Versions that have this issue: v7.00.b, v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Corrected erroneously setting of the DZ bit for integer divide instruction during interrupt [CR<455214>].
  - Can only occur when using exceptions and integer division.
  - Versions that have this issue: v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Resolved Watchpoint not working when area optimized option selected [CR<455599>].
  - Versions that have this issue: v7.00.b, v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Corrected MicroBlaze handling cache tag valid bits when cache is turned off while it is accessed [CR<456096>].
  - Only occurs when a WDC or WIC instruction is executed after turning off the cache.
  - Versions that have this issue: v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that breakpoints are ignored while MicroBlaze is in debug stop and XMD is inserting instructions, to prevent XMD from falsely detecting breakpoints [CR<456453>].
  - Can only occur when area optimization is not enabled.
  - Versions that have this issue: v7.00.b, v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Remove Data Storage Exception generated for non load/store instructions [CR<466899>].
  - Can only occur when using the Memory Management Unit.
  - Versions that have this issue: v7.00.b, v7.00.a

Known Issues / Limitations:

- None

10.1 - Changes in tool interface files (.mpd)

- Virtex2p new default value for parameter C_FAMILY
- New parameter C_ICACHE_ALWAYS_USED, to enable the use Xilinx Cache Link (XCL) for all I-Cache Memory Accesses
- New parameter C_DCACHE_ALWAYS_USED, to enable the use Xilinx Cache Link (XCL) for all D-Cache Memory Accesses
- PORT IPLB_MRdBTerm typo corrected
- PORT DPLB_MRdBTerm typo corrected

10.1 - Changes in Tcl script files associated with core (.tcl)

- None

10.1 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Changed Figure 1-1 to show direct FSL connections.
  - Added v7.10 in Table 1-1 Configurable Feature Overview, including new feature to always use XCL for all cache memory accesses.
- Chapter 1 - Registers:
  - Added new configurable features to PVR.
  - Registers: Added v7.10.a to MicroBlaze release version code in PVR.
- Chapter 2 - MicroBlaze I/O Overview
  - Changed Figure 2-1 to show direct FSL connections.
  - Added description of direct FSL connections and corrected PLB signal name IPLB_MRdBTerm in Table 2-1 Summary of MicroBlaze Core I/O.
- Chapter 2 - Fast Simplex Link (FSL) Interface Description: Added description of direct FSL connections.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description: Added description of new feature to always use XCL for all cache memory accesses.
- Chapter 2 - MicroBlaze Core Configurability: Updated with changes introduced in MicroBlaze v7.10.

Changes in v7.00.b, introduced in 9.2.2

9.2.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected that signal on Ext_BRK was not taken if IE='1' [CR<452311>].
  - Can only occur when area optimization is not enabled.
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected reading of PVR from Xilinx Microprocessor Debugger [CR<452912>] [CR<454609>].
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Changed 64-bit multiplication to avoid incorrect result for some operand values [CR<453420>].
  - Can only occur with Spartan family.
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a
- Avoid incorrectly setting FSR on an interrupted floating-point instruction [CR<453429>].
  - Can only occur when area optimization is not enabled.
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that exceptions following an interrupt or other exception are correctly discarded [CR<453459>].
  - Can only occur when using exceptions.
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected erroneous clearing of the IE bit in MSR when an exception occurs [CR<453574>].
  - Can only occur when using exceptions, and with area optimization enabled.
  - Versions that have this issue: v7.00.a
- Corrected interrupt occurring after interrupts have been disabled [CR<454690>].
  - Can only occur when area optimization is not enabled.
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Changed signed integer division to avoid incorrect result under certain circumstances [CR<454951>].
  - Versions that have this issue: v7.00.a, v6.00.b, v6.00.a, v4.00.b, v4.00.a

Known Issues / Limitations:

- None

9.2.2 - Changes in tool interface files (.mpd)

- None

9.2.2 - Changes in Tcl script files associated with core (.tcl)

- None

9.2.2 - Changes in documentation associated with core

- Chapter 1 - Registers: Clarified that Buslock Enable in MSR is only applicable for OPB.
- Chapter 1 - Registers: Corrected EDR description.
- Chapter 1 - Registers: Added v7.00.b to MicroBlaze release version code in PVR.
- Chapter 2 - MicroBlaze I/O Overview: Corrected debug module references in Table 2-1 Summary of MicroBlaze Core I/O.
- Chapter 3 - Memory Model: Corrected document references.
- Chapter 4 - Clarified delay slot use for blocking FSL instructions.

Changes in v7.00.a, introduced in 9.2.1

9.2.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected address strobe generation for LMB with MMU enabled [CR<450631>].
    - Version that has this issue: v7.00.a

Known Issues / Limitations:

- None

9.2.1 - Changes in tool interface files (.mpd)

- None

9.2.1 - Changes in Tcl script files associated with core (.tcl)

- None

9.2.1 - Changes in documentation associated with core

- None

Changes in v7.00.a, introduced in 9.2

9.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Processor Local Bus (PLB) data and instruction side interface.
- Floating Point conversion and square root instructions.
- Memory Management Unit, MMU.
- Extended Fast Simplex Link (FSL) instructions.

Resolved issues:

- Corrected erroneously service of interrupts during exception [CR<439651>].
    - Can only occur when using exceptions, and with area optimization enabled.
    - Versions that have this issue: v6.00.b, v6.00.a, v4.00.b, v4.00.a
- Corrected inhibit of IMM instruction in conjunction with FPU instruction causing an exception [CR<441369], [CR<441114>], [CR<442298>].
    - Can only occur when using FPU exceptions.
    - Versions that have this issue: v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected erroneously implementation of 32 Kb caches in Virtex5 [CR<444167>].
    - Versions that have this issue: v6.00.b, v6.00.a
- Corrected exception trace output when a divide by zero exception is signaled on trace_exception_kind.
    - Can only occur when exceptions.
    - Versions that have this issue: v6.00.b, v6.00.a
- Corrected Reset signal connection inside MicroBlaze [CR<447698>].
    - Does not affect MicroBlaze functionality,
    - Versions that have this issue: v6.00.b, v6.00.a
- Corrected BTR reading causing the program to the wrong address when handling an unaligned exception [CR<448608>].
    - Can only occur when using area optimization.
    - Versions that have this issue: v6.00.b, v6.00.a
- Corrected erroneously executing of an invalidated FPU instruction [CR<453429>].
    - Can only occur when area optimization is enabled.
    - Versions that have this issue: v6.00.b, v6.00.a, v5.00.c, v5.00.b, v5.00.a

Known Issues / Limitations:

- None

9.2 - Changes in tool interface files (.mpd)

- Added ports and parameters for new IPLB and DPLB interface.
- Added parameter C_INTERCONNECT to select either OPB or PLB.
- Introduced new FSL direct connection DRFSL and DWFSL.
- Made MFSL and SFSL exclusive to the new DRFSL and DWFSL.
- ICACHE_FSL_IN and ICACHE_FSL_OUT removed.
- DCACHE_FSL_IN and DCACHE_FSL_OUT removed.
- Extend selection of C_USE_FPU to select new Floating Point conversion and square root instruction.
- Parameter C_DIV_ZERO_EXCEPTION only valid when C_USE_DIV = 1.
- Parameter FSL_EXCEPTION added to generate exception from FSL transaction.
- Maximum number of FSL interfaces (C_FSL_LINKS) increased to 16.
- Parameter C_USE_EXTENDED_FSL_INSTR added to enable new FSL instructions.
- Added assignment to cache addresses depending on connected IP.
- Added MMU parameters.
- Added DBG_SHIFT signal and DEBUG_RST signals.
- Added Trace_PID_Reg port.
- Added Trace_MB_Halted port.
- Changed width of port Trace_MSR_Reg.
- Changed width of port Trace_Exception_Kind.
- Added SIGIS = RST for ports RESET and DEBUG_RST [CR<437599>].

9.2 - Changes in Tcl script files associated with core (.tcl)

- Updated check of matching lmb_bram_if_cntrl to be higher than v2.10.a
- Improved procedure is_connected to also check for source of signal
- Add MPMC connections to check_icache_fsl and check_dcache_fsl procedures
- Added check that clock and reset is connected
- Updated check for debug bus interface to include new signals in bus definition
- Added check for new PLB bus
- Added warning message for cache sizes 2kB and 4kB
- Improved checks for interrupt signal connection
- Adding procedure to assign cache addresses depending on connected IP

9.2 - Changes in documentation associated with core

- Chapter 1 - Overview:
    - Changed Figure 1-1 to add optional Memory Management Unit, Data and Instruction PLB connections, and increased number of FSL connections.
    - Added v7.00 and removed older versions in Table 1-1 Configurable Feature Overview, including new features: MMU, PLB interfaces, extended FPU and FSL instructions.
- Chapter 1 - Data Types and Endianness: Added missing Half-word Data Type description.
- Chapter 1 - Instructions: Added new extended FPU and FSL instructions to

MicroBlaze Instruction Set Summary in Table 1-5.

- Chapter 1 - Registers:
  - Added description of new MMU bits in MSR, new MMU and FSL exceptions in EAR, new MMU registers, and new EDR register.
  - Added new configurable features to PVR.
  - Added v7.00.a to MicroBlaze release version code in PVR.
- Chapter 1 - Privileged Instructions: New section.
- Chapter 1 - Virtual-Memory Management: New section.
- Chapter 1 - Reset, Interrupts, Exceptions, and Break: Added description of MMU exceptions, FSL exception, and PLB interface exceptions.
- Chapter 1 - Floating Point Unit (FPU): Added description of new extended FPU instructions.
- Chapter 2 - Overview: Added description of new PLB interface.
- Chapter 2 - MicroBlaze I/O Overview:
  - Changed Figure 2-1 to add optional Memory Management Unit, Data and Instruction PLB connections, and increased number of FSL connections.
  - Added description of PLB interface signals to Table 2-1 Summary of MicroBlaze Core I/O.
- Chapter 2 - Processor Local Bus (PLB) Interface Description: New section.
- Chapter 2 - Debug Interface Description: Added information about DEBUG bus.
- Chapter 2 - Trace Interface Description: Added information about TRACE bus, and changes to support MMU.
- Chapter 2 - MicroBlaze Core Configurability: Updated with changes introduced in MicroBlaze v7.00.
- Chapter 4:
  - Included description of privileged instructions.
  - Added description of special handling for BRALID, BRK, BRKI, RTBD, RTED and RTID with MMU.
  - Added new FPU instructions FLT, FINT and FSQRT.
  - Included description of access to new MMU registers for MFS and MTS.
  - Added description of new FSL instructions, including GETD and PUTD.
  - Added new 64-bit multiplication instruction MULHSU.

Changes in v6.00.b, introduced in 9.1.1

9.1.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected jump to wrong address on interrupts/exceptions in rare cases [CR<434687>].
    - Can only occur when area optimization is not enabled and with exceptions enabled.
    - Versions that have this issue: v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Update debug status correctly for watchpoints [CR<434688>].
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Ensure that IMM instruction effect does not prevail on exceptions [CR<434692>].
    - Can only occur when area optimization is not enabled and with exceptions enabled.
    - Versions that have this issue: v6.00.a, v5.00.c, v5.00.b, v5.00.a
- Corrected integer divide [CR<435649>] [CR<435957>].
    - Can only occur when area optimization is not enabled.
    - Versions that have this issue: v6.00.a, v5.00.c, v5.00.b, v5.00.a

Known Issues / Limitations:

- None

9.1.1 - Changes in tool interface files (.mpd)

- Removed TRACE and DEBUG bus definitions [CR<435919>].
- Added attribute "RST" to port RESET.

9.1.1 - Changes in Tcl script files associated with core (.tcl)

- None

9.1.1 - Changes in documentation associated with core

- Chapter 1 - Registers: Added v6.00.b to MicroBlaze release version code in PVR.
- Chapter 1 - Registers: Added Spartan3AN to target architectures in PVR.
- Chapter 2 - Debug Interface Description: Removed DEBUG bus.

- Chapter 2 - Trace Interface Description: Removed TRACE bus.
- Chapter 2 - MicroBlaze Core Configurability: Updated to add Spartan3AN.
- Chapter 3 - Interrupt and Exception Handling: Added information that Break address location is reserved when XMD is used.

Changes in v6.00.a, introduced in 9.1

9.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- MicroCache 64-1024 bytes implemented LUT RAM in favor of BRAM
- Integer hardware multiplication handling 64-bit result
- Option to select area optimized implementation (3-stage pipeline) or performance optimized implementation (5-stage pipeline)

Resolved issues:

- Improved XCL data cache interface to accept data the cycle after the XCL request is issued.
    - This issue can not occur in any system with Xilinx Memory Controllers.
    - Versions that have this issue: v4.00.b, 4.00.a
- Removed erroneously checking of the FSL Full signal during two clock cycles [CR<428345>].
    - Versions that have this issue: v4.00.b, 4.00.a
- Corrected invalid instruction in EX during interrupt handling [CR<424337>].
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a
- Corrected register conflicts in pipeline during exception in delay slots [CR<430845>].
    - Can only occur when using exceptions.
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a
- Removed invalid breakpoint detection on flushed instructions after an exception was taken [CR<430827>].
    - Can only occur when using exceptions.
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a
- Stopped erroneously execution of invalidated FSL instruction at exception [CR<432238>].
    - Can only occur when using exceptions.
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a
- Corrected not updating of FSR due to pipeline stall in EX pipe stage [CR<432545>].
    - Can only occur when using exceptions.
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a
- Corrected Dbg_Stop input functionality [CR<432636>].
    - Versions that have this issue: v5.00.c, v5.00.b, v5.00.a

Known Issues / Limitations:

- None

9.1 - Changes in tool interface files (.mpd)

- Bus DEBUG and TRACE added.
- Parameter C_AREA_OPTIMIZED added
- Parameters C_USE_MRS_INSTR and C_USE_PCMP_INSTR reinstated from being constant enabled
- Parameter C_USE_HW_MUL range changed to include new 64-bit result option
- Parameter C_DIV_ZERO_EXCEPTION cannot be set to 1 when C_USE_DIV is 0, i.e. no HW division
- Range of parameter C_ADDR_TAG_BITS, C_CACHE_BYTE_SIZE, C_DCACHE_ADDR_TAG and C_DCACHE_BYTE_SIZE adjusted to accommodate for new cache sizes (Micro Cache)

9.1 - Changes in Tcl script files associated with core (.tcl)

- Updated error message on non-standard LMB slave
- Updated error message on required version of LMB BRAM controller
- Procedure to output warning message added
- Enhanced cache address checking
- Added check on connection of Debug interface
- Added check on enabled exception without corresponding feature in use
- Adding procedure to assign parameters C_I_OPB and C_I_LMB depending on if the buses are in use

9.1 - Changes in documentation associated with core

- Entire document: Editorial improvements and corrections, including new contents overview in each chapter.
- Chapter 1 - Overview: Added v6.00 to Configurable Feature Overview in Table 1-1, including new features: Area or speed optimized, Hardware multiplier 64-bit result, and LUT cache memory.
- Chapter 1 - Registers:
    - Added description of configuration effects on MSR bits.
    - Added new configurable features to PVR.
    - Added v6.00.a to MicroBlaze release version code in PVR.
- Chapter 1 - Pipeline Architecture: Added description of three-stage pipeline used with area optimization.
- Chapter 1 - Branches: Clarified that R17 is not valid for exceptions in delay slots.
- Chapter 1 - Memory Architecture: Added latency for area optimization, and description of 8 word cache lines.
- Chapter 1 - Reset, Interrupts, Exceptions, and Break: Corrected equivalent pseudocode for exceptions.
- Chapter 1 - Instruction Cache: Added information on LUT cache memory feature.
- Chapter 1 - Data Cache: Added information on LUT cache memory feature.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description: Added information on required wait states for XCL.

- Chapter 2 - Debug Interface Description: Added information about DEBUG bus.
- Chapter 2 - Trace Interface Description: Added information about TRACE bus.
- Chapter 2 - MicroBlaze Core Configurability: Updated with changes introduced in MicroBlaze v6.00.
- Chapter 3 - Register Usage Conventions: Added missing special registers rbtr and rpvr.
- Chapter 4:
    - Added instruction latency values applicable for area optimization.
    - Clarified allowed instruction usage in delay slots.
    - Added new 64-bit multiplication instructions MULH and MULHU.

Changes in v5.00.c, introduced in 8.2.2

8.2.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Corrected output signal MB_Halted [CR<422279>].
    - Versions that have this issue: v5.00.b, v5.00.a

Known Issues / Limitations:

- None

8.2.2 - Changes in tool interface files (.mpd)

- None

8.2.2 - Changes in Tcl script files associated with core (.tcl)

- None

8.2.2 - Changes in documentation associated with core

- Chapter 1 - Registers:
    - Added v5.00.c to MicroBlaze release version code in PVR.
    - Corrected PVR mnemonics.

Changes in v5.00.b, introduced in 8.2.1

8.2.1 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- None

Resolved issues:

- Changed all asynchronous resets in the code to be synchronous [CR<234785>].
  - Does not affect MicroBlaze functionality,
  - Version that have this issue: v5.00.a
- Fixed problem with interrupt during an IMM instruction [CR<234785>].
  - Version that have this issue: v5.00.a
- Changed FPU FDIV instruction to not depend on the C_USE_DIV parameter [CR<234703>].
  - Version that have this issue: v5.00.a
- Corrected problem with using software breakpoints with caches enabled [CR<233573>].
  - Version that have this issue: v5.00.a
- Fixed problem with delay slot in pipeline during debug sessions [CR<234785>].
  - Version that have this issue: v5.00.a

Known Issues / Limitations:

- None

8.2.1 - Changes in tool interface files (.mpd)

- None

8.2.1 - Changes in Tcl script files associated with core (.tcl)

- Error generated for unconnected XCL bus

8.2.1 - Changes in documentation associated with core

- Chapter 1 - Overview: Changed v4.00 to active in Configurable Feature Overview in Table 1-1.
- Chapter 1 - Instructions: Correction of WIC and WDC semantics in Table 1-5 MicroBlaze Instruction Set Summary.
- Chapter 1 - Registers:
  - Added v5.00.b to MicroBlaze release version code in PVR.

    - Added Spartan3A to target architectures in PVR.
- Chapter 4 - Corrected description of WIC and WDC semantics.

Changes in v5.00.a, introduced in 8.2

8.2 - Changes in VHDL/Verilog/Netlist sources (.vhd, .v, .ngc, .edn)

New Features:

- Performance version with 5-stage pipeline
- Processor Version Register, PVR
- Option to select 8 word cacheline sizes

Resolved issues:

- None

Known Issues / Limitations:

- None

8.2 - Changes in tool interface files (.mpd)

- Added attribute SYSLEVEL_UPDATE_VALUE_PROC to update parameters C_INTERRUPT_IS_EDGE and C_EDGE_IS_POSITIVE
- Added parameters C_SCO, C_DATA_SIZE, C_DYNAMIC_SIZING
- Previous options enabled by C_USE_MSR_INSTR and C_USE_PCMP_INSTR now always enabled
- Parameters to control new PVR feature introduced
- Instruction cache parameters changed to not allow the size 1024
- Parameters C_ICACHE_LIN_LEN and C_DCACHE_LIN_LEN added to allow 4 or 8 word size cacheline sizes
- Port MB_Halted added
- New Trace interface, with changes to all trace signals

8.2 - Changes in Tcl script files associated with core (.tcl)

- Added procedure syslevel_update_interrupt_edge to assure that the MicroBlaze and interrupt controller use the same type of interrupts
- Clean up old data-structure APIs

8.2 - Changes in documentation associated with core

- Chapter 1 - Overview:
  - Changed Figure 1-1 to remove IOPB and DOPB connections to caches.
  - Added v5.00 to Configurable Feature Overview in Table 1-1.
- Chapter 1 - Data Types and Endianness: Corrected Byte Data Type description in

Table 1-4.
- Chapter 1 - Instructions:
  - Minor corrections of semantics of MicroBlaze Instruction Set Summary in Table 1-5.
  - Added BTR and PVR registers to Table 1-5.
- Chapter 1 - Registers: Added description of BTR and PVR registers.
- Chapter 1 - Pipeline Architecture: Changed to describe new five-stage pipeline implementation.
- Chapter 1 - Branches: Added description of exception in delay slots.
- Chapter 1 - Memory Architecture: Changed description of memory access latency.
- Chapter 1 - Reset, Interrupts, Exceptions, and Break: Clarified exception descriptions.
- Chapter 1 - Instruction Cache: Removed IOPB caching, HW Debugging and Lock Bit.
- Chapter 1 - Data Cache: Removed IOPB caching, HW Debugging and Lock Bit.
- Chapter 2 - MicroBlaze I/O Overview: Changed Figure 2-1 to remove IOPB and DOPB connections to caches.
- Chapter 2 - On-Chip Peripheral Bus (OPB) Interface Description: Removed paragraph on bus OR-logic.
- Chapter 2 - Xilinx CacheLink (XCL) Interface Description: Added clarifications and improved Read Miss description.
- Chapter 2 - MicroBlaze Core Configurability: Updated with changes introduced in MicroBlaze v5.00.
- Chapter 3 - Register Usage Conventions: Added BTR and PVR registers.
- Chapter 4:
  - Reduced instruction latency values to reflect performance improvements.
  - Added BTR and PVR registers to MFS description.
  - Changed description of WIC and WDC to reflect new semantics.