XDF XILINX DEVELOPER FORUM

Platform Management

Presented By

Jerry Wong
System Software & SoC Solutions – Product and Technical Marketing

XILINX

Overview of Platform Management …

Part 1 of 4:

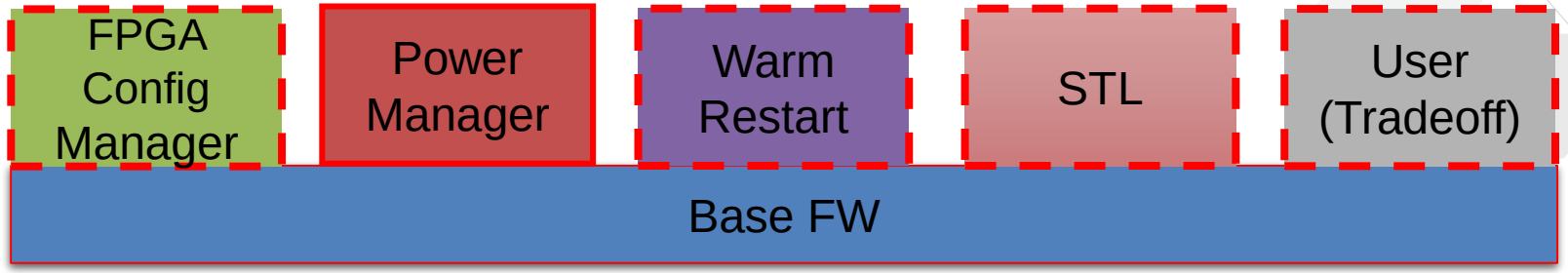
Platform Management Overview and Boot …

… Overview for those that are new to Xilinx …

Platform Management Firmware

Platform Management Contains …

- **Base Firmware**
  - Required
- **Programmable Logic Configuration Manager**
  - Optional
- **Power Management Framework**
  - Required
- **Warm Restart Manager**
  - Optional
- **Functional Safety Software Test Library (STL)**
  - Optional
- **User Firmware**
  - Optional



… Select from optional functions …

Platform Management Functions - Associated Markets

Platform Management Applied …

Platform Management Feature	Primary Markets	Secondary Markets
Boot & Configuration	All	
Security	A&D, Auto, ISM	Wired
Partial Reconfiguration	Data Center	A&D, Auto, Wired
Power Management	A&D (MILCOM, SATCOM), Auto	ISM
Reset	Wired, A&D	Auto, ISM
Functional Safety	Auto, ISM	A&D (Aerospace & Defense)
PL Health Monitor	A&D, Space, Data Center	Wired

Note: Functions can be selected up to the available 128KB RAM …

… Often “enabling” functions to various applications …

Customizing PMU Firmware

How to select Platform Management Modules …

- **Modules can be enabled in code**
  - **`xpfw_config.h`**
  - `ENABLE_PM` - Enable Power Management Module
  - `ENABLE_EM` - Enable Error Management Module
  - `ENABLE_RTC_TEST` - Enable RTC Event Handler Test Module
  - `ENABLE_SCHEDULER` - Enable Scheduler Module
  - `ENABLE_SAFETY` - Enable Safety Code

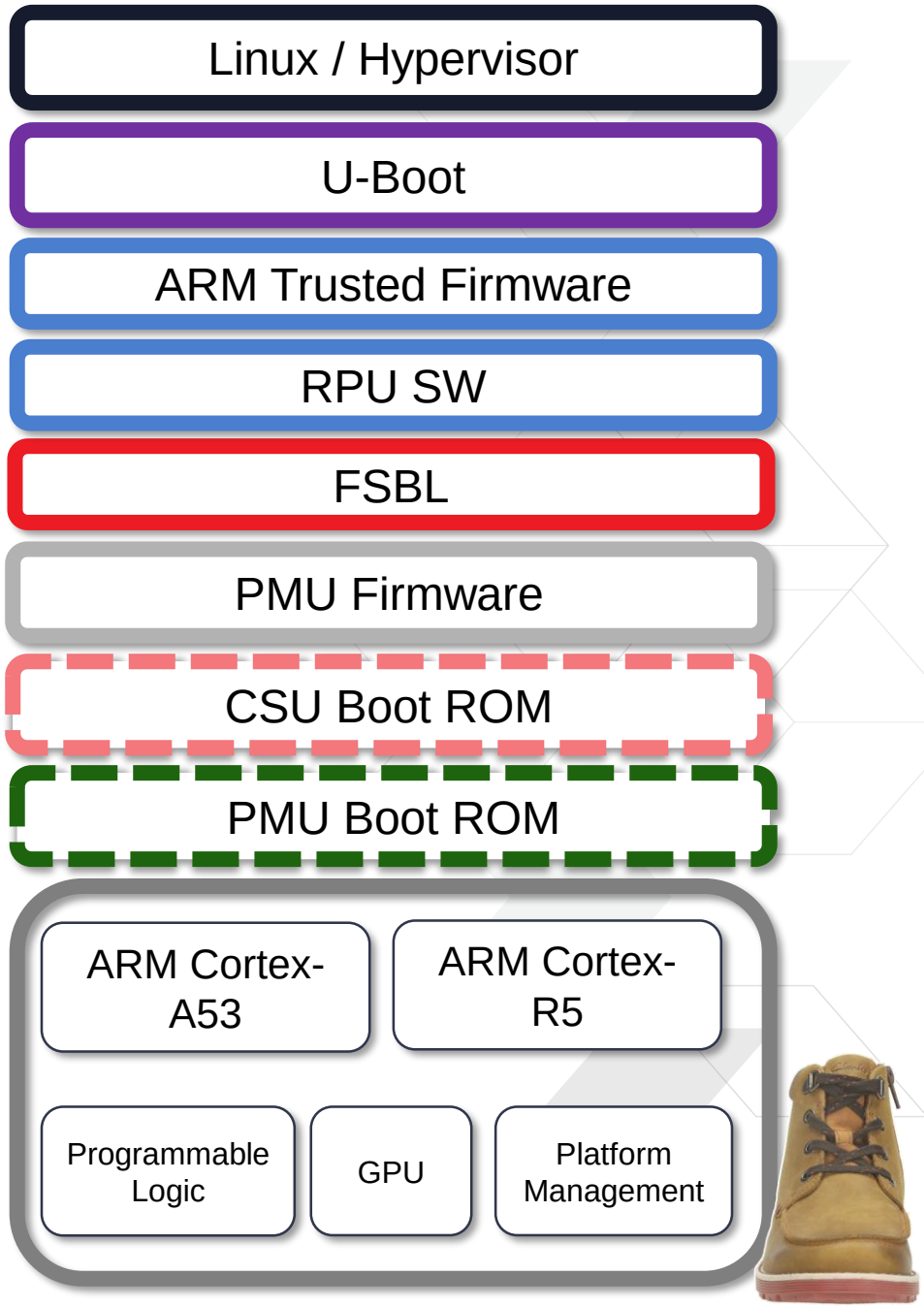
- **UART output**
  - `fw_printf()` – useful for standard debug techniques
  - Default is to print on UART0 – can be changed to UART1 in BSP settings

- **EEMI Implementation**
  - Found in `pm_core.c`

… See PMU Firmware Wiki for more …

Zynq UltraScale+ MPSoC Boot

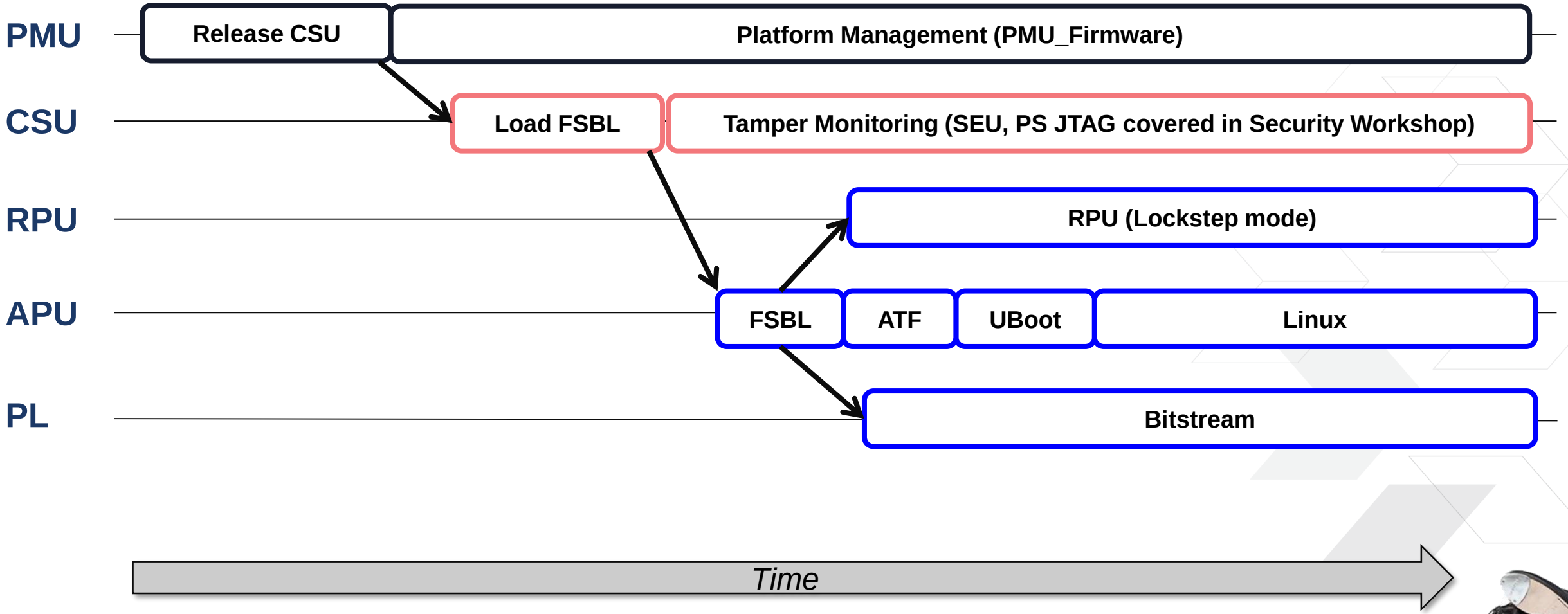
- **FSBL (First Stage Boot Loader)**
  - Configures Processing Subsystem (PS)
  - Loads Partitions - Bitstream, ATF, U-boot, & RPU-Application
- **PMU(Platform Management Unit) Firmware**
  - Provides Platform Management Services - Power Management, Restart, Safety, Error Management, PL Config
- **ATF (ARM Trusted Firmware)**
  - Mandatory component of the ARMv8 security architecture
- **U-Boot**
  - Universal Boot Loader, used by Linux Community
- **Linux / RPU-SW**
  - Design specific Software layers on APU or RPU respectively



… Boot functions in order …

An Example - Understanding Boot Levels

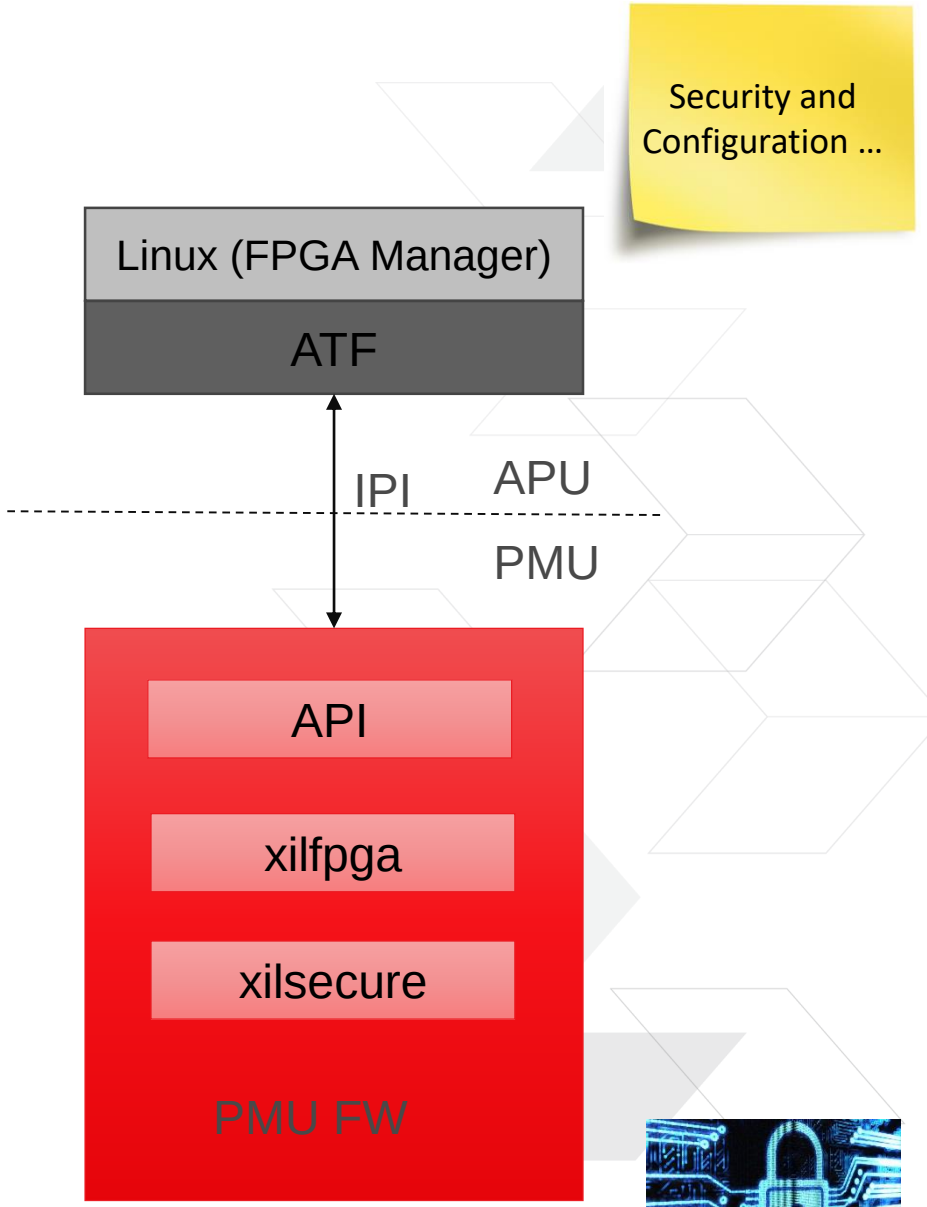
Boot Dependencies …



… Boot has various dependencies …

FPGA Configuration Manager

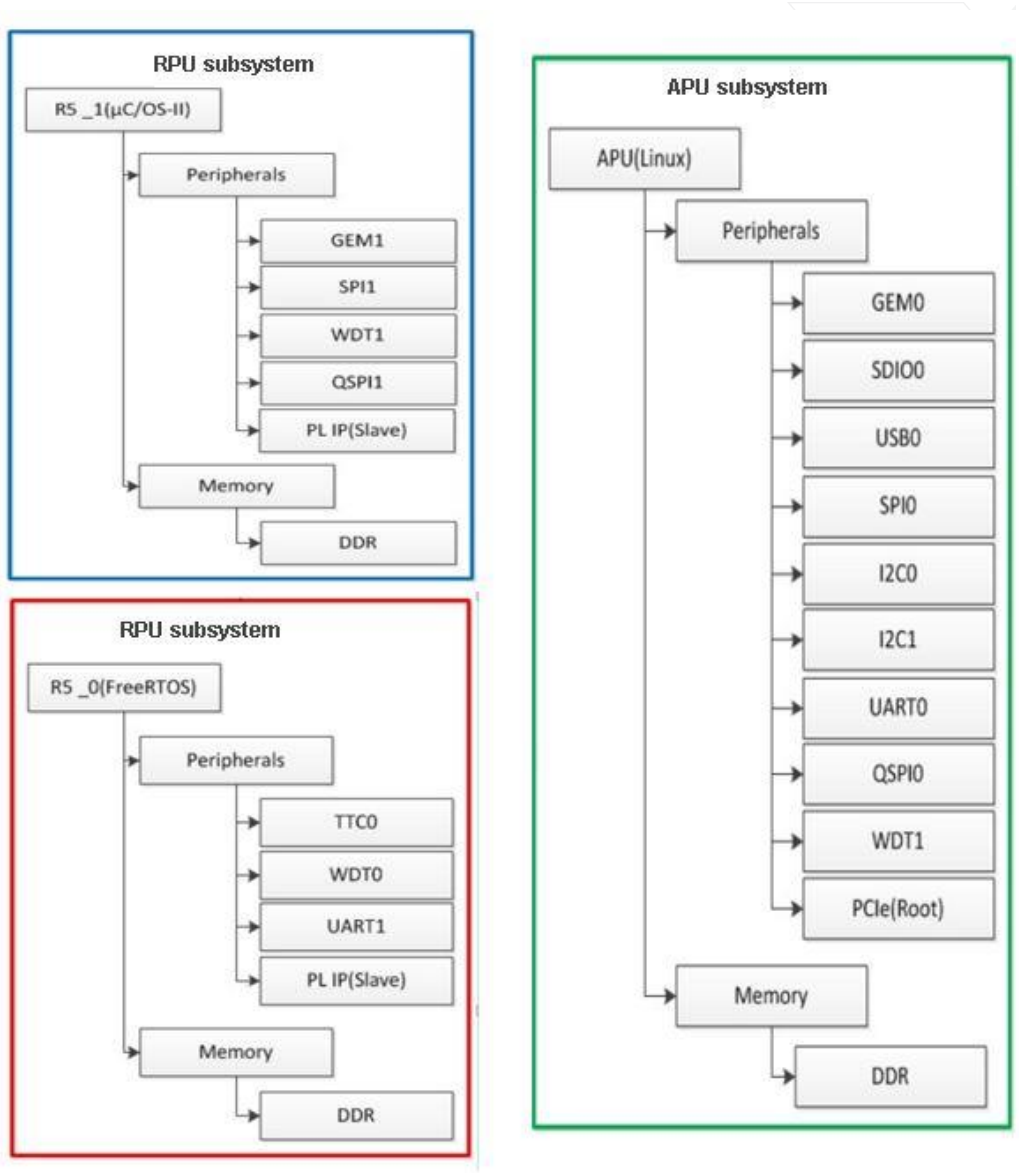
- **Use Case**
  - Secure/Non-Secure Bitstream Download from Linux/U-Boot/RPU (See Security session)
- **Two Components for FPGA Manager in PMU**
  - xilsecure – Provides an interface to access CSU resources (SHA3, AES, RSA engines)
  - xilfpga – Provides an interface for configuring PL via PCAP (Processor Configuration Access Port) from the PS
- **Summary**
  - Source available and up streamed to GitHub
  - Runs as Secure Master
  - Service can be used by A53 or R5 code
  - IPI is used as interface for the API
  - PMUFW uses xilfpga and xilsecure libraries to perform bitstream decryption, authentication and download



… Security is done during Configuration …

Isolation Configuration

- **Text and Tree Diagram applies to**
  - Power Management
  - Warm Restart
  - Safety
- **Define Subsystems based on Use-case**
  - Subsystem Restart - Restarts the subsystem from a clean state without effecting the other active subsystems
  - Subsystem idling is a function of idling of all components of a defined subsystem
- **Subsystems can be defined in Vivado via isolation configuration menu**



Associate Processors and Peripherals …

… Define a tree once in Vivado … Info is shared with other tools …

PMU: Xilinx & User Firmware

Platform Management Recap …

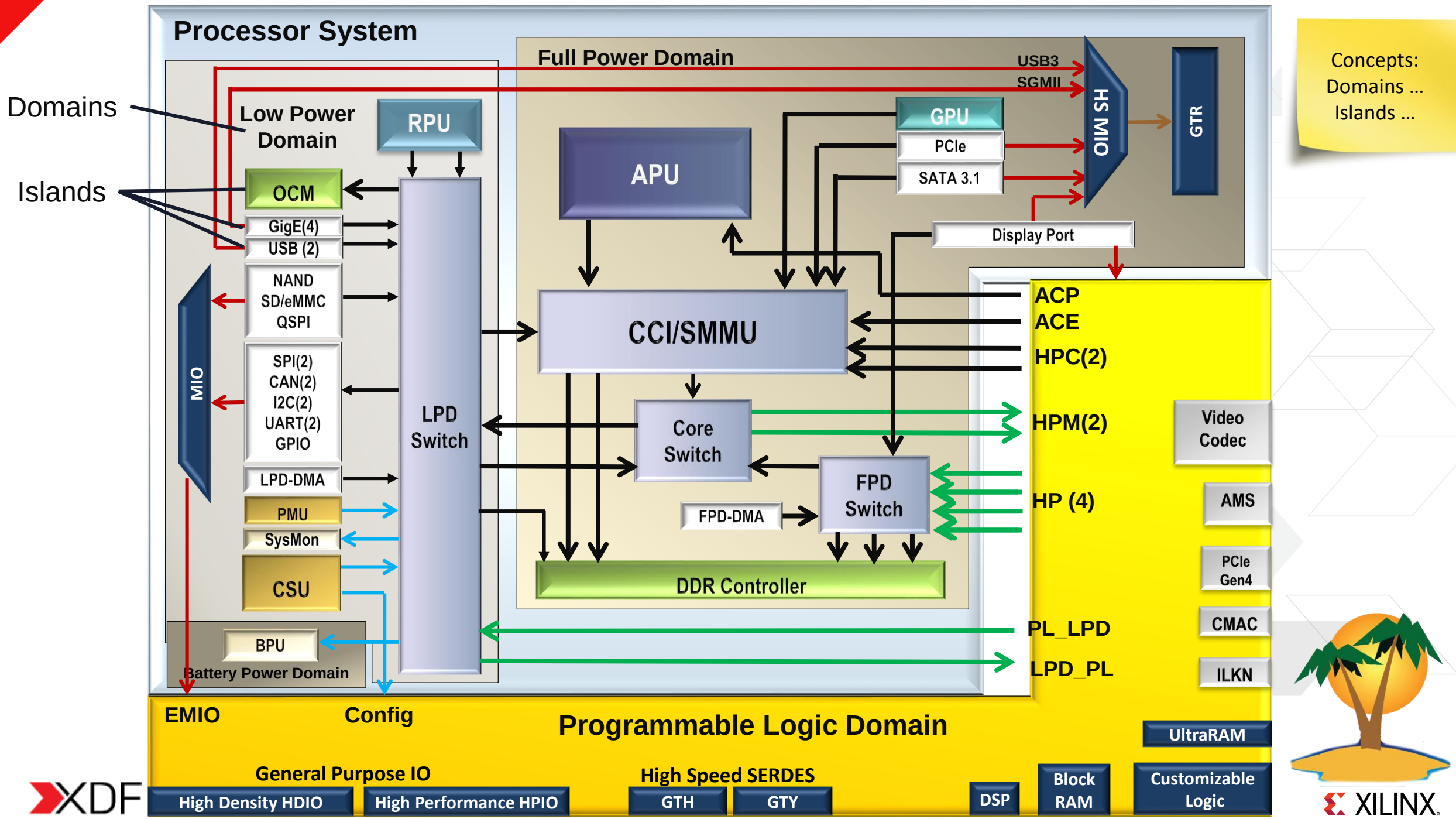
- **PMU Firmware extends the PMU ROM functionality**
  - Closely interacts with the PMU ROM as needed
  - SW Framework provided for management functions
    - For specialized applications may be customized for application specific tasks
  - Uses Inter-Processor Interrupts (IPI) standard to communicate with other on-chip Processors
- **The home for critical platform management functions:**
  - Power
  - Post boot (after initial CSU PL configuration) programmable logic configuration
  - Warm Restart
  - Functional Safety Software Test Library
- **User Code – Xilinx provides framework**
  - System error handling
  - High reliability code
  - ….
- **Loaded in PMU RAM by CSU ROM / FSBL**

… Many functions usable as-is …

Part 2 of 4:

Power Management

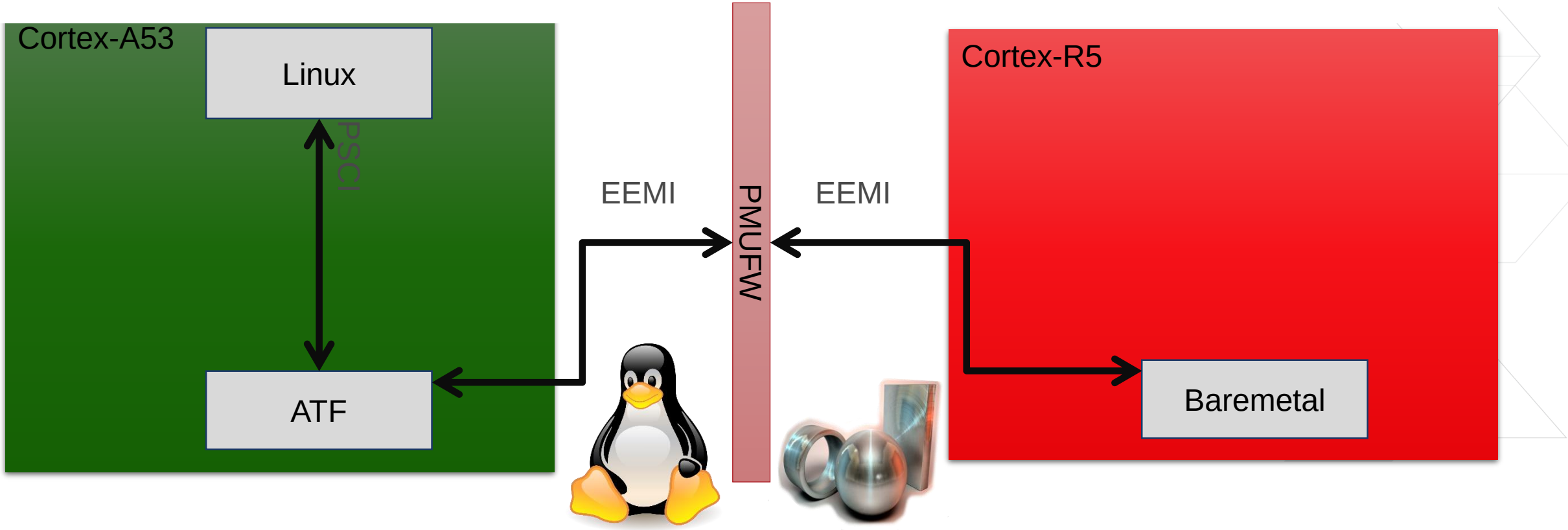
… Power state of shared peripherals managed centrally …


Processor System
Full Power Domain
Low Power Domain
Domains
Islands
RPU
APU
GPU
PCIe
SATA 3.1
USB3
SGMII
HS MIO
GTR
OCM
GigE(4)
USB (2)
NAND
SD/eMMC
QSPI
SPI(2)
CAN(2)
I2C(2)
UART(2)
GPIO
MIO
LPD-DMA
PMU
SysMon
CSU
BPU
Battery Power Domain
LPD Switch
CCI/SMMU
Core Switch
FPD Switch
FPD-DMA
DDR Controller
Display Port
ACP
ACE
HPC(2)
HPM(2)
HP (4)
PL_LPD
LPD_PL
Video Codec
AMS
PCIe Gen4
CMAC
ILKN
EMIO
Config
Programmable Logic Domain
UltraRAM
General Purpose IO
High Density HDIO
High Performance HPIO
High Speed SERDES
GTH
GTY
DSP
Block RAM
Customizable Logic
Concepts:
Domains …
Islands …
XDF
XILINX

Platform Management for Zynq UltraScale+ Devices

Platform Management Architecture …

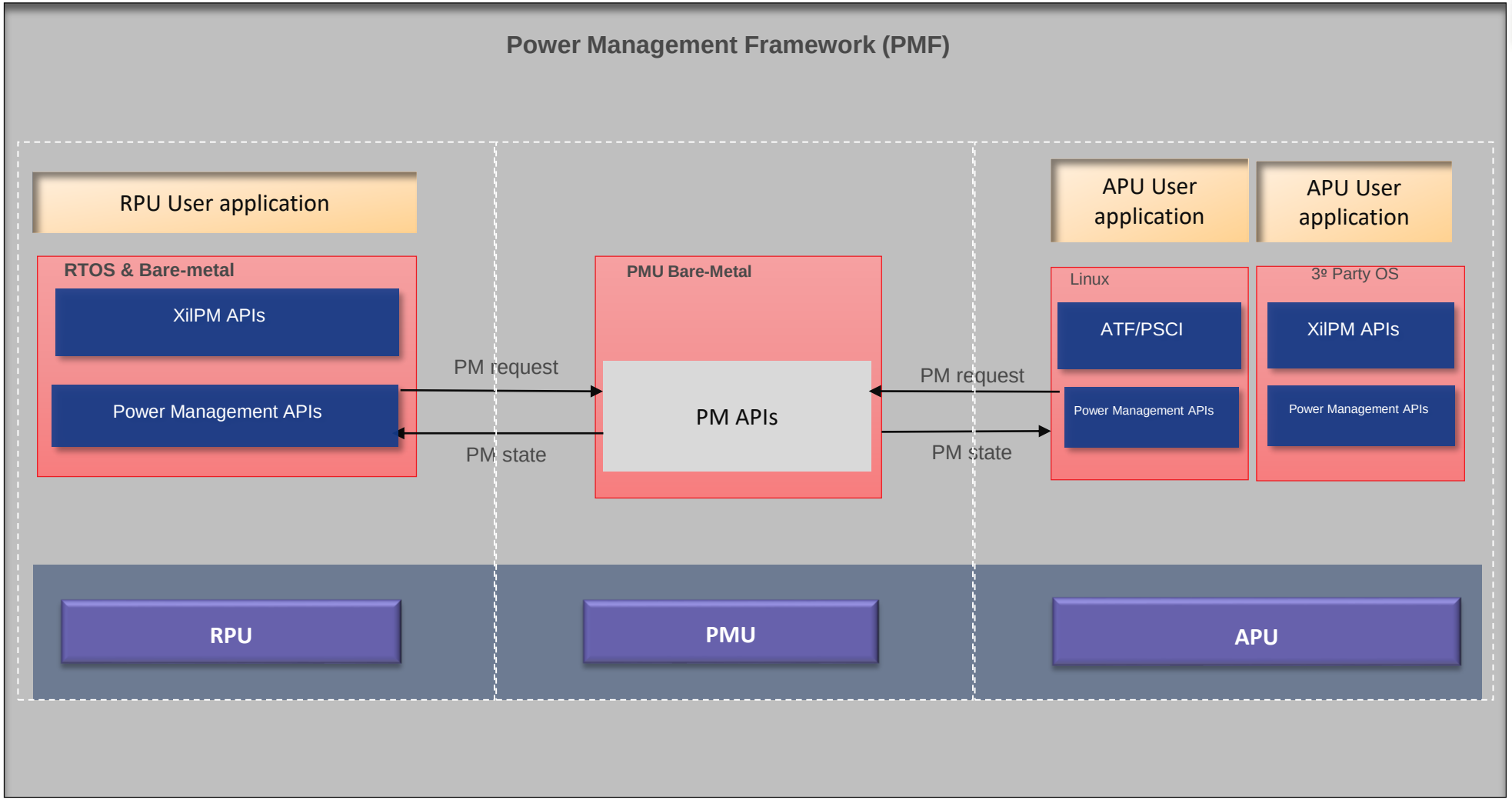
- **Dedicated Platform Management interface**
- **Key component of the Xilinx Power Management Framework**
  - Implements the core of EEMI architecture



… Platform Management is built around communication …

Platform Management Software Stack

What is communicated …



… PMU knows “state” and provides central services to all …

XILINX

Power Off Suspend to DDR

A sample power state …

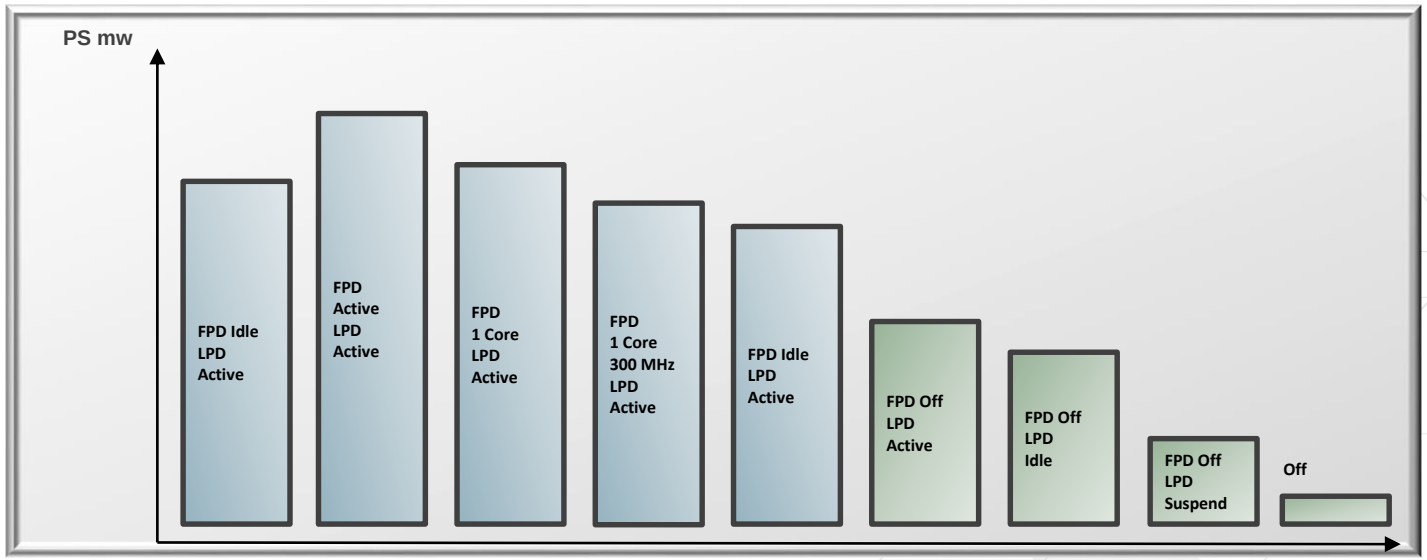
- Power Advantage Tool lets you see the power of your design (ZCU102, ZCU106, ZCU111)
- Suspend to DDR retains DDR contents via self-refresh. Allows detecting resume by the return value of XPm_GetBootStatus.
- Power Off Suspend to DDR supports very low standby power designs

… The Power Off state suspends to a nice low standby power …

What Typical Power States are Available

Other Power States …

- **Wiki example demonstrates [Typical Power States] (“Dimmer”):**
- **PS Power States:**
  - Full Performance
  - APU Hotplug Cores
  - APU Frequency Scaling
  - APU Suspend
  - FPD Off
  - RPU Suspend
  - Deep Sleep
  - Power Off Suspend



Use case / mA		2.5W	1.8W	1.6W	1.6W	0.4W	0.3W	35mW	3uW
APU, Full Power Domain (FPD)	ON	ON	1-APU ON, FPD ON	1-APU ON, FPD ON	APU OFF, FPD ON	OFF	OFF	OFF	OFF
RPU, Low Power Domain (LPD)	R5 Active, LPD ON	R5 Active, LPD ON	R5 Active, LPD ON	R5 Active, LPD ON	R5 Active, LPD ON	R5 Active, LPD ON	R5 Idle LPD ON	R5 Off, LPD ON	OFF
PL Domain (PLD)	ON	ON	ON	ON	ON	ON	ON	ON	OFF
Battery Domain (BD)	ON	ON	ON	ON	ON	ON	ON	ON	ON

… Several PS Power States that require no coding …

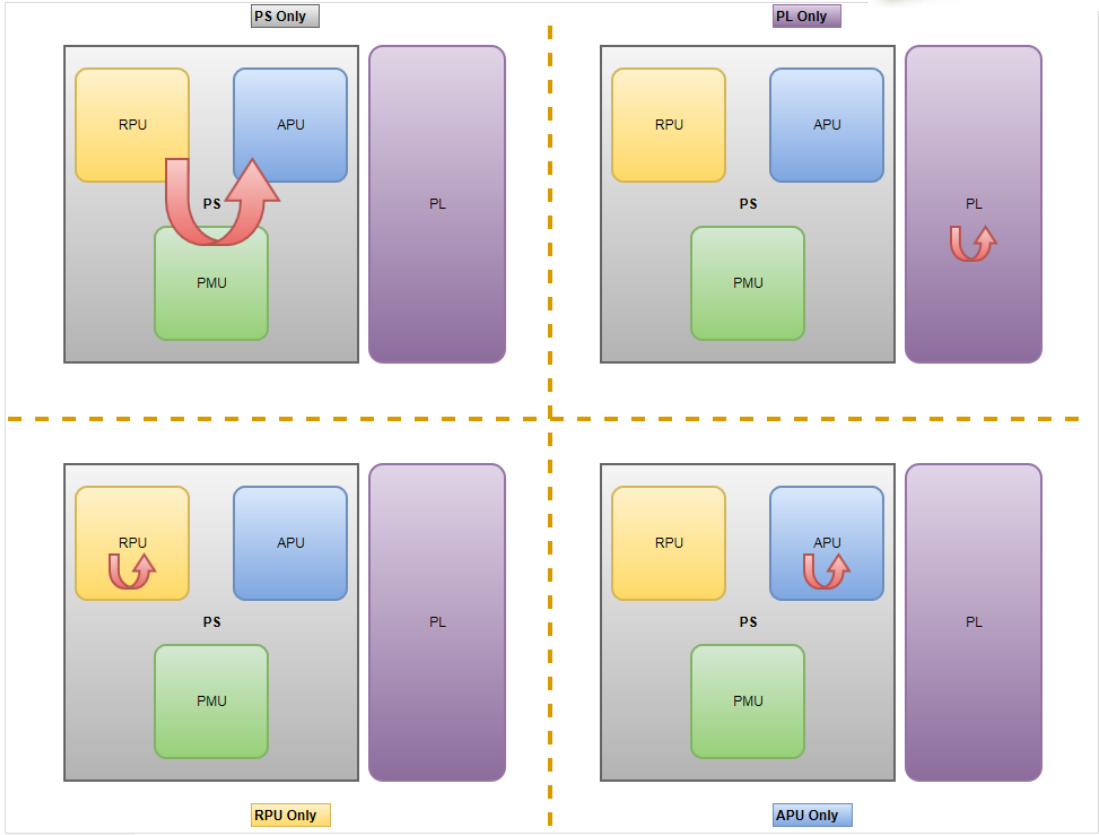
Part 3 of 4:

Warm Restart …

Warm Restart Manager

Four Warm Restart Modes …

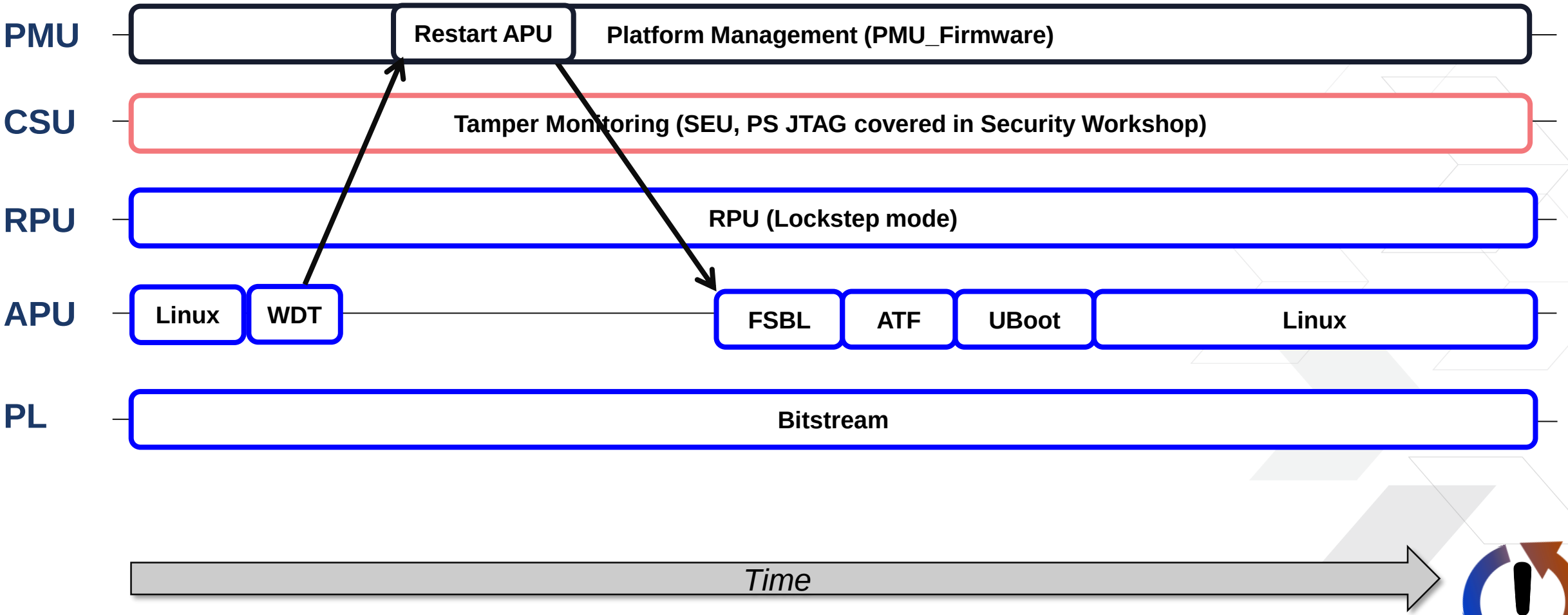
- **Use Case**
  - Independent PS/PL/APU/RPU sub-system restarts
- **Summary**
  - Enables independent sub-system restarts
    - PMU is always alive and has access to control registers
  - IPI/WDT error triggers restart
  - PMU idles down peripherals and DMAs
  - Asserts reset to subsystem
  - Loads images
    - Offloaded to resident FSBL in the case of full PS Restart
  - Releases resets



… Restart is typically used to recover from error states …

Warm Restart Example

Warm Restart Dependencies …



… Warm Restart is similar to Boot, other processors unaffected …

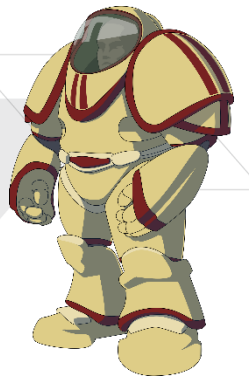
Part 4 of 4:

Functional Safety …

Safety/Reliability

Safety Features
…

- **TMR Processors in PMU**
  - Triple Modular Redundancy Voting Logic
- **Physical Diversity (R5 / PMU / CSU) Synthesized to different frequency targets**
  - Different net lists
  - Different areas
  - Different layouts
  - Different routing
- **“Early” Separation of Clocks and Resets to Individual Cores**
- **ECC**
  - ECC for PMU & CSU RAMs
- **Memory interleaving to avoid multi-bit error by SEUs (Single Event Upsets)**
  - 8:1 interleaving reduces probability of multi-bit error to nil
- **Independent memories for Data and ECC**
  - Separate address latches
  - Reduces probability of address latch corruption resulting in bad data
    - Ex. Bad address for ECC data will result in “random” ECC for correct data



… Redundancy for reliability …

Functional Safety Software Test Library (STL)

STL Features …

- **Complements hardware safety features by increasing Diagnostic Coverage**
- **APIs execute periodically for coverage of random hardware failures**
  - E.g., Register checking, Interconnect checking, Memory scrubbing etc.
- **APIs execute on user demand for latent failure coverage**
  - Ex: XMPU (Xilinx Memory Protection Unit), SysMon, error injection, etc.
  - Executes from: R5 and PMU

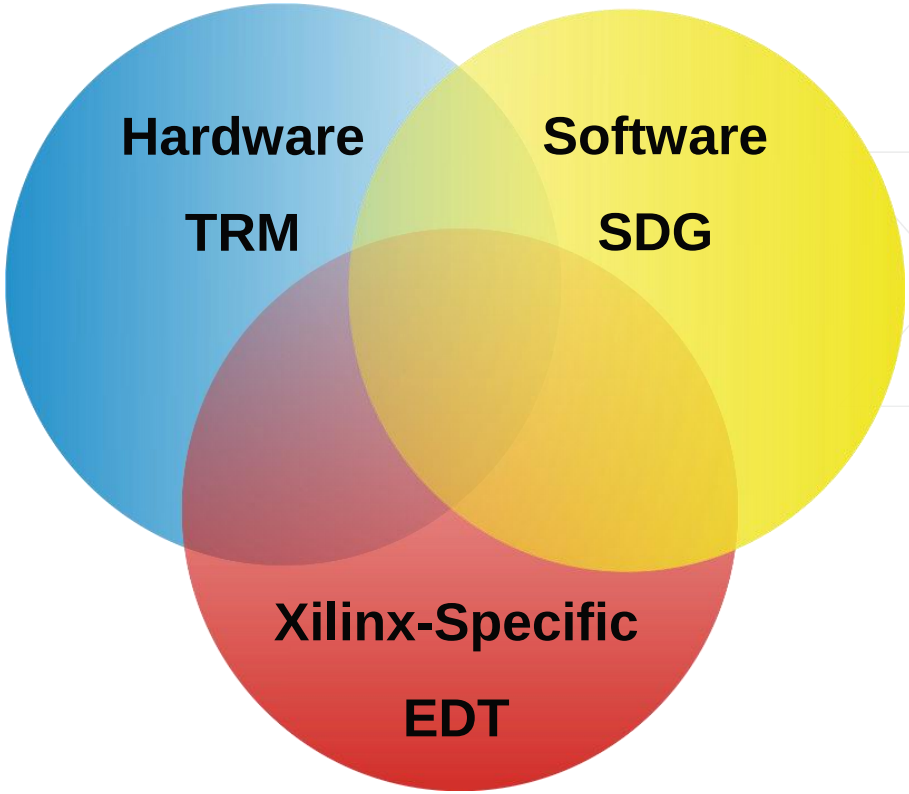
- Software Test Library Coverage
  - R5 Caches, TCMs & OCM
  - PMU RAM
  - Low Power Domain Interconnect/Switch
  - Peripherals: Ethernet, CAN & UART
  - System Monitor
  - LPD General Interrupt Controller
  - LPD DMA
  - LPD Watchdog Timer
  - Error injection into LPD memories & R5 lockstep
  - XMPU (Xilinx Memory Protection Unit), XPPU (Xilinx Peripheral Protection Unit
  - LPD reset/clock controller, LPD TTC, PMU TMR (Triple Modular Redundancy)

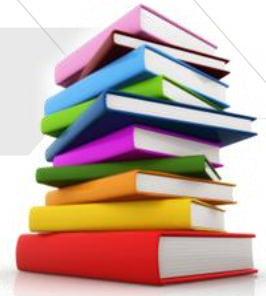
… Periodic test where there is no hardware redundancy …

The Trifecta of Embedded References

What to reference …

- **HW: Technical Reference Manual (TRM = ug1085)**
- **SW: Software Developer's Guide (SDG = ug1137)**
- **Xilinx-specific: Embedded Design Tutorial (EDT = ug1209)**





… Of the many documents … Best three to start with …

Backup Slides

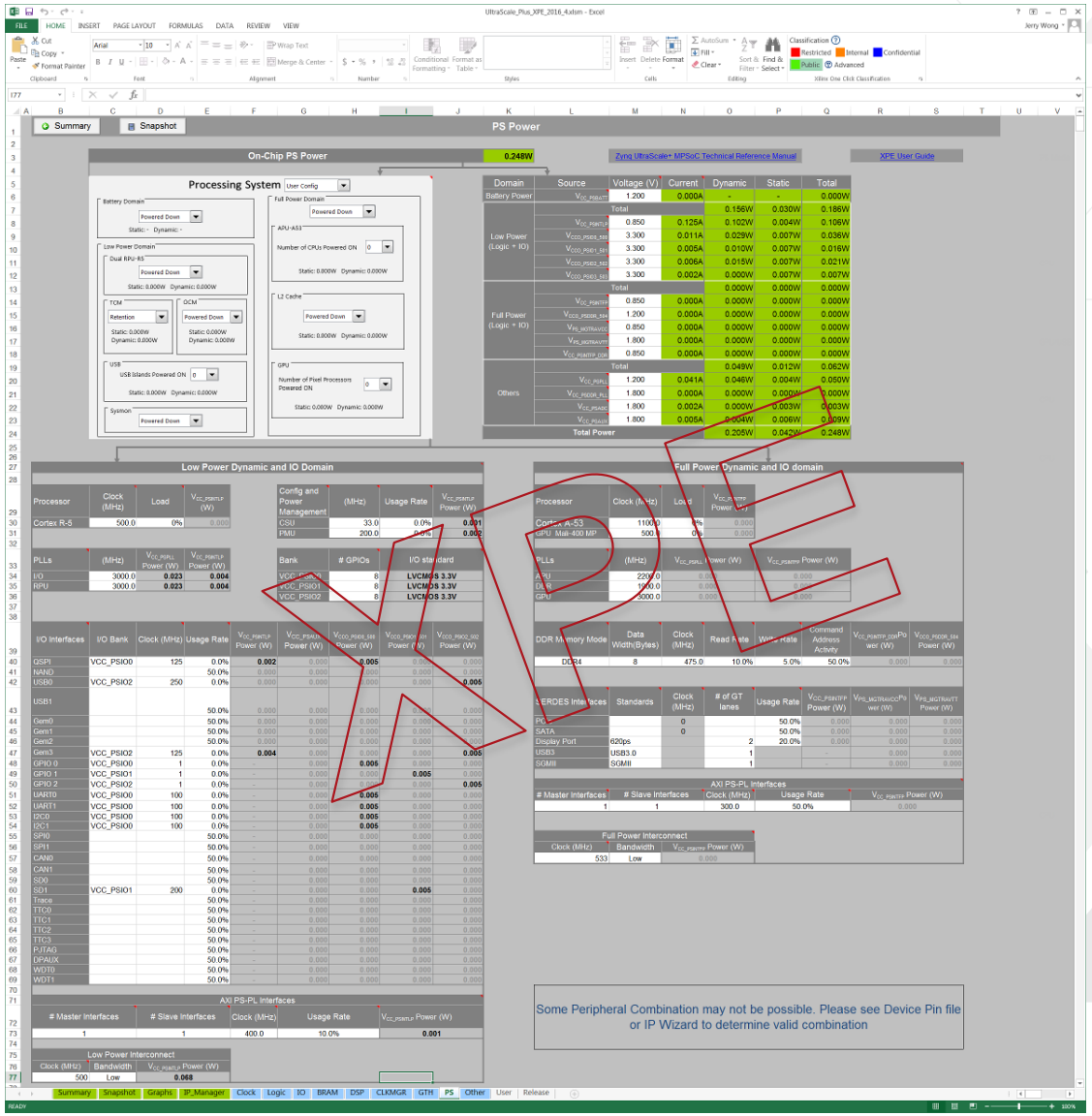
How to Estimate Power: Xilinx Power Estimator

Tool to estimate power …

- **Xilinx Power Estimator (XPE)**
  - Spreadsheet to model PS Power, etc.
  - Helps with power tradeoffs during the evaluation phase of your low power mode.
  - Fill out XPE, then discuss your design with a Xilinx FAE
  - Suggests Power Management Methodology

Download at

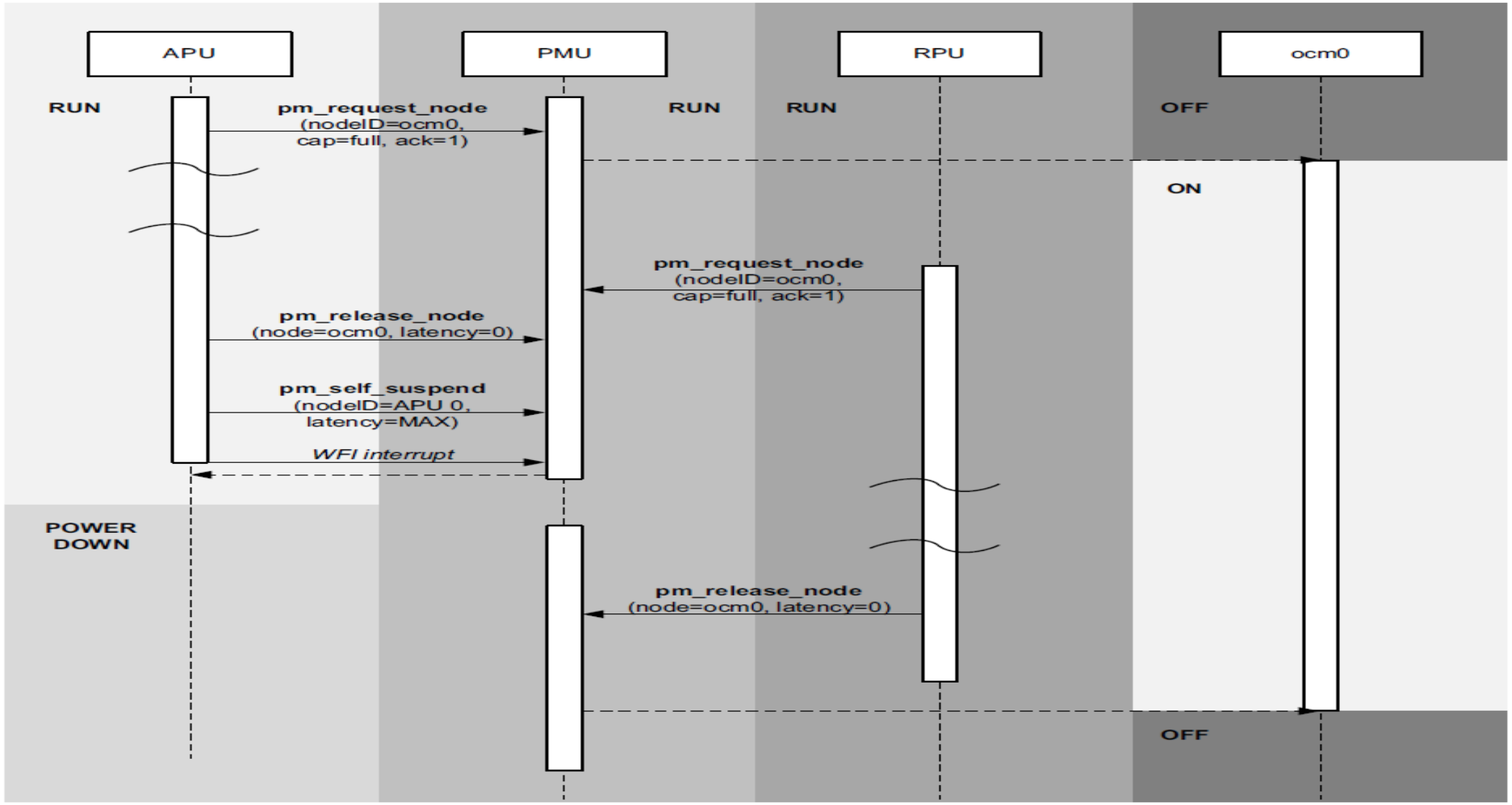
https://www.xilinx.com/products/technology/power/xpe.html



… Compare many low power mode power tradeoffs …

EEMI: How Do We Control a Power Island

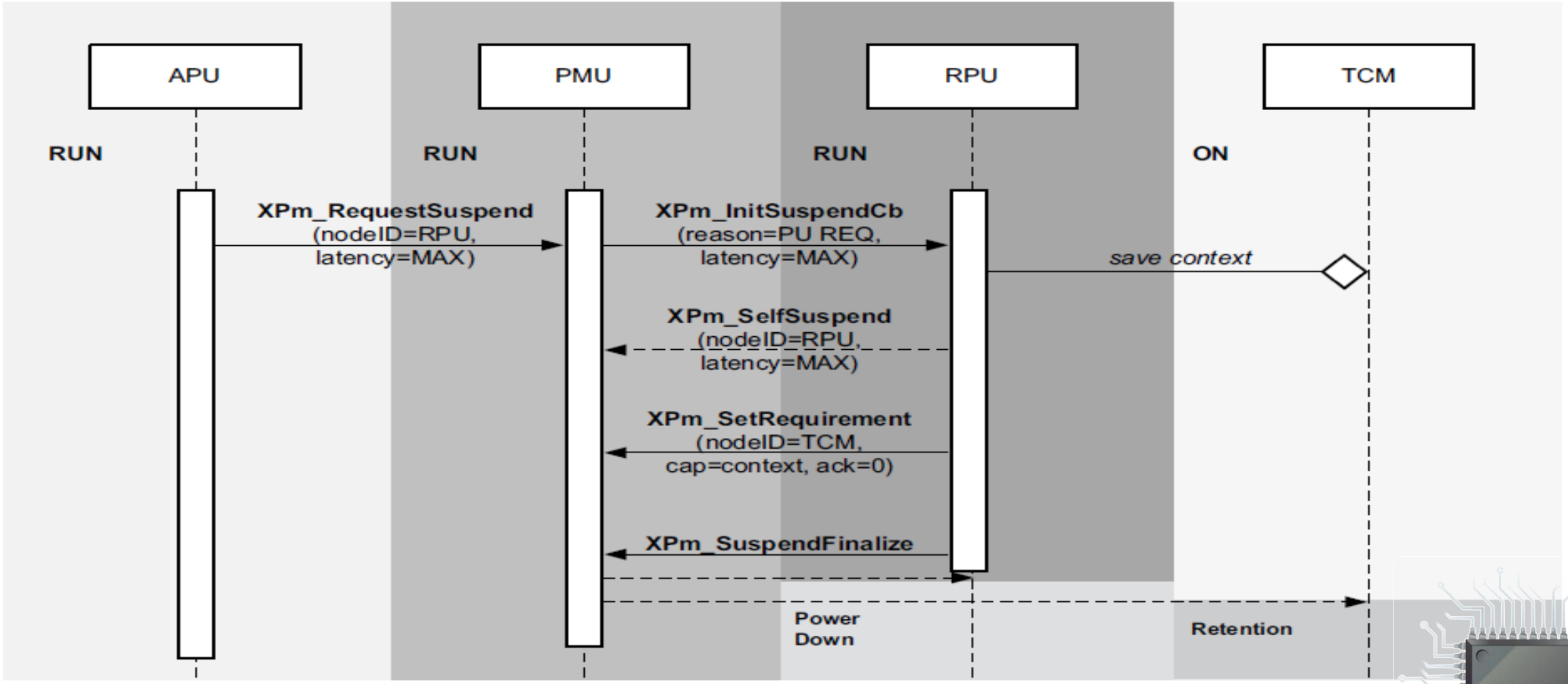
API Example #1
Power Island …



… PMU turns off any island when it is not in use …

EEMI: How Do We Suspend a Processor

API Example #2
Processor …



… PMU communicates / performs requests to suspend …

Additional Security Features

- Key Revocation – Public Key Authentication
- Encrypt/Decrypt Algorithm Enhancement
- Key Agility
- Permanent Decryptor Disable
- Tamper Logging
- DPA Resistance
- Obfuscated Key Loading
- Key Readback Protections
- User Access to Crypto Functions
- Other Items…