

Xilinx Adapt 2021: Data Center, 5G and Core Vertical Markets News



Aerospace & Defense

Industry's First 7nm Radiation Tolerant Adaptive SoC for Space 2.0 Applications



Space Industry Market Challenges & Requirements



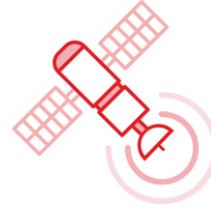
- ▶ Downlink bandwidth is limited
- ▶ Fast time-to-market
 - Platform concept for reuse on multiple missions



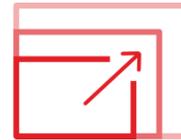
- ▶ Low latency and high bandwidth
 - Seamless and reliable connectivity for broadband communications



- ▶ Machine learning in orbit
 - Object Detection
 - Image Classification



- ▶ Need capability to process on board a satellite vs ground station
 - Reduce development time to launch (2-3 years vs. 5-6 years)
 - Process hundreds of Gbps data streams in real time



- ▶ Flexible system architecture
 - Change algorithms “on the fly”
- ▶ Reliable components for long mission life, extreme environments
- ▶ SWaP (Size, Weight and Power) Tradeoffs

Target Markets and Applications

for Space 2.0

Communications Constellations



- ▶ Broadband Internet
- ▶ High Speed Networks

Earth Observation Payloads



- ▶ Hyperspectral Cameras
- ▶ Synthetic Aperture Radar

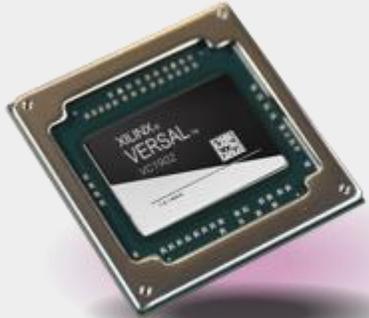
Navigation/Technology



- ▶ GPS
- ▶ Entry/Descent/Landing
- ▶ Instruments
- ▶ Avionics

Signal Processing, HW/SW Reconfigurable, Robust Package, Space Grade Tested, On Orbit Flexibility

Introducing XQR Versal for Space 2.0 Applications



- ▶ 7nm Adaptable SoC for Space Applications
 - AI Core and AI Edge family members with Scalar, Intelligent and Adaptable Engines (ARM CPUs, AI Engines & Prog. Logic)
 - Innovative silicon design for SEU mitigation
 - True on-orbit reconfiguration with unlimited programming cycles

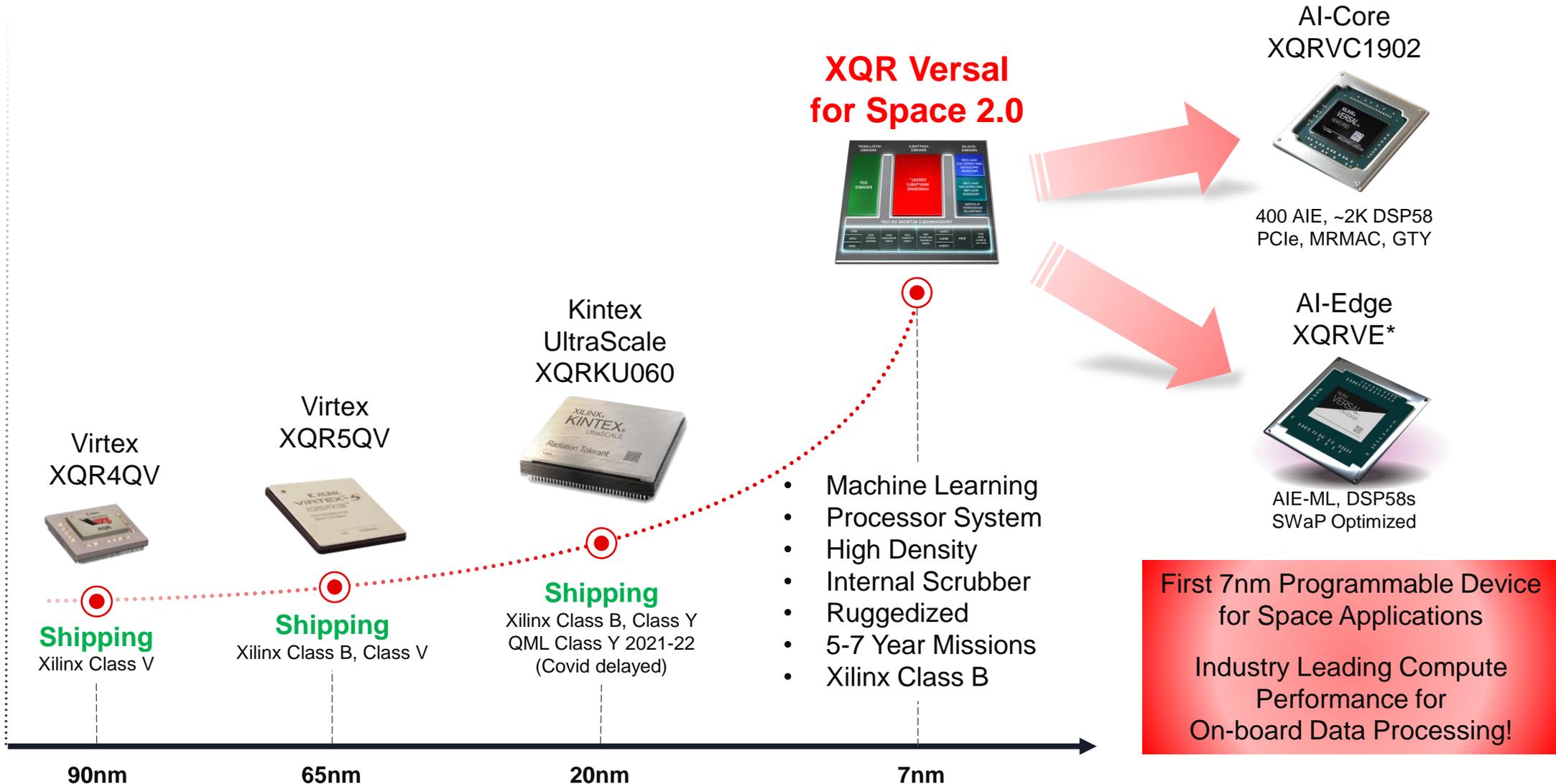


- ▶ Ruggedized Organic Packaging
 - AI Core 45mm x 45mm, AI Edge TBD
 - Lidless with stiffener ring for added thermal mitigation capabilities
 - Footprint compatible with commercial packages



- ▶ Production Space Test Flow
 - Xilinx B-Flow for Organic Substrates (QML Q Equivalent)
 - Designed for Space 2.0 Applications

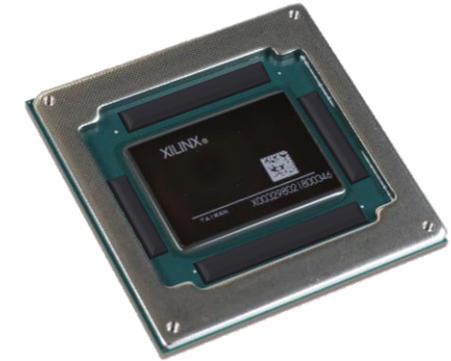
Xilinx Space Grade Solutions



* Under evaluation

XQR Versal for Space 2.0 Portfolio

	AI Core	AI Edge	
	XQRVC1902-1MSBVSRA2197	XQRVE*	
Intelligent Engines	AI Engines	400 (AIE)	12 - 34 (AIE-ML)
	AI Engine Data Memory (Mb)	100	6 – 17
	AI-ML Shared Memory (Mb)	-	48 – 68
	DSP Engines	1,968	176 – 464
Adaptable Engines	System Logic Cells (K)	1,968	80 – 329
	LUTs	899,840	36,608 - 150,272
	NoC Master/Slave Ports	28	2 – 5
	Distributed RAM (Mb)	27	1.1 - 4.6
Memory	Total Block RAM (Mb)	34	1.7 - 5.4
	UltraRAM (Mb)	130	13.2 - 43.6
	Accelerator RAM (Mb)	0	32
	Total SRAM Capacity (Mb)	164	48 - 85.6
	DDR Memory Controllers	4	1
	DDR Bus Width	256	64
Scalar Engines	Application Processing Unit	Dual-core Arm Cortex-A72, 48KB/32KB L1\$ w/ECC 1 MB L2\$ w/ECC	
	Real-time Processing Unit	Dual-core Arm Cortex-R5, 32KB/32KB L1\$ and 256KB TCM w/ECC	
	Memory	256KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2) USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial XCVRs	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug	
	GTY Transceivers (32.75Gb/s)	44	0 – 8
Integrated Protocol IP	CCIX & PCIe w/DMA (CPM)	1 x Gen4x16, CCIX	-
	PCI Express	4 x Gen4x8	0 - 1 x Gen4x8
	Multi-rate Ethernet MAC	4	0 – 1
Package	Ruggedized Organic BGA	VSRA2197, 45mm x 45mm, 0.92mm pitch	SSRA484/784, 19/23mm x 19/23mm, 0.8mm pitch
IO	648 XPIO, 44 HDIO, 78 MIO, 44 GTY 114-216 XPIO, 0-22 HDIO, 78 MIO, 0-8 GTY		



➤ Device Availability

- XQR AI Core - 3Q2022
- XQR AI Edge - 2Q2024

➤ [XQR Versal Product Tables](#)

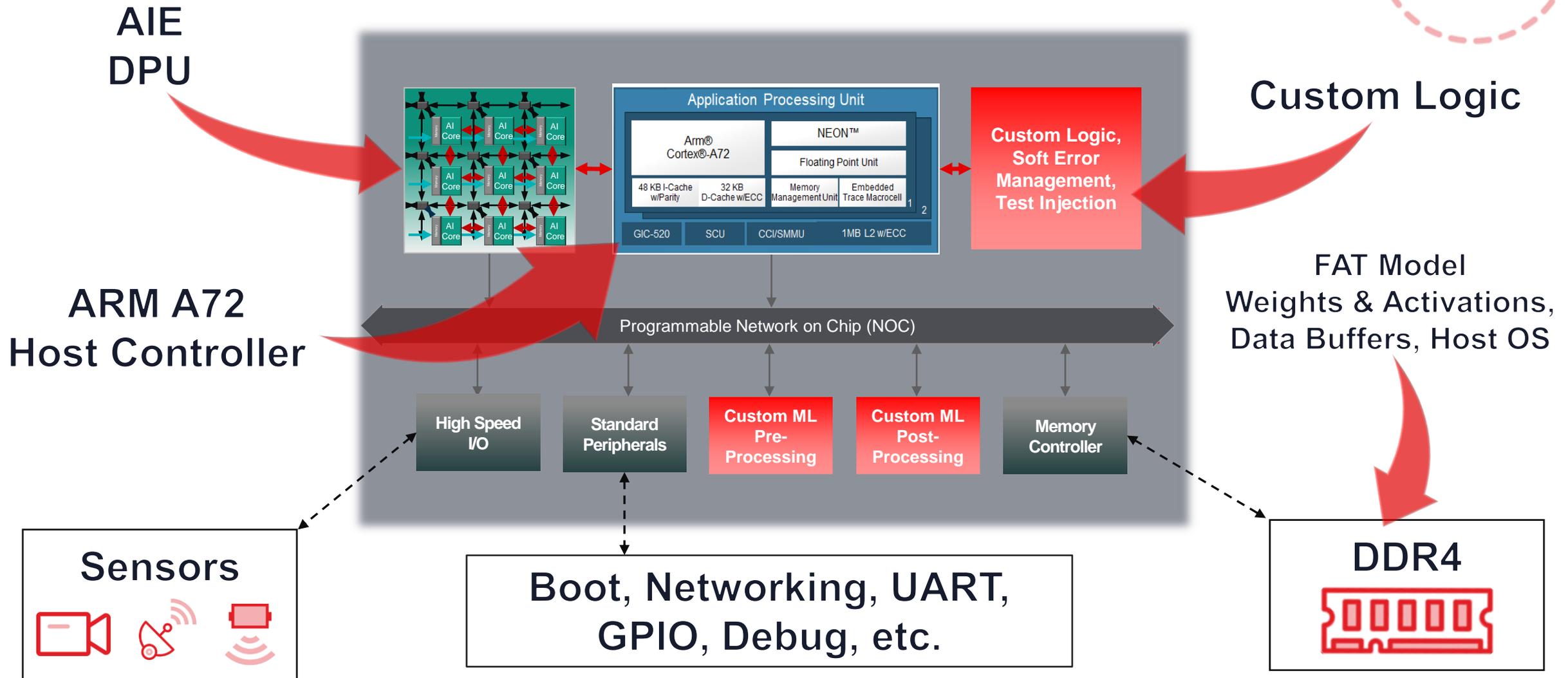
➤ Start designing today

- Use XC equivalent device
- Migrate to XQR

* Under evaluation

Payload Use Case

ML/AI DPU Convolutional Neural Network Platform



Key Takeaways

Industry's first 7nm Radiation Tolerant Adaptive SoC targeted for broadband and constellation satellite applications

True unlimited on-orbit reconfiguration to enable “upgrade-on-the-fly” capability

Complete solution to “process and analyze” for real-time on-board processing needs including machine learning and artificial intelligence



Aerospace & Defense

Defense-Grade XQ Ruggedized Versal Portfolio



Aerospace & Defense Industry System Challenges

High-availability in harsh environments



- ▶ Exposure to temperature extremes, moisture, dirt, shock vibration, radiation

Long product life cycle



- ▶ Supporting systems for 20+ years lifecycle requirements
- ▶ Obsolescence management
- ▶ Ensuring supply chain resilience against counterfeit devices deployment

Rigorous qualification requirements



- ▶ MIL-STD Reliability, hardware & embedded software qualifications
- ▶ Security certifications (agencies, military specific, EAL, etc.)
- ▶ Safety certifications (DO-254, DO-178, etc.)

Support Mission Critical Applications, Protection of Design and IP

Xilinx Defense-Grade (XQ) Versal – Key Features

An aerial view of a large aircraft carrier sailing on the open ocean. The ship's deck is visible, with several fighter jets parked in a row. The ship's superstructure, including radar masts and communication equipment, is prominent. The water is a deep blue, and the sky is clear.

Eutectic Sn / Pb (Tin / Lead) BGA

Ruggedized Packaging

Full Mitigation of Tin Whiskering (Sn / Pb ++)

Extended Temperature Range & Full Range Tested

Mil-Std 883 Group D Characterization

Anti-counterfeiting Protections

Mask Set Control

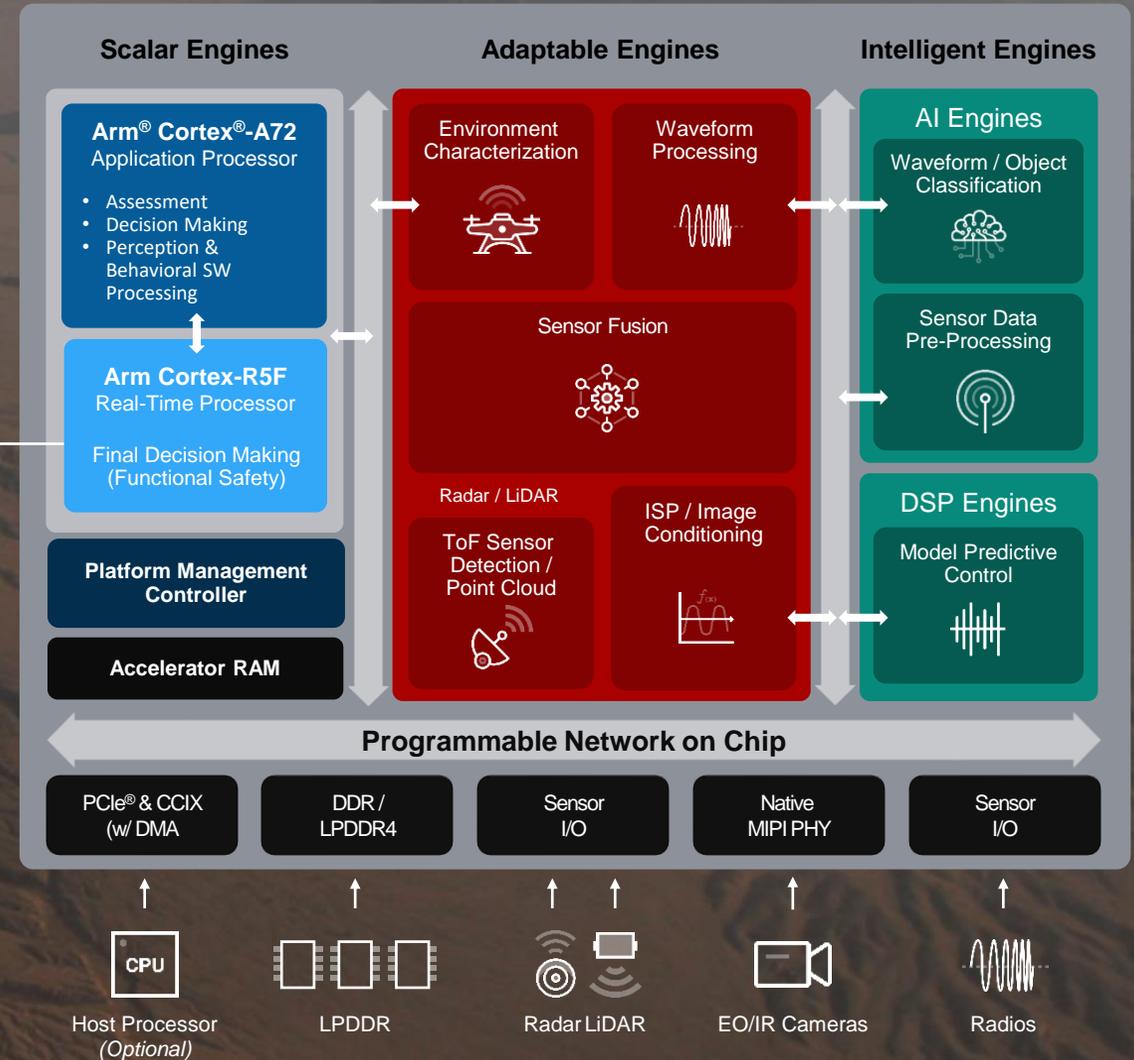
Long Term Availability

Defense-Grade XQ Versal AI Edge for Unmanned Systems



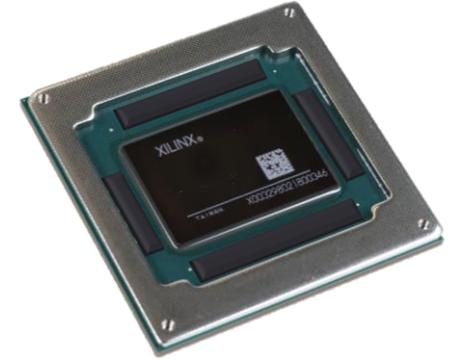
Multi-Mission and Situationally Aware Unmanned Systems with Low SWaP

- ▶ Adaptable Engines for sensor fusion and pre-processing
- ▶ Intelligent Engines for low power, low latency AI and signal conditioning
- ▶ Scalar Engines for command and control
- ▶ Ruggedized Defense-grade parts (XQ)



XQ Versal Ruggedized Portfolio

Product	XQ Versal Edge		XQ Versal AI Core			XQ Versal Prime				XQ Versal Premium			
Device	VE2102	VE2302	VC1352	VC1702	VC1902	VM1102	VM1402	VM1502	VM1802	VP1202	VP1402	VP1502	VP1702
XQ Package Footprint	SBRA484, SSRA784	SSRA784	NBRA1024, NSRE1369	NSRG1369, VSRA1596, VSRA2197	VIRA1596, VSRD1760, VSRA2197	SSRA784	NSRB1369, VSRD1760, VSRC1596	VSRA2197	VSRD1760, VSRA2197	VSRC2197, VSRA2785	VSRF1760, VSRA2785	VSRA2785, VSRA3340	VSRA3340
Speed-Temperature	1LSI, -1MSI, -2MSI, -1MSM											-1LSI, -1MSI, -2MSI	



▶ **1st Devices Availability: 1Q2022**

- XQ AI Core device (XQVC1902)
- XQ Prime device (XQVM1802)

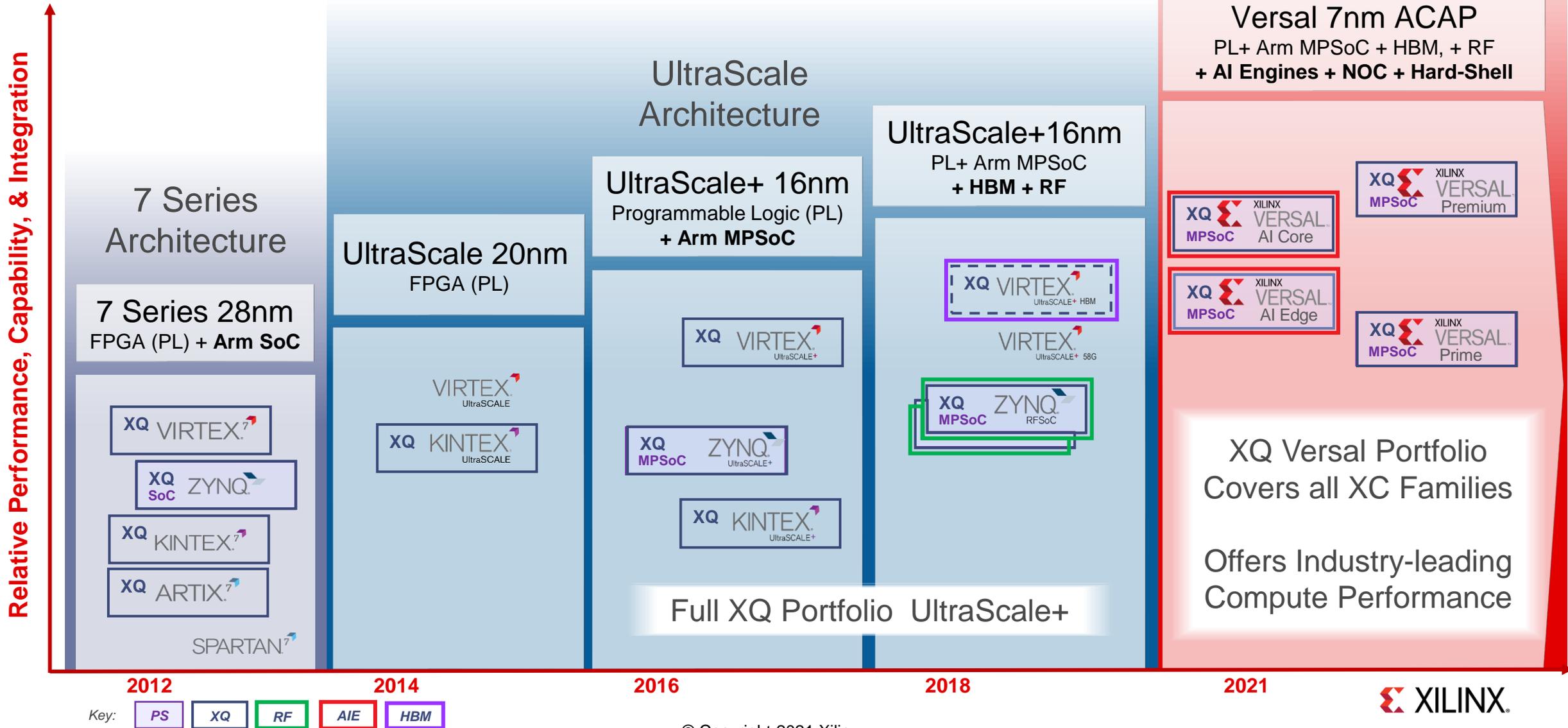
▶ **XQ Versal Product Tables**

▶ **Start designs today**

- Use XC equivalent device-footprint
- Migrate to XQ from compatible XC

- ▶ **Select speed-temp-voltage options available in XQ**
- ▶ **M-temp (-55C to +125C) available in most devices **-1MSM** grade**

Extending Defense-Grade with XQ Versal



Key Takeaways

Extending 30+ years of Xilinx heritage & commitment to aerospace & defense industry, extending XQ families with the addition of XQ Versal Portfolio

Industry's most advanced defense-grade product: XQ Versal ACAP built on 7nm technology, offered in ruggedized package, with extended qualifications

Enabling industry-leading AI/ML and compute capability with XQ Versal ACAP in the harshest aerospace & defense application environments

Available military temp range (-55°C to +125°C), for full XQ Versal ACAP, including advanced processor system, programmable logic, and adaptable compute engines

Automotive

New Automotive LiDAR Research From Xilinx and Strategy Analytics



New Global LiDAR Forecast



Copyright© Strategy Analytics 2021

Xilinx Value Proposition in LiDAR



Flexibility

- ▶ Hardware re-programmability for adaptable algorithm implementations over time, over-the-air updates (OTA HW), and fast time-to-market.
- ▶ Heterogeneous compute domains (the right engine for the right job) for raw data processing, point cloud generation, and CNN.

Parallel Processing

- ▶ Xilinx programmable logic (PL) offers parallel processing of multiple data paths simultaneously and independently. This capability enables true hardware (HW)-based processing pipelines for multiple lidar receive (RX) channels. Parallel HW processing reduces the need for clock speed, thus, reducing power.

Customizable Deep Learning Processor Unit (DPU)

- ▶ Configurable computation engine dedicated to point cloud data processing – specifically object detection and segmentation.
- ▶ Adaptable for both 2D & 3D point cloud data processing.
- ▶ Helps our customers to future-proof their next-gen lidar systems with object detection & segmentation capabilities.

We are the Leading Silicon Supplier in the LiDAR Market

Top Customer Collaborations



Xilinx field programmable gate arrays (FPGA) and adaptive system-on-chips (SoC) are used in Velodyne's LiDAR sensors for image processing. Xilinx technology allows for flexible programming while providing scalable processing performance for complex sensory data. Our multi-processor system-on-a-chip (MPSoC) devices, which we're providing to Velodyne, combine CPU processing power with the flexibility of field-programmability, which means the devices can be reprogrammed as the design evolves. One device can be used for multiple "flavors" of Velodyne lidar, including future generations of product.



Image credit: Xilinx



Fixed-function silicon cannot match the flexibility and adaptability of the Xilinx programmable logic, advanced DSP, and connectivity options. The adaptability of our silicon allows us to keep pace with Ouster's evolving requirements without forcing them to redesign their entire architecture. We've also got a long-standing heritage in functional safety, which means customers like Ouster have the assurance that our automotive-qualified products provide them with the reliability they, and their customers, require.



Video credit: Xilinx

Xilinx Value Proposition:

Low latency point cloud data transmission

High-speed connectivity and data transmission via GTH transceivers

Advanced DSP capabilities produce rich point cloud images

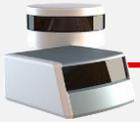


Xilinx Automotive ADAS & AD Focus Areas

Full Display Mirror



LiDAR



Forward Camera



In-Cabin Monitoring Camera



Domain Controller

- > Gateway
- > Compute Acceleration
- > Data Aggregation, Pre-processing, and Distribution (DAPD)



Surround View Camera

> Rear



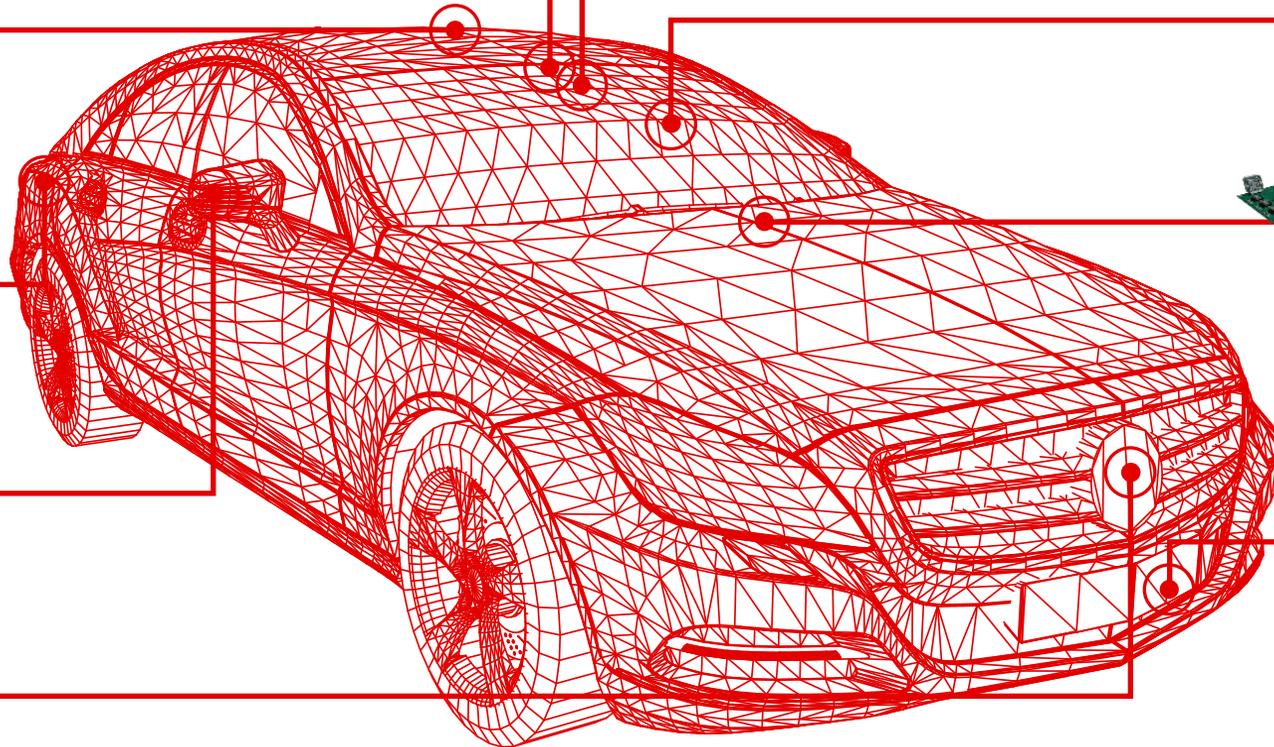
> Side



> Front



RADAR



Note: Not representing actual vehicle architecture;
Sensors are for illustrative purposes

Data Center

Microsoft Azure Synapse Analytics Powered by Alveo Acceleration



Azure Synapse Accelerates Big Data Analytics with Alveo

- ▶ 90% of Synapse Apache Spark workloads are CSV/JSON/Parquet. Xilinx Alveo U250 accelerators address one of the most common problems associated with Spark workloads: CSV/JSON parsing performance
- ▶ Xilinx accelerators deliver **40x performance improvements for Synapse Apache Spark** instances
- ▶ Azure Synapse now leverages Azure NP-VM FPGA-a-a-Service, powered by Xilinx Alveo, for Spark query acceleration
- ▶ Result: >40x increase in CSV/JSON Spark performance
 - CPU CSV parser per core(Ev3 series): 15MB/sec
 - FPGA CSV parser raw performance: 6.1 - 7.7 GB/sec



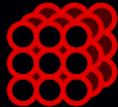
Data Center

Xilinx Video Transcoding SDK



Xilinx Video Transcoding SDK

U30: Industry-best performance



2x Density



50% lower power



50% lower cost

Video SDK: Ready To Stream



Full SDK: Tutorials, docs, examples, broad media framework support



Production hardened and ready to deploy



Faster time to market



Industrial and Healthcare

Kria robotics stack

Bringing ROS 2 down to silicon

Pam Yocca Pam Yocca
Harini Katakam Susan Cheng
Stefano Stabellini Pam Yocca
Victor Mayoral-Vilches Susan Cheng
Quenton Hall Terry O'Neal
Pranavi Somisetty
Susan Cheng Susan Cheng
Stefano Stabellini Quenton Hall
Todd Kirkland Pranavi Somisetty Vamshi Kirshna
Subh Bhattacharya
Girish Malpeddi
Todd Kirkland
Wesley Skeffington
Randy Hartgrove
Todd Kirkland
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Harini Katakam
Terry O'Neal
Evan Leal Chetan Khona

Chetan Khona
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Evan Leal

Quenton Hall Pam Yocca Harini Katakam
Vamshi Kirshna Susan Cheng Stefano Stabellini
Kiran Vishal Thangawir Phaaaskar
Sweatha Rao Sweatha Rao
Chetan Khona Evan Leal
Jasvinder Khurana
Brian Woods Evan Leal
Randy Hartgrove
Wesley Skeffington
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Chetan Khona Sweatha Rao
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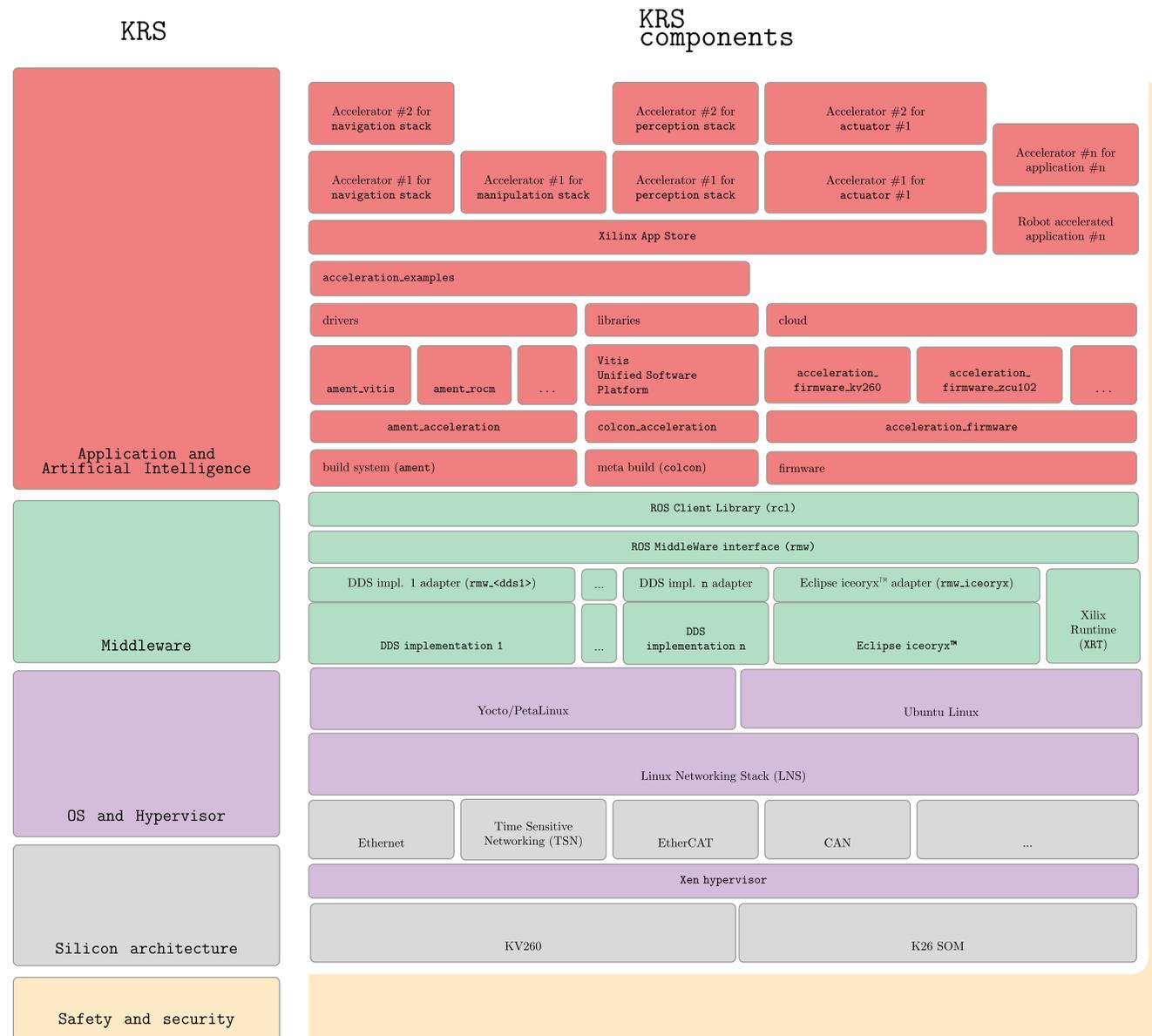
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The Kria robotics stack (KRS) is **a complete integrated set of robot components and utilities, built around ROS 2 and set to accelerate the development, certification and maintenance of industrial-grade robotic solutions**

Empowering Hardware Acceleration and next-gen “robot chips”



Xilinx is Adopting ROS 2 and Gazebo as its Robotics SDK



KRS, a ROS 2 superset for industrial applications

Build industrial-grade Accelerated Applications for Robots with ROS 2



ROS 2-centric experience

- ROS 2 and Gazebo focused Software Development Kit (SDK)
- Roboticians can leverage Xilinx tools easily through KRS to produce robot accelerated applications



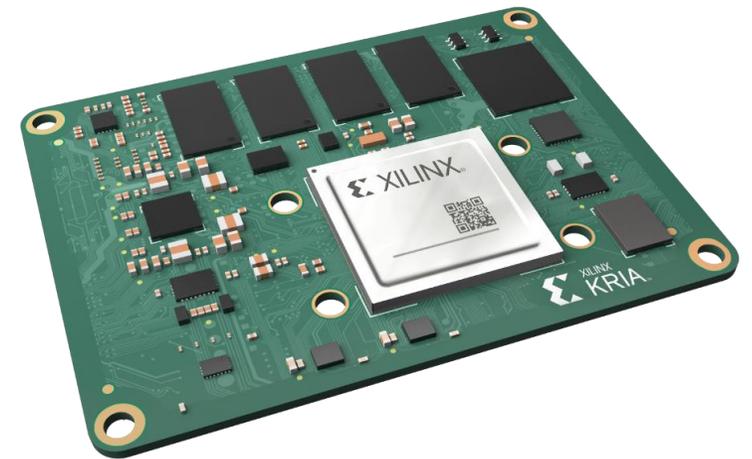
Real-time ROS 2

- More deterministic ROS 2 behaviors
- Through KRS, roboticians can leverage adaptive computing to create custom compute architectures and obtain a more deterministic and reliable ROS 2 experience



Accelerated Apps for Robots

- A marketplace for ROS 2 packages
- Download accelerated and customized ROS 2 underlayers for improved real-time, throughput, low latency or cybersecurity



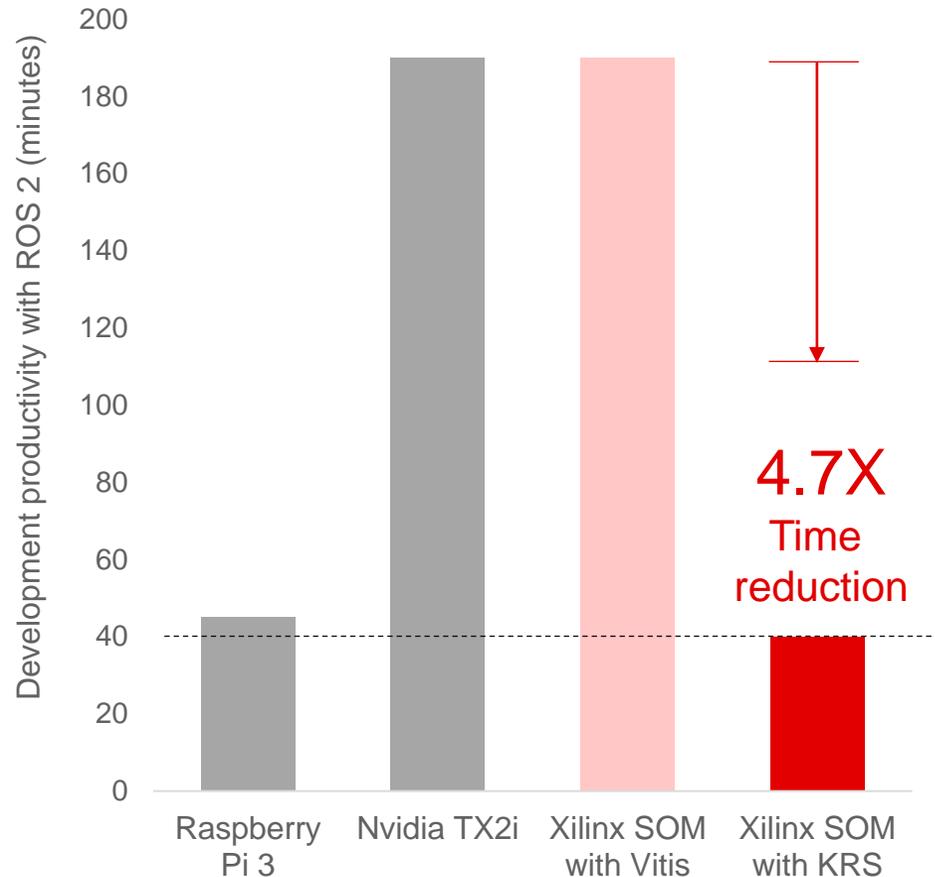
Kria K26 System-On-Module (SOM)

KRS Extends the Kria SOM Portfolio to Roboticians

Performance & ROS 2 Dev. Productivity Advantages

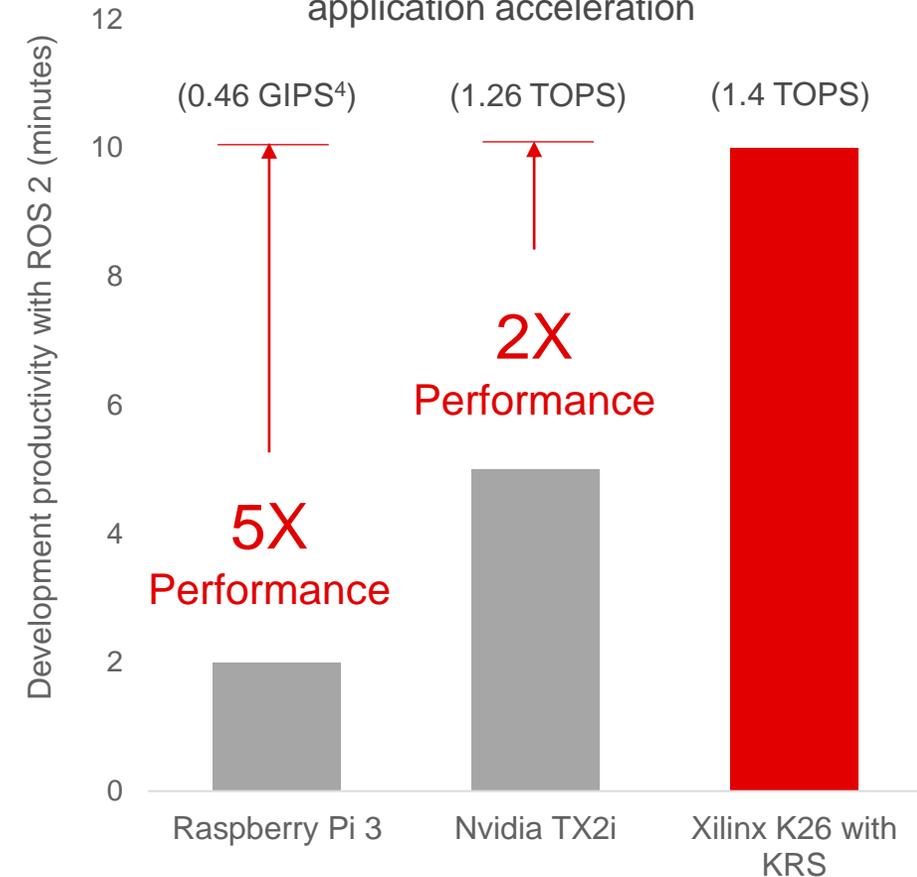
4.7X ROS 2 dev. productivity

when compared to NVIDIA CUDA² or Xilinx Vitis flows¹



2X Performance¹

A boost in performance when compared to Raspberry Pi and Nvidia TX2i³ through whole application acceleration



1: Evaluated using doublevadd_publisher and accelerated_doublevadd_publisher – https://github.com/ros-acceleration/acceleration_examples

2: Accounts for setting up the toolchain with ROS 2, cross-compilation of host code or creation and build of the accelerator among other necessary steps.

3: ROS 2 Node running in the scalar CPUs.

4: <https://magpi.raspberrypi.org/articles/raspberry-pi-4-specs-benchmarks>

Xilinx is Leading ROS 2 Acceleration with the *Hardware Acceleration Working Group (HAWG)*

Announced in April, received strong interest, watch full meeting [here](#) ([discussion](#)).

Xilinx contributed and [open-sourced](#) a reference architecture for acceleration

Check out the [acceleration ROS Enhancement Proposal \(REP\)](#) to learn more

Join us in the next HAWG meeting, happening [September 29th](#).



KV260 is the official reference hardware platform of the HAWG

Collaborating with Industry to Make ROS 2 Faster and Real-Time

Industrial and Healthcare

Vitis Libraries for Medical Ultrasound



Xilinx a Leader Across Medical Modalities

Market Leader



Surgical Robots

Market Leader



Endoscopy



CT, MRI, PET Imaging



Radio Therapy

Market Leader



Ultrasound is #1 Application

Ultrasound

Fast Growing



3D Dental Imaging

Fast Growing



Patient Monitors

Fast Growing



Smart Hospital Beds

Fast Growing



Defibrillators

Supporting Demand in Markets Disrupted by COVID-19

Existing Applications

Hospital Equipment + Test Diagnostic



Patient Monitors



Ultrasound



Ventilators



CT Scanners



Lab / Chemistry



Endoscopy

Helping Accelerate New Technology Trends

HcIoT - New and Emerging



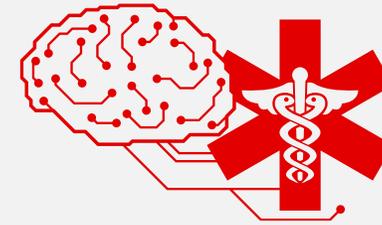
**Telemedicine /
TeleHealth**



**Point
of Care**



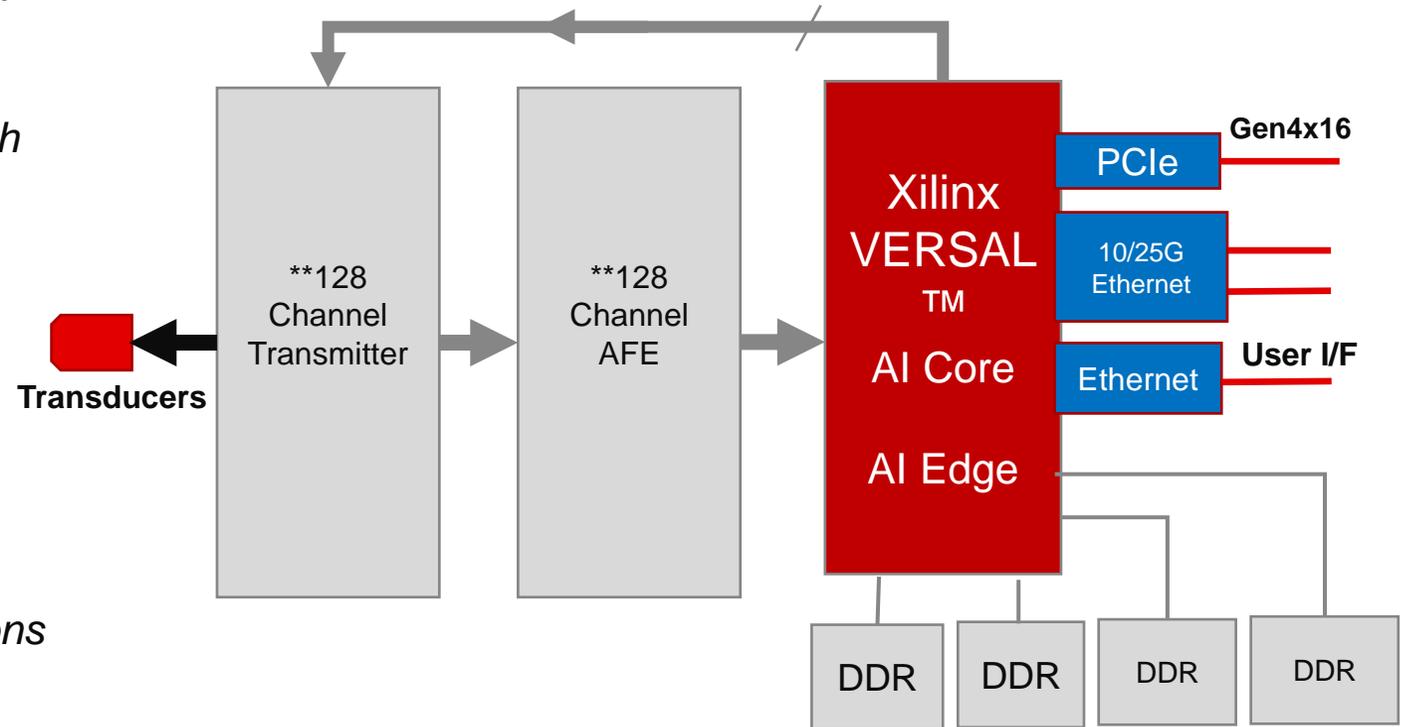
**Remote
Patient Monitoring**



**AI Applications
in Healthcare**

Xilinx Versal SoCs for Ultrafast Imaging in Ultrasound

- ▶ **'Ultrafast' Imaging** techniques in medical Ultrasound scanners can produce the
 - ▶ *Best image quality, accuracy, coverage depth*
- ▶ A single **Xilinx Versal™ SoC** can enable 'UltraFast' Imaging in an Ultra-Premium Medical Ultrasound Scanner
- ▶ Xilinx expanding **Vitis** unified software platform to include libraries for 'UltraFast' imaging
 - *Fast development times and multiple iterations of algorithms for developers*
- ▶ Libraries optimized and targeted for the innovative **Versal AI engines**



Integrated UltraFast Medical Ultrasound Libraries: *Productivity & Performance*

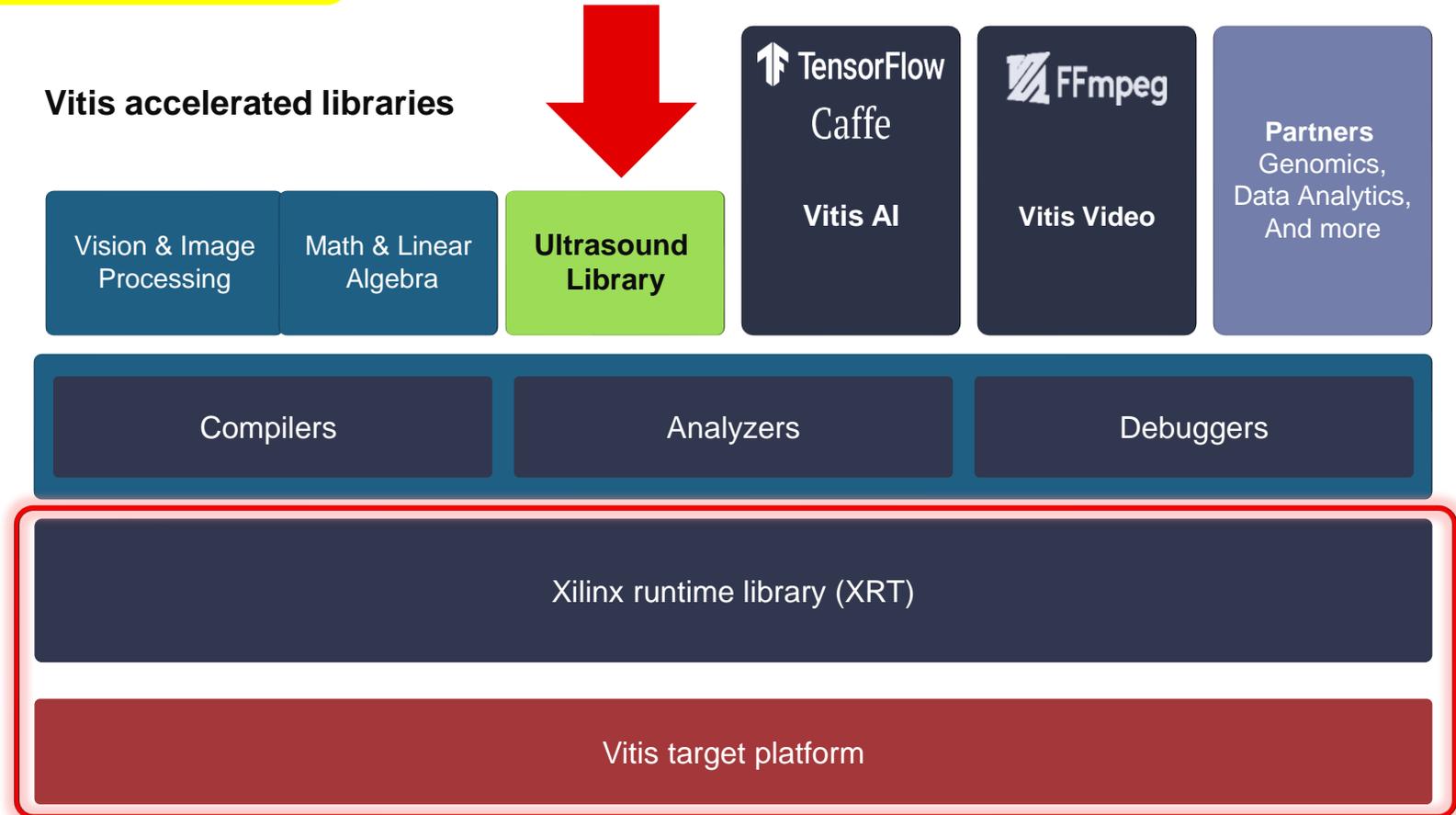
****Early Access- End 2021****
**** Production – Mid 2022****

▶ Xilinx Vitis™ Unified Software Platform enables productivity

Vitis Ultrasound Libraries

- Domain-specific, open-source and performance-optimized libraries
- Enables rapid design for medical imaging scientists' Matlab code to Xilinx's Model-based design tool
- Develop using commonly-used high-level programming languages like C, C++, and Python

Vitis accelerated libraries



Performance: UltraFast Ultrasonic Imaging

All Data: 64 Active Elements, 1 Beamformer, 200 Lines

* FPS – Frames per second

**Benchmarks shown above against RTX2070 running CUDA

Small Parts Ultrasound Imaging

	Versal VCK190	GPU-RTX 2070	PC i7
Linear Interpolation	1101 fps	~40 fps	~1 fps
Matched Filter or Catmull-Rohm Spline Interpolation	365 fps	~4 fps	~0.006 fps
Linear Interpolation (int16)	4406 fps	~100 fps	~1 fps
Matched Filter Interpolation (int16)	1461 fps	~15 fps	~0.006 fps

Abdominal Imaging

	Versal VCK190	GPU-RTX 2070	PC i7
Linear Interpolation	482 fps	~20 fps	~0.25 fps
Matched Filter Catmull-Rohm Spline Interpolation	160 fps	~1 fps	~0.0015 fps
Linear Interpolation (int16)	1920 fps	~90 fps	~0.25 fps
Matched Filter Interpolation (int16)	640 fps	~10 fps	~0.0015 fps

AI Engines on Versal Produced Benchmarks ~40 Times Faster Than CUDA Optimized GPUs

Wired & Wireless Communications

Xilinx Shipping Zynq RFSoc DFE in Volume

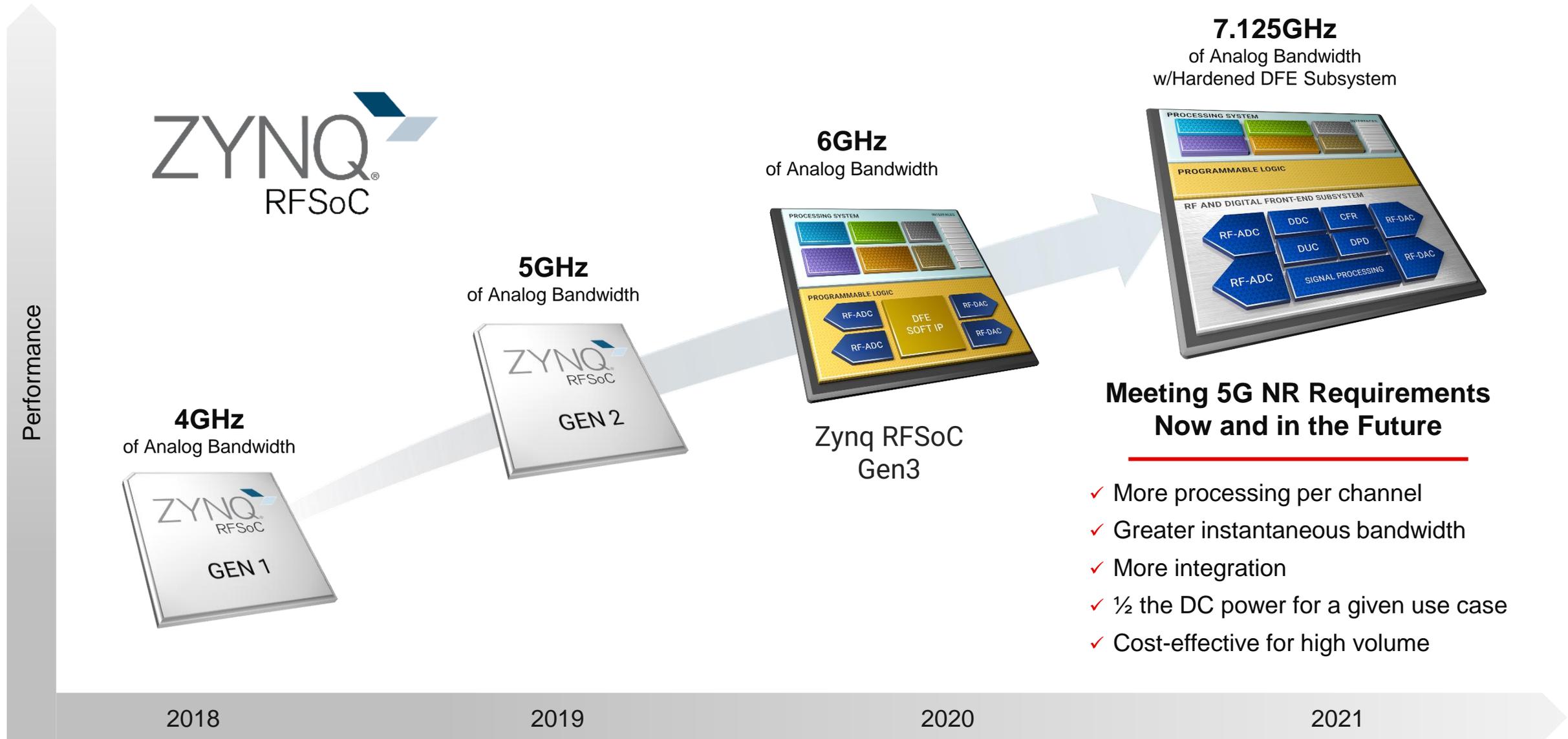


ZYNQ[®]
RFSoc DFE

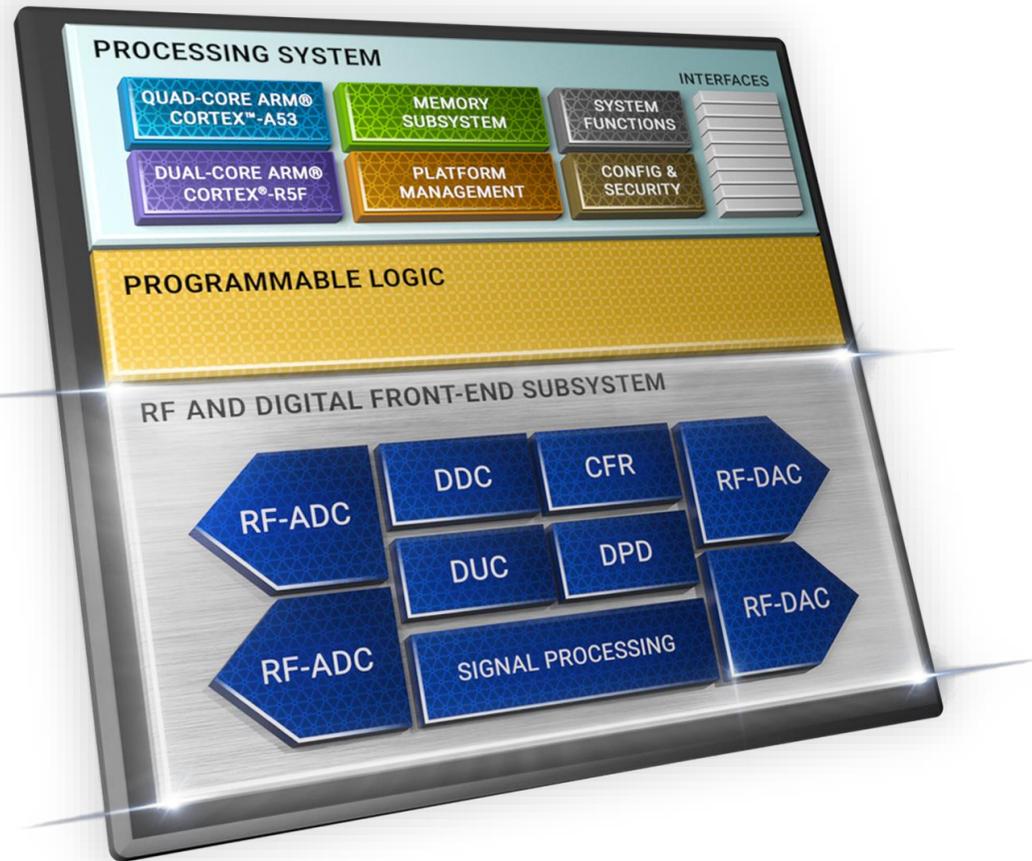
Shipping



Portfolio for Current and Future Market Needs



Zynq RFSoc DFE: Adaptive SoC with a Hardened Radio Subsystem



Adaptive SoC

Arm Processing System • UltraScale+ Programmable Logic • 32G SerDes

Hardened Radio Subsystem Single-Chip 8T8R FDD/TDD



Direct-RF DACs/ADCs
7.125GHz Direct-RF Bandwidth



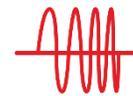
Digital Pre-Distortion (DPD)
Supports traditional & ultrawide band (400MHz) GaN PAs



Crest Factor Reduction (CFR)
Up to 400MHz of Instantaneous Bandwidth



DUC / DDC¹
Multi-carrier, multiband support



Signal Processing IP
Re-Sampling, Equalizer

1: Digital Up-Conversion, Digital Down Conversion



Thank You

