PRODUCT BRIEF

# Versal Premium Series with AI Engines

## Built for Extreme Signal Processing

## OVERVIEW

Versal® Premium adaptive compute acceleration platform (ACAP) delivers industry-leading adaptive signal processing capacity by integrating AI Engines.

While providing 4X signal processing capacity[1] compared to previous generation FPGAs, the Versal Premium series also includes highly scalable serial bandwidth, power-optimized networking IP cores, and massive on-chip memory to eliminate data movement bottlenecks.

As a heterogeneous compute platform, Versal Premium ACAPs enable a significantly reduced size, weight, and power (SWaP) advantage for a wide range of signal processing intensive applications in aerospace & defense and test & measurement markets.

## HIGHLIGHTS

**Architectural Innovation for Industry-Leading Adaptive Compute Performance**

- 4X signal processing capacity vs. previous generation FPGAs
- Customizable memory hierarchies and locality to maximize bandwidth and minimize latency per workload
- Re-architected programmable logic at 2X density vs. previous gen FPGAs

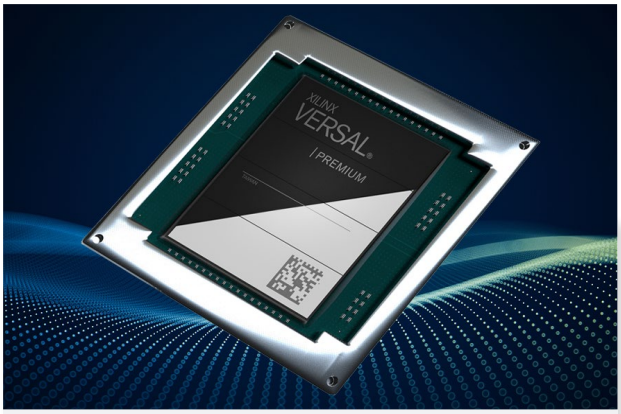
**Eliminating I/O Bottlenecks to Support Higher Density Antennas and Devices Under Test (DUTs)**

- Offers scalable serial bandwidth in a smaller area with power efficiency
- Provides secure, multi-terabit networking via integrated connectivity IP
- Enables high-density antenna and DUT designs with a breadth of protocols

**Reduced Size, Weight, and Power (SWaP) through Heterogeneous, Power-Optimized Integration**

- 4X more processing in a 67% smaller footprint at 43% lower power
- Eliminates additional processor ICs for smaller, lower power designs
- Simplifies system-level development and debug

1: Total equivalent DSP Engine capacity vs. Virtex® UltraScale+™ VU13P FPGA




## TARGET APPLICATIONS

### RADAR

- Digital Array Radar (DAR)
- Adaptive Beamforming
- Space Time Adaptive Processing (STAP)
- Synthetic Aperture Radar (SAR)

### SIGNALS INTELLIGENCE

- RF Machine Learning
- Digital RF Memory (DRFM)
- Direction Finding
- Digital Receiver / Exciter (DREX)

### WIRELESS TESTERS

- 5G Protocol Tester
- 5G Production Tester
- WLAN Device Tester
- Wireless Network Tester

### SEMICONDUCTOR AUTOMATED TEST EQUIPMENT (ATE)

- RF Transceiver
- Analog/Mixed signal
- Radar/Camera Sensor
- SoC

## FEATURES

| FEATURE HIGHLIGHTS | |
|---|---|
| AI Engines | > Tile-based architecture of 1.3GHz VLIW/SIMD vector processors<br>> Array of interconnected cores with terabytes-per-second of interface bandwidth to other engines for greater compute throughput<br>> Up to 10CTOPs with CINT16 and FP32 compute bandwidth for signal processing<br>> C/C++programmable, compile in minutes, and library-base design for framework developers |
| DSP Engines | > Enhanced architecture for fixed point and high-precision floating point support with low latency<br>> Up to 99TOPs with INT8 and 23TFLOPs of FP32 compute bandwidth for signal processing<br>> Code portability from previous generation devices |
| Adaptable Engines | > Fine-grained parallel processing for higher compute capacity and less routing utilization<br>> Up to 123TB/s of programmable memory hierarchy for optimal compute efficiency<br>> Dynamic Function eXchange (DFX) to swap functionality in milliseconds, reducing device cost and system power and enabling adaptability as algorithms evolve |
| Scalar Engines | > Dual-core Arm® Cortex®-A72 application processing unit for Linux-class operating systems<br>> Dual-core Arm Cortex-R5F real-time processing unit with low latency and determinism<br>> Platform management for quick boot, power and thermal management, and safety and security enclave |
| Programmable Network on Chip | > Terabits of dedicated bandwidth for guaranteed QoS with flexible bit-widths and no logic routing consumption<br>> Software programmable framework with memory-mapped access to all resources<br>> Easy IP and kernel placement with hardened connectivity to DDR, PCIe, and peripherals |
| NRZ and PAM4 Transceivers | > Up to 9Tb/s of serial bandwidth to support more antennas or testers without I/O bottlenecks<br>> 32G NRZ transceivers for mainstream power-optimized 100G interfaces<br>> 58G/112 PAM4 transceivers for the latest protocols and maximized bandwidth density |
| Integrated 100G Multirate and 600G Ethernet Cores | > Up to 5Tb/s of flexible Ethernet connectivity enabled by hardened 100G/600G cores<br>> Multirate: Bidirectional 400/200/100/50/40/25/10G with FEC<br>> Multi-standard: FlexE, Flex-O, eCPRI, FCoE, OTN |
| 400G High-Speed Cryptography Engines | > Up to 1.6Tb/s of line rate encryption throughput for secure networking<br>> Bulk encryption: AES-GCM-256/128, MACsec, IPsec<br>> Channelized rates from 40x10G to 1x400G per engine |
| PCIe® Gen5 with DMA and CCIX, CXL | > Symmetric/asymmetric access to memory with cache coherent interconnect for accelerators<br>> Efficient communication to backend processing systems or test analyzers |
| Integrated 600G Interlaken Cores with FEC | > Scalable chip-to-chip interconnect from 10Gb/s to 600Gb/s<br>> Integrated RS-FEC for power-optimized error correction |

## TAKE THE NEXT STEP

For more information about the Versal Premium series, visit https://www.xilinx.com/versal-premium.

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