

## Introduction

Cobham Gaisler provides its LEON line of SPARC 32-bit processors for implementation in Xilinx FPGAs. The LEON3FT and LEON5FT processors are synthesisable VHDL models of 32-bit processors compliant with the SPARC V8 architecture. The models are highly configurable, and particularly suitable for system-on-a-chip (SOC) designs.

The processor models are available as part of the GRLIB IP Library. The GRLIB IP Library is an integrated set of reusable IP cores, designed for system-on-chip (SOC) development. The IP cores are centered around the common on-chip bus, and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique plug&play method is used to configure and connect the IP cores without the need to modify any global resources.

The library includes a wide range of peripherals, including cores for AMBA AHB/APB control, the LEON SPARC processors, 32-bit PC133 SDRAM controller with EDAC, DDR2/3 SDRAM controller with EDAC, 32-bit PCI bridge with DMA, 10/100/1000 Mbit Ethernet MAC, 8/16/32-bit PROM and SRAM controller, 16/32/64-bit DDR/DDR2 controllers, USB 2.0 host and device controllers, CAN controller, SpaceWire controllers, SpaceFibre controllers, TAP controller, SPI, I2C, UART with FIFO, modular timer unit, interrupt controller, and a 32-bit GPIO port.

## LEON3FT SPARC 32-bit Microprocessor

The LEON3FT is widely used within space applications and has flight heritage together with Xilinx FPGAs. The LEON3FT is also used in processor components such as the Cobham GR712RC, UT699 and UT700 microprocessor devices.

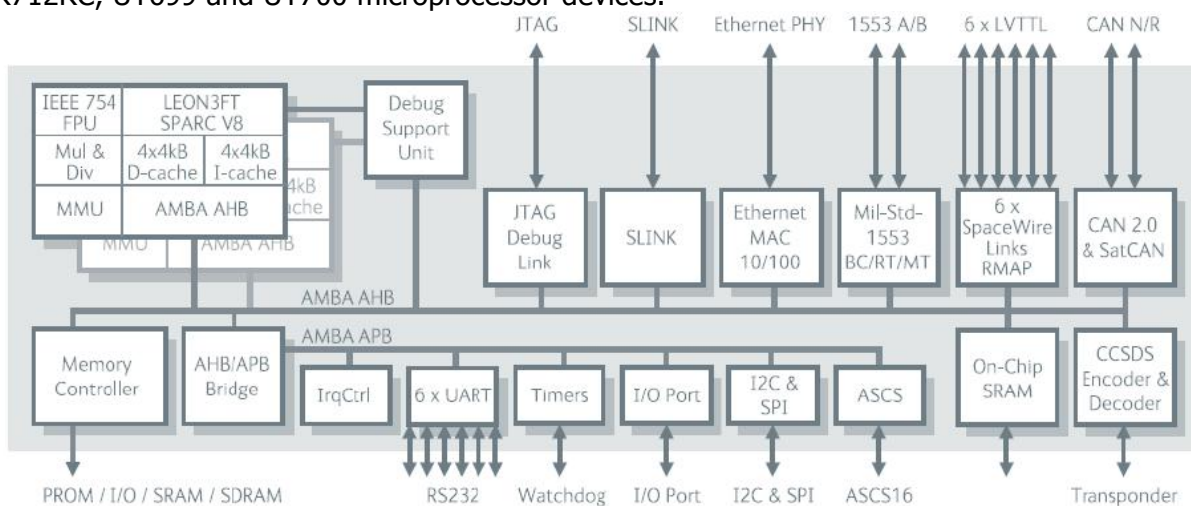


Figure 1 Example LEON3FT-based SoC design: GR712RC

## LEON5FT SPARC 32-bit Microprocessor

The processor pipeline design of the LEON5 is significantly enhanced compared to earlier LEON3 and LEON4 processors. The main new feature of the LEON5 pipeline is the dual-issue functionality, allowing up to two instructions per cycle to be executed in parallel in the processor. To support the increased issue rate of the pipeline, the LEON5 has advanced branch prediction capabilities. The cache controller of the LEON5 supports a store buffer FIFO with one cycle per store sustained throughput, wide AHB slave support to enable fast stores and fast cache refill, as well as several other enhancements.

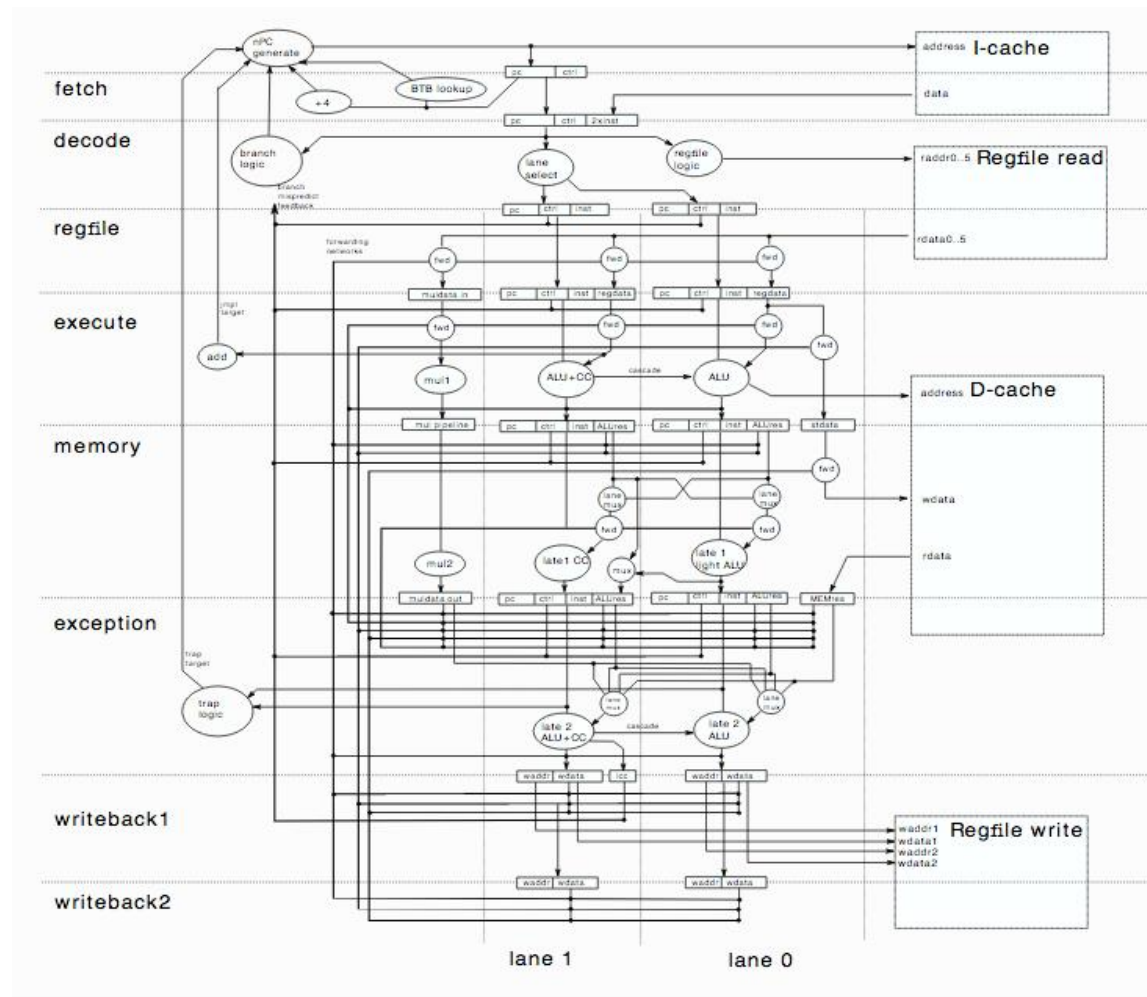


Figure 2 LEON5 integer unit datapath block diagram

The LEON5 is interfaced using the AMBA 2.0 AHB bus (subsystem with Level-2 cache and AXI4 backend is also available) and supports the IP core plug&play method provided in the Cobham Gaisler IP library (GRLIB). The processor can be efficiently implemented on FPGA and ASIC technologies and uses standard synchronous memory cells for caches and register file. The processor supports the MUL and DIV instructions, an IEEE-754 floating-point unit (FPU) and Memory Management Unit (MMU). The cache system consists of separate I/D multi-set Level-1 (L1) caches with up to 4 ways per cache, and an optional Level-2 (L2) cache for increased performance in data intensive applications.

## Software Ecosystem

The LEON line of processors are supported by a large range of software tools: compilers, kernels, simulators and debug monitors. Cobham Gaisler provides toolchains for Bare-C, RTEMS, Linux, ThreadX and VxWorks.

## LEON3FT Features

The LEON3FT processor core has the following features:

- SPARC V8 instruction set with V8e extensions
- Advanced 7-stage pipeline
- Hardware multiply, divide and MAC units
- High-performance, fully pipelined IEEE-754 FPU
- Separate instruction and data cache (Harvard architecture) with snooping
- Configurable caches: 1 - 4 ways, 1 - 256 kbytes/way. Random, LRR or LRU replacement
- Local instruction and data scratch pad RAM, 1 - 512 Kbytes
- SPARC Reference MMU (SRMMU) with configurable TLB
- AMBA-2.0 AHB bus interface
- Advanced on-chip debug support with instruction and data trace buffer
- Symmetric Multi-processor support (SMP)
- Robust and fully synchronous single-edge clock design
- Extensively configurable
- Large range of software tools: compilers, kernels, simulators and debug monitors
- Register file SEU error-correction of up to 4 errors per 32-bit word
- Cache memory error-correction of up to 4 errors per tag or 32-bit word
- Autonomous and software transparent error handling
- No timing or performance impact due to error detection and correction
- Performance: 1.8 CoreMark/MHz (gcc -4.1.2)

## LEON5FT Features

The LEON5FT processor core has the following features:

- SPARC V8 instruction set with V8e extensions and compare-and-swap
- Advanced 8-stage dual-issue pipeline
- Complex dynamic branch predictor and small branch target buffer
- Addition of Late ALU to decrease pipeline stalls
- 64-bit single-clock load/store operation
- 64-bit 4-port register file
- Hardware multiply and divide units
- Hardware floating-point support
  - Non-pipelined area efficient FPU (NanoFPU) or High-performance, fully pipelined IEEE-754 FPU including hardware support for denormalized numbers (GRFPU5)
- Separate instruction and data L1 cache (Harvard architecture) with snooping
- Optional L2 cache: 256-bit internal, 1-4 ways, 16 Kbyte - 8 Mbyte
- SPARC Reference MMU (SRMMU) with TLB

- AMBA-2.0 AHB bus interface, 32-, 64- or 128-bit wide
    - Subsystem including processor and Level-2 cache with AXI4 backend also available
  - Advanced on-chip debug support with instruction and data trace buffer, and performance counter
  - Symmetric Multi-processor support (SMP)
  - Robust and fully synchronous single-edge clock design
  - Cache memory error-correction of up to 4 errors per tag or 32-bit word
  - Autonomous and software transparent error handling
  - High performance:
    - Dhrystone\*: 3.23 DMIPS/MHz (-O3, inlining allowed)
    - Coremark\* : 4.52 CoreMark/MHz (-O3,-funroll-all-loops -finline-functions -finline-limit=1000)
- \* All the results generated using BCC 2.0.7 toolchain

## Availability

LEON3FT and LEON5FT are available as part of the GRLIB VHDL IP Core library.

## Additional information

LEON3FT Processor Model product page: [www.gaisler.com/LEON3FT](http://www.gaisler.com/LEON3FT)

LEON5 Processor Model product page: [www.gaisler.com/LEON5](http://www.gaisler.com/LEON5)

LEON on Xilinx Kintex Ultrascale: [www.gaisler.com/LEON-XCKU](http://www.gaisler.com/LEON-XCKU)