

### SpaceWire IP Cores

**SpaceWire** is a data-handling network for use on-board spacecraft which connects together instruments, mass memory, processors, downlink telemetry, and other on-board sub-systems. SpaceWire has some specific characteristics that help it support space applications.

**STAR-Dundee** provides essential SpaceWire interface and network components as VHDL IP blocks for use in FPGAs and ASICs including:

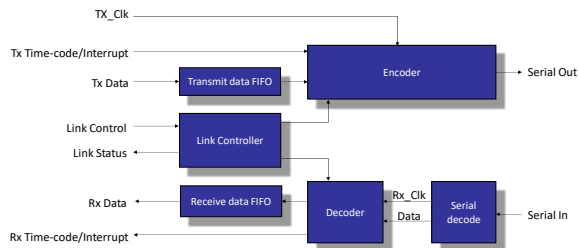
- SpaceWire Interface with DMA controller option
- SpaceWire Remote Memory Access Protocol (RMAP) Target / Initiator
- SpaceWire packet switch

### SpaceWire Interface

The STAR-Dundee SpaceWire Interface IP is a SpaceWire network interface block which is fully compliant with the ECSS-E-ST-50-12C SpaceWire standard. The IP can be instantiated with a packet streaming interface or with an integrated DMA controller.

### Functions

The SpaceWire Interface IP comprises a SpaceWire protocol encoder and decoder, an initialisation state machine controller, receive and transmit data FIFOs with flow control management counters, and time-code interfaces for time distribution. An overview of the IP functional blocks is shown below.



SpaceWire Interface IP function overview

### Features

The SpaceWire IP provides a highly flexible SpaceWire network component with the following features:

- Compliant with the SpaceWire standard, ECSS-E-ST-50-12C
- Configurable clock to support higher serial bit rates
- Host FIFO data interface. Write enable when not FULL, Read data when not empty. Time-code TICK IN and TICK OUT interface for time distribution. Status and error reporting interface
- Encoder Double Data Rate (DDR) option compatible with Xilinx IO buffers
- Includes link-level error recovery scheme from clause 11 of the SpaceWire standard

### DMA Controller

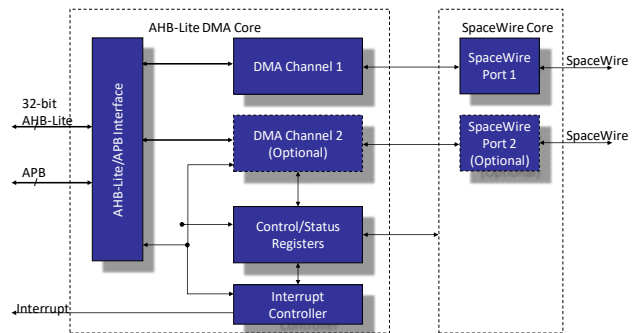
The SpaceWire Interface with DMA controller core is a generic synthesisable VHDL model which can be instantiated in an AHB-Lite compatible system to move packet data between a SpaceWire network and system memory.

The core provides either 1 or 2 bi-directional DMA channels which are programmable through an APB interface. The interface to system memory is an AHB-Lite master. AHB-Lite is an AMBA bus protocol specification used to connect an AHB master to multiple AHB slaves, typically connecting to ARM or AHB-Lite compatible processor systems such as the MicroBlaze and Zynq processors (using Xilinx AXI to AHB-Lite/APB conversion interface).

### Functions

The IP core comprises an AHB-Lite master interface, an APB slave interface, up to 2 bi-directional programmable DMA channels, a set of control and status registers, and an interrupt controller and vector for system interrupts.

An overview of the IP functional blocks is shown below:



DMA IP Controller function overview

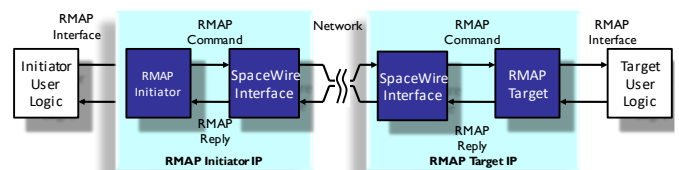
### Features

The IP provides a highly flexible interface between an AHB-Lite/APB compatible system and a SpaceWire network. The IP has the following features:

- Powerful DMA controller which simplifies data transfer between buffers in system memory and SpaceWire packets sent/received on the SpaceWire link
- Hardware CRC generation and checking
- AHB-Lite bus master and APB register interface

### SpaceWire RMAP Target / Initiator

The RMAP protocol provides a standard mechanism for reading from and writing to memory in a SpaceWire network. This simple but powerful capability has been designed into components like the SpW-10X router and into missions like BepiColombo and MMS. The RMAP standard document is an ECSS standard, ECSS-E-ST-50-52C. The separation of the functionality of the RMAP Initiator core and Target IP cores is shown below:

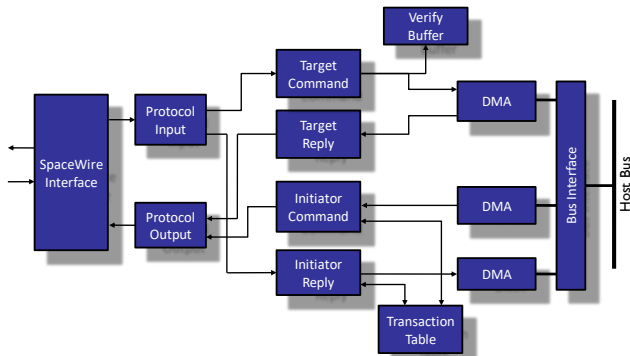


RMAP Initiator / Target separation of functionality

### Functions

The architecture of the RMAP IP core (both Target and Initiator instantiated) is shown below. The protocol input and output blocks

determine the destination of packets dependent on the packet header and support RMAP and non-RMAP packet transfers. The RMAP Target units decode RMAP command packets, read or write data from the host bus and return RMAP reply packets. The RMAP Initiator units accept commands into the transaction table, encode RMAP command packets, decode reply RMAP packets and output status information. Target and Initiator units interact with the user memory space by DMA.



RMAP Initiator / Target function overview

## Features

The IP has the following features:

- Compliant with the RMAP standard, ECSS-E-ST-50-52C
- Complete RMAP protocol handling core with memory interface, AHB-Lite bus master and APB register interface
- Configurable bus width, burst transfer depth, RMAP data byte order
- Configurable initiator transaction table size (outstanding transaction limit)
- Configurable internal FIFO sizes, verify buffers size
- Watchdog timer on bus transfers

## SpaceWire Router IP

The STAR-Dundee SpaceWire Router IP core implements the SpaceWire network layer routing functions defined in the ECSS-E-ST-50-12C SpaceWire standard.

### Functions

The SpaceWire Router IP core comprises a number of serial SpaceWire interfaces or optional parallel FIFO interfaces which are interconnected via a non-blocking wormhole packet switch. The packet switch implements address decoding for both path and logical addresses, output port arbitration, and packet routing.

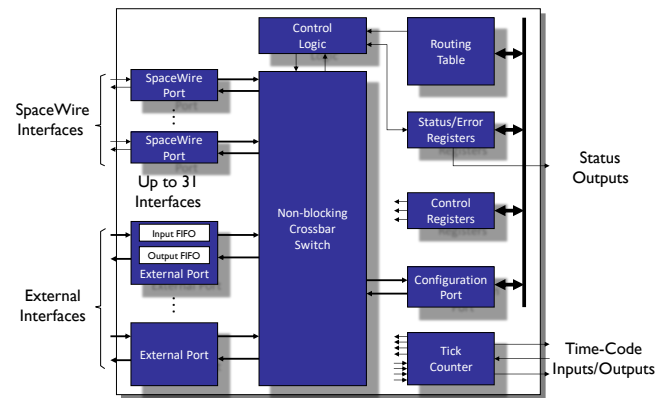
A configurable logical address table provides support for two levels of priority, header deletion and group adaptive routing.

Each port has a watchdog timer function which can be used to recover blocked network paths.

### Features

The STAR-Dundee SpaceWire Router IP permits the creation of a compatible, flexible wormhole router based on a non-blocking crossbar switch. The router features:

- Up to a total of 31 SpaceWire and/or FIFO ports
- Non-blocking, fully connected switch
- Ports can be set to start automatically when packets are ready to send and to stop when there is no data to send
- Internal configuration port with APB access option
- Logical address table with group adaptive routing option
- Internal status/error registers accessible via the configuration port or APB



SpaceWire Router function overview

## Resource Utilisation

The approximate utilisation figures for typical IP core configuration with 32-byte transmit and receive packet FIFOs is given in the table below. Xilinx FPGA results are obtained using XST or Vivado Synthesis tool depending on the device

IP Core	Virtex-5QV XQR5VFX130	UltraScale KU060
SpaceWire Interface	0.6% / 0.6%	0.1% / 0.1%
RMAP <sup>(1)</sup>	2.0% / 1.9%	0.5% / 0.2%
SpaceWire Router <sup>(2)</sup>	11.3% / 8.4%	2.8% / 1.1%

% LUT / % FF utilisation

<sup>(1)</sup> RMAP Target utilisation

<sup>(2)</sup> SpaceWire Router with 8 SpaceWire ports, 1 host FIFO port and embedded RMAP configuration port

## Delivery Files

The STAR-Dundee IP Cores are provided with reference designs for a number of development kits including the KCU105 development kit.

A comprehensive set of example test cases with ModelSim/Quarta simulation scripts is also provided

## Licensing

STAR-Dundee offers essential SpaceWire interface and network components as VHDL IP blocks for use in FPGAs and ASICs. Our IP has proven to be robust and is widely used across the space industry, having been integrated into many flight FPGAs and flight ASICs.

Each of our SpaceWire IP cores has the following features:

- Delivered as synthesisable VHDL source code in obfuscated or clear code format
- Configurable, giving flexibility through generics in the VHDL source
- Easily targeted at Xilinx FPGA families including space-qualified devices (XQRKU060 and Virtex-5QV) and commercial devices (Spartan-6, Kintex-7, Artix-7, etc.)

For more information on the IP cores, licencing, or for custom requirements, please contact us.