XDF XILINX DEVELOPER FORUM

System Design from Antenna to Digital
with Zynq UltraScale+ RFSoC

Presented By

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RF & Microwave FAE
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XILINX

AGENDA

- Software-defined Radio for LTE Band-3 1800 MHz
  - System design with Zynq® UltraScale+™ RFSoC + Qorvo RF
- Avnet RFSoC Support Package for MATLAB® and Simulink®
  - Modeling
  - Simulation and algorithm exploration
  - Verification
- Demo

CHALLENGES OF MODERN WIRELESS SYSTEM DESIGN

Requires multi-disciplinary expertise

- Wireless system architecture, knowledge of evolving standards
- RF design
- FPGA design
- Embedded software design
- Analog and digital signal processing
- IP network architecture
- High-speed layout / signal integrity board design

Need proven pre-engineered subsystems for fast proof-of-concept

EBV Elektronik
An Avnet Company

SYSTEM DESIGN

Software-defined Radio for
LTE Band-3 1800 MHz

SMALL CELL WIRELESS NETWORKS

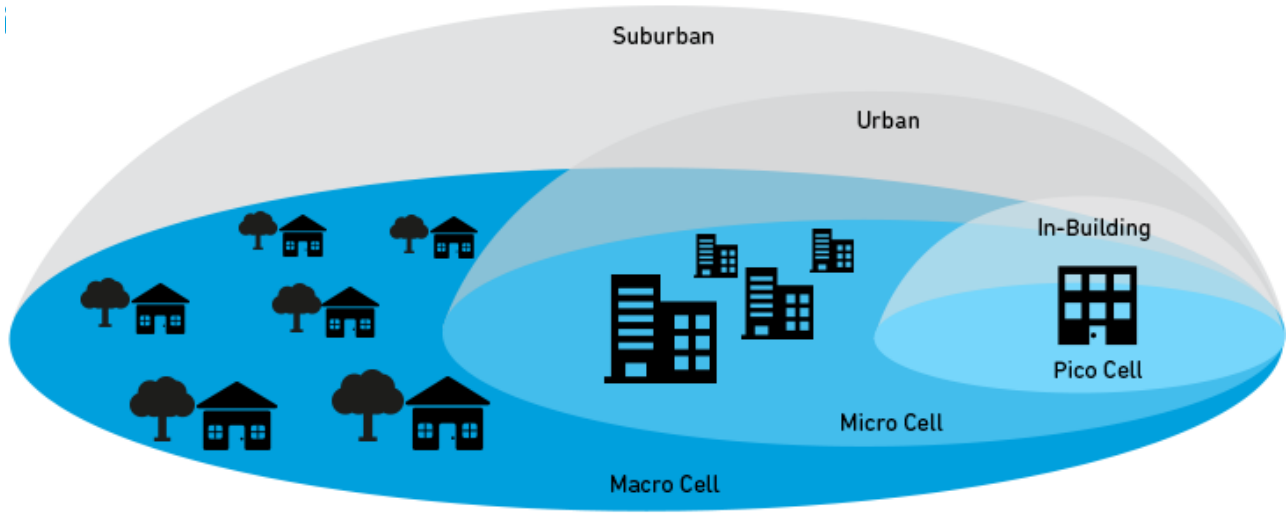
Network densification towards 5G

- In pre-5G/LTE-Advanced Pro (LTE-A Pro) transition

Small cells

- Provide increased data capacity
- Help service providers eliminate expensive rooftop systems
- Help improve the performance of mobile handsets

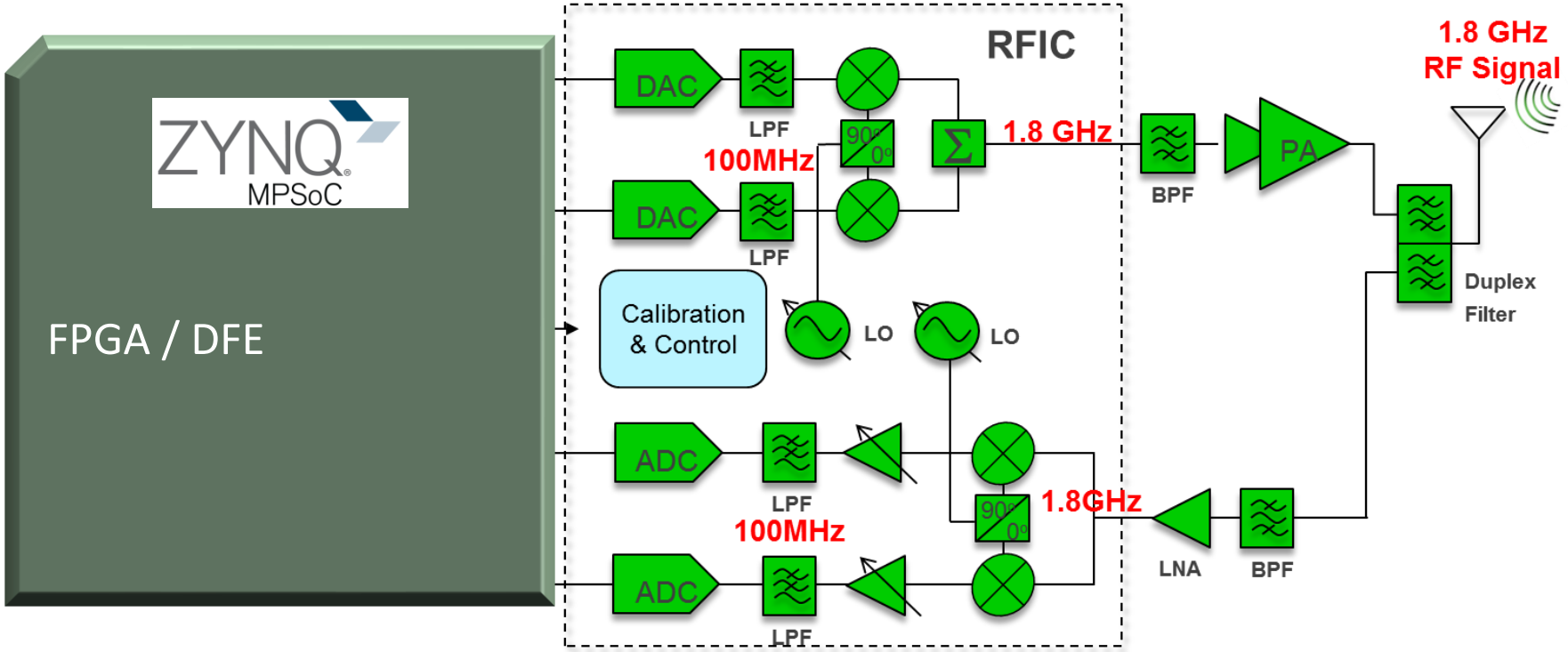
Base Station Categories



Cell Type	Output Power (W)	Cell Radius (km)	Users	Locations
Femtocell	0.001 to 0.25	0.010 to 0.1	1 to 30	Indoor
Pico Cell	0.25 to 1	0.1 to 0.2	30 to 100	Indoor/Outdoor
Micro Cell	1 to 10	0.2 to 2.0	100 to 2000	Indoor/Outdoor
Macro Cell	10 to >50	8 to 30	>2000	Outdoor

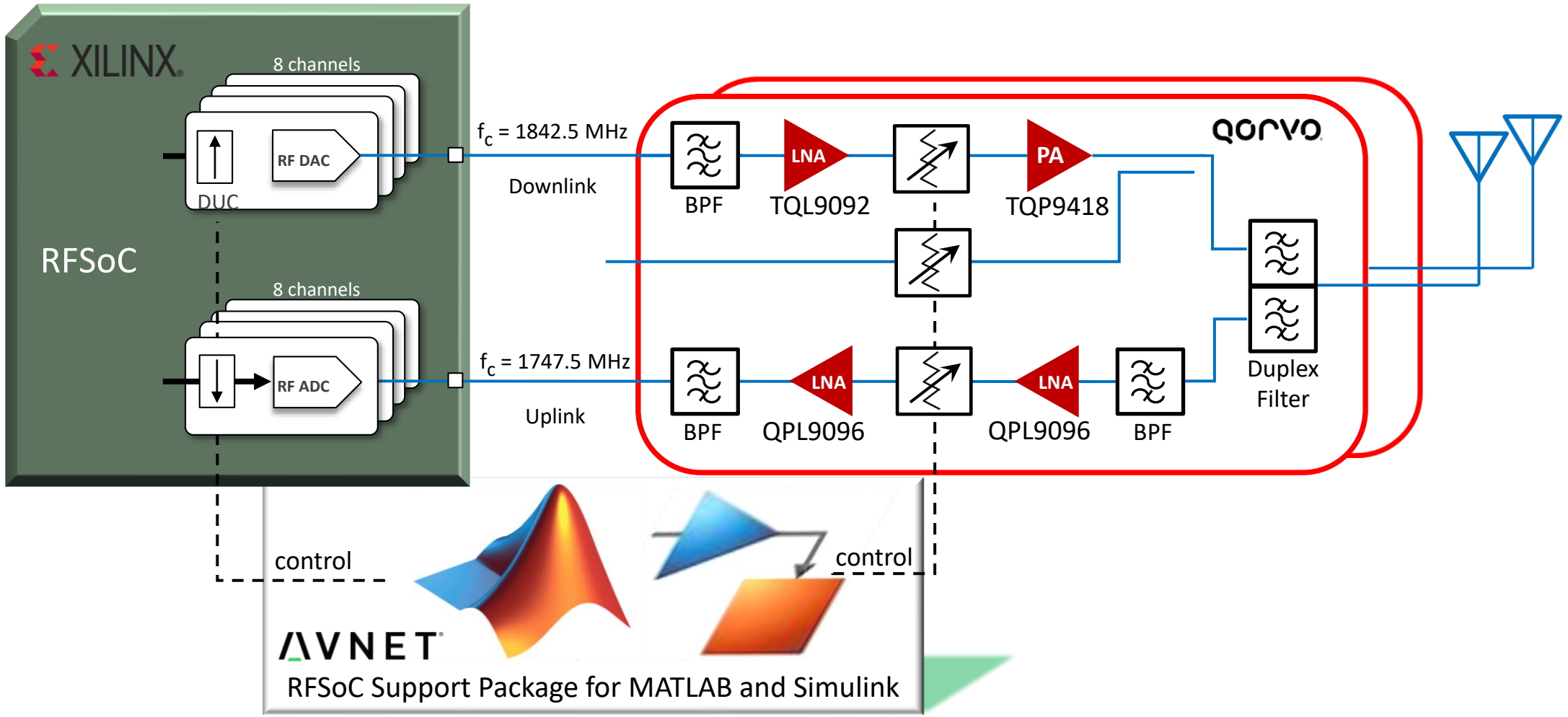
qorvo

TRADITIONAL BASEBAND/IF SAMPLING & RF SIGNAL PROCESSING



- Extra complexity, cost and power consumption
- Signal processing in the analog/RF domain with analog mixers and filters
- I/Q phase & gain imbalance, LO leakage, voltage and temperature variation

SOFTWARE-DEFINED RADIO FOR LTE BAND-3 1800 MHZ



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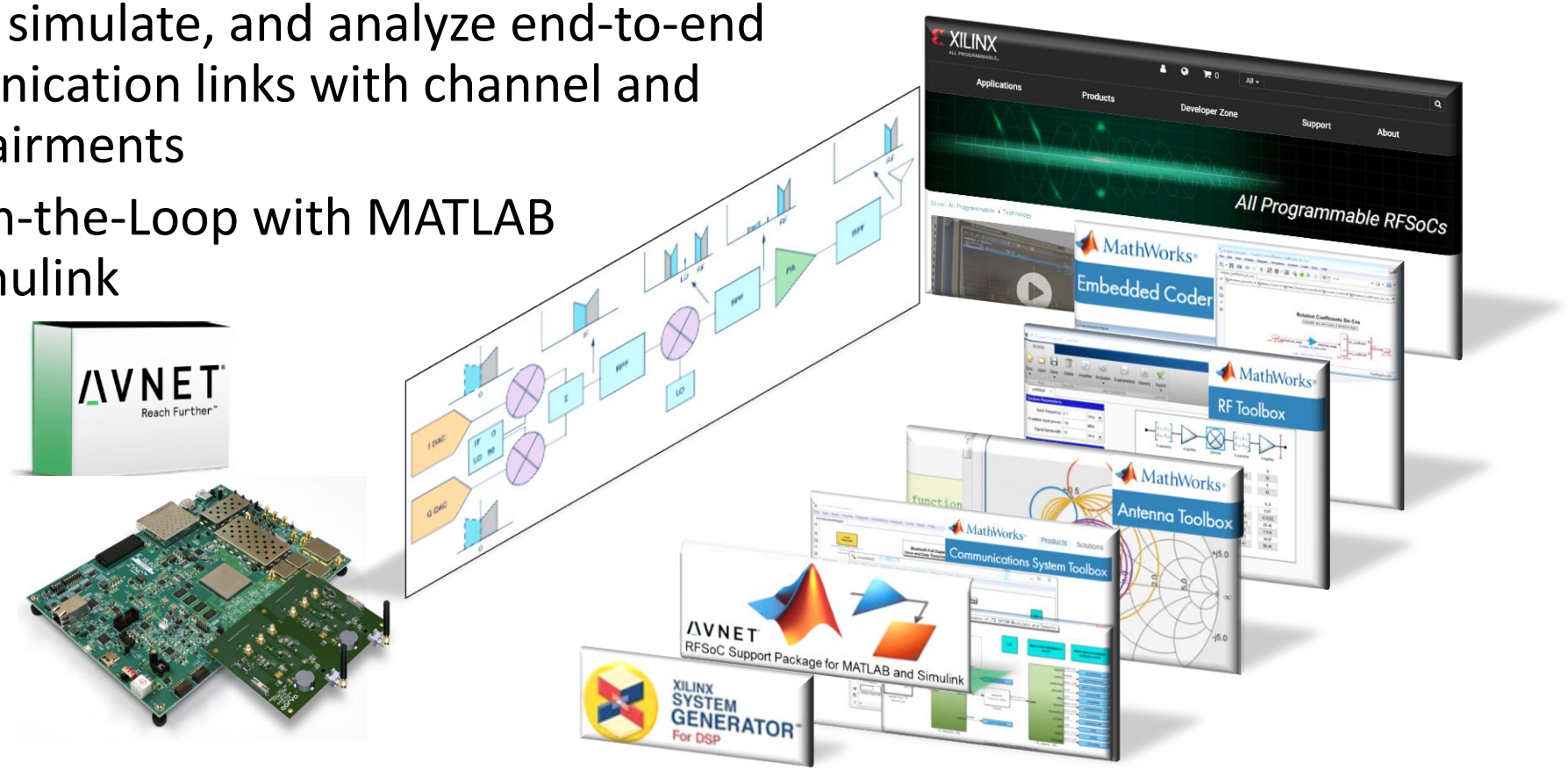
AVNET RFSOC SUPPORT

Package for MATLAB
and Simulink

MULTI-DOMAIN SIMULATION FROM ANTENNA TO DIGITAL

- Design, simulate, and analyze end-to-end communication links with channel and RF impairments
- Radio-in-the-Loop with MATLAB and Simulink

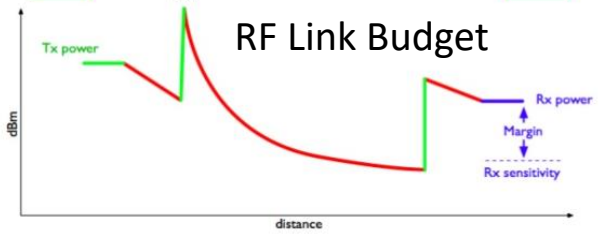


MODELING THE SIGNAL CHAIN FROM BASEBAND TO RF

Case Study: LTE Band-3 1800 MHz → **Modeling the RF Signal Chain** → **Algorithm Exploration** → **Demo Avnet RFSoC Development Kit**

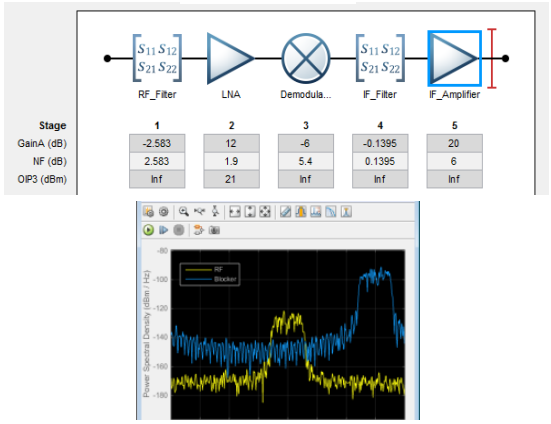
MathWorks

$$Rx_B = Tx_A + G_A - L_{fs} - A_{Rain} + G_B$$

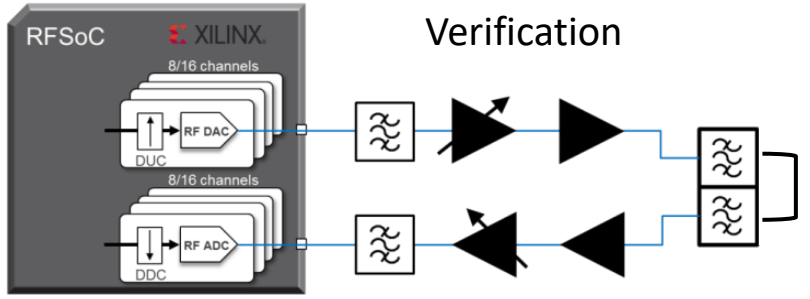


RF Link Budget

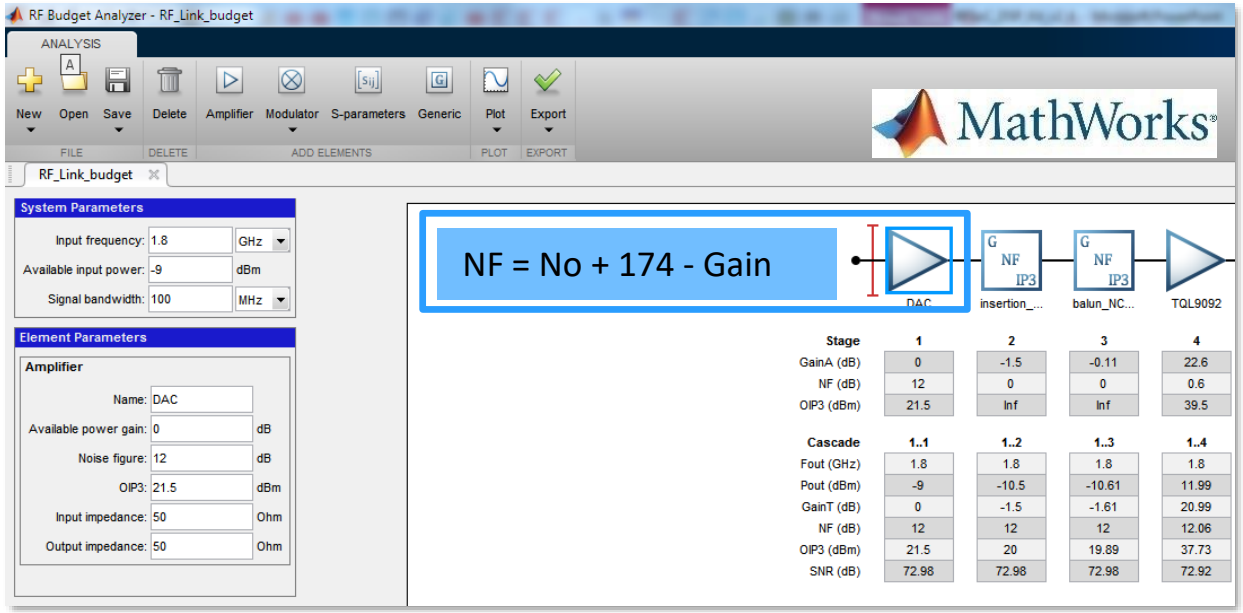
Simulation

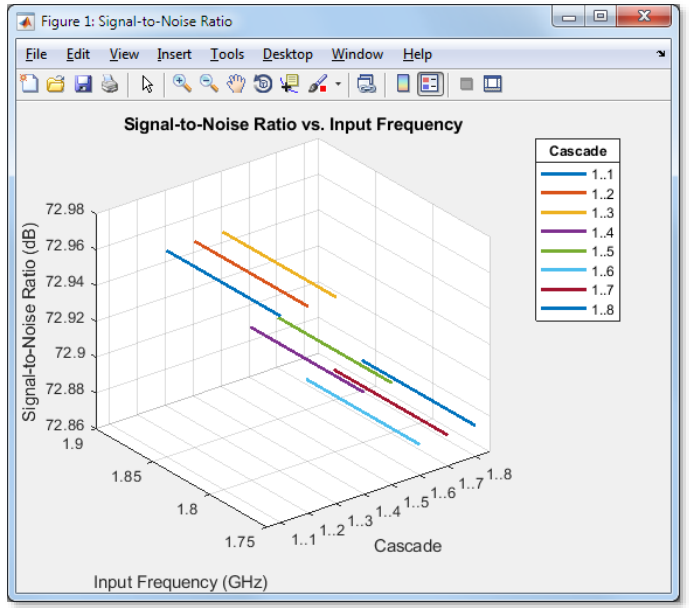


Verification



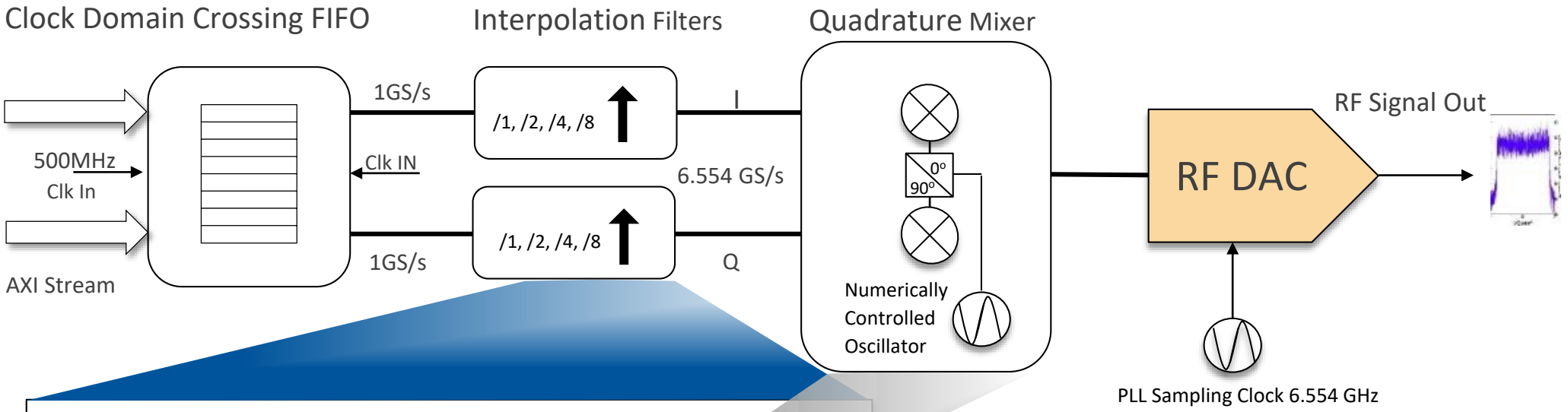
RF LINK BUDGET ANALYSIS OF RF SIGNAL CHAIN

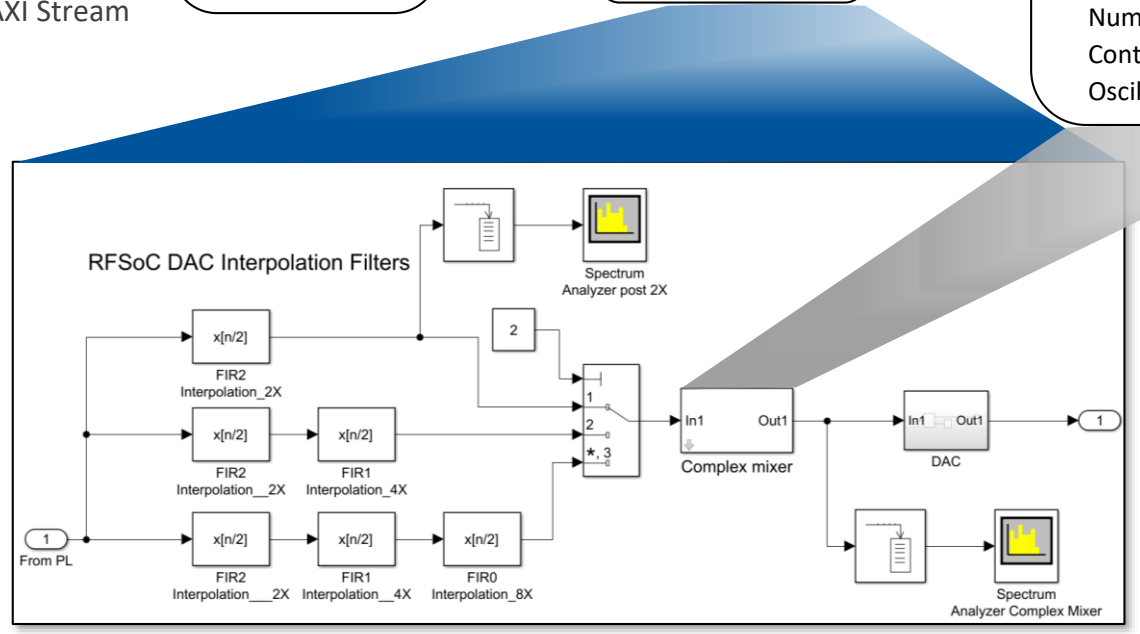




- MathWorks RF Budget Analyzer App
- Analyze gain, noise figure, and IP3 of cascaded RF elements
- Plot RF budget results across bandwidth and from stage to stage
- Export to RF Blockset for simulation within larger model

MODELING THE DIGITAL UP-CONVERTER IN RF-DAC TILE

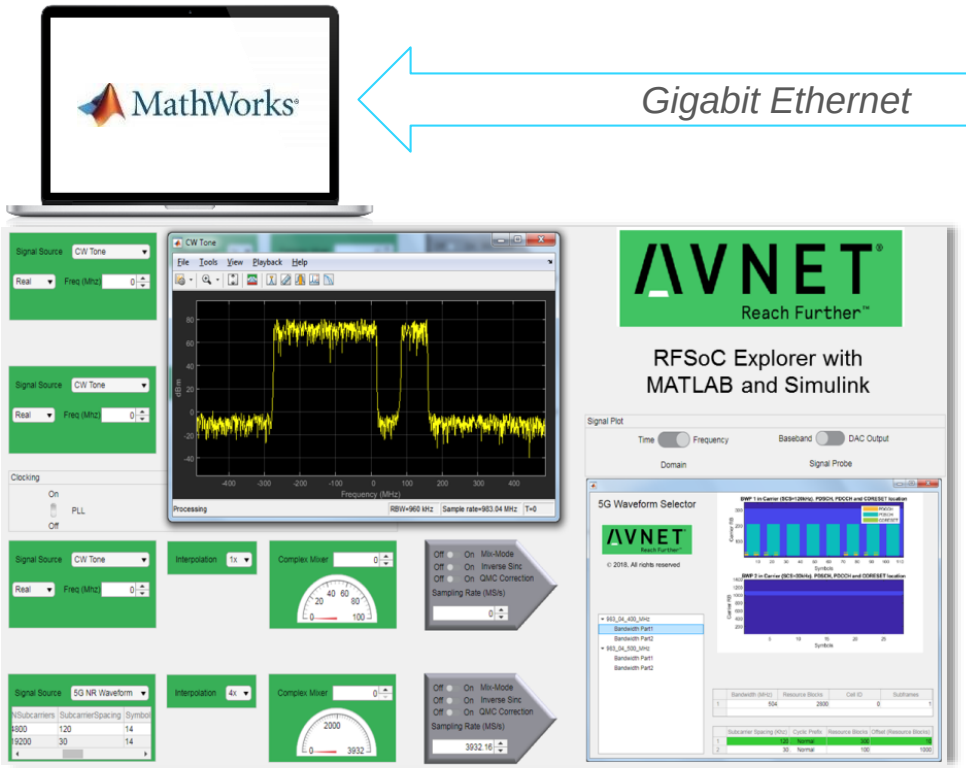




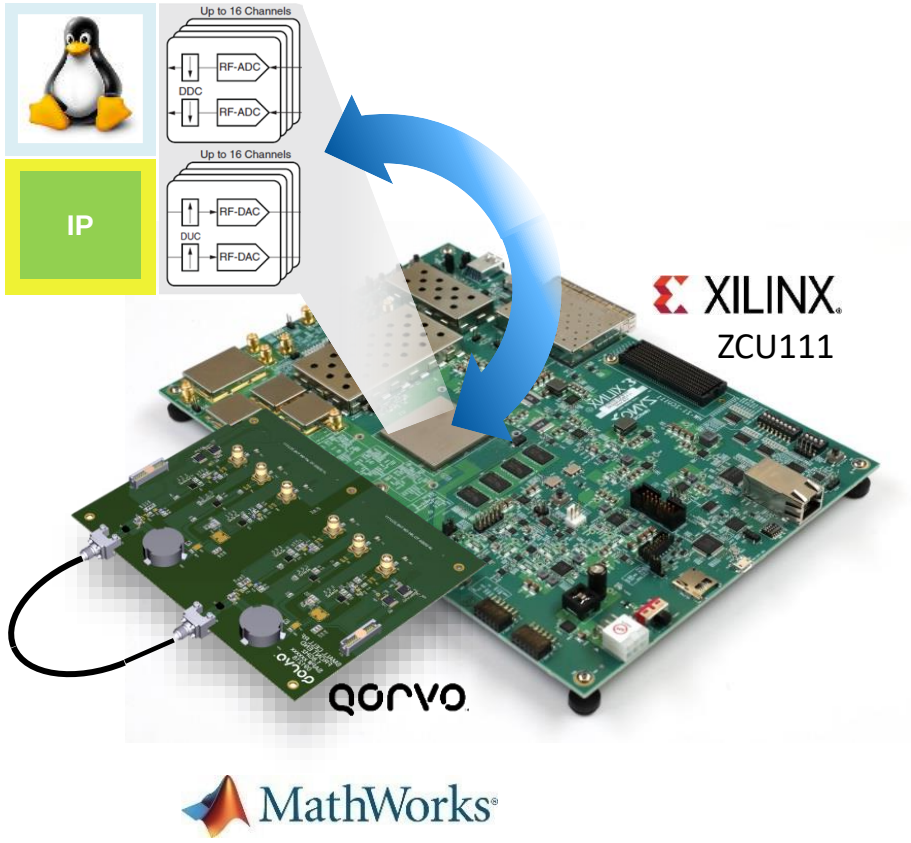
- Simulink model of hardened DUC in RF-DAC
  - cascaded halfband interpolation filters
  - quadrature mixer
- Aid for frequency planning, post-DAC analog reconstruction filter

ALGORITHM EXPLORATION WITH ZYNQ ULTRASCALE+ RFSOC

Case Study: LTE Band-3 1800 MHz → **Modeling the RF Signal Chain** → **Algorithm Exploration** → **Demo Avnet RFSoC Development Kit**



Gigabit Ethernet

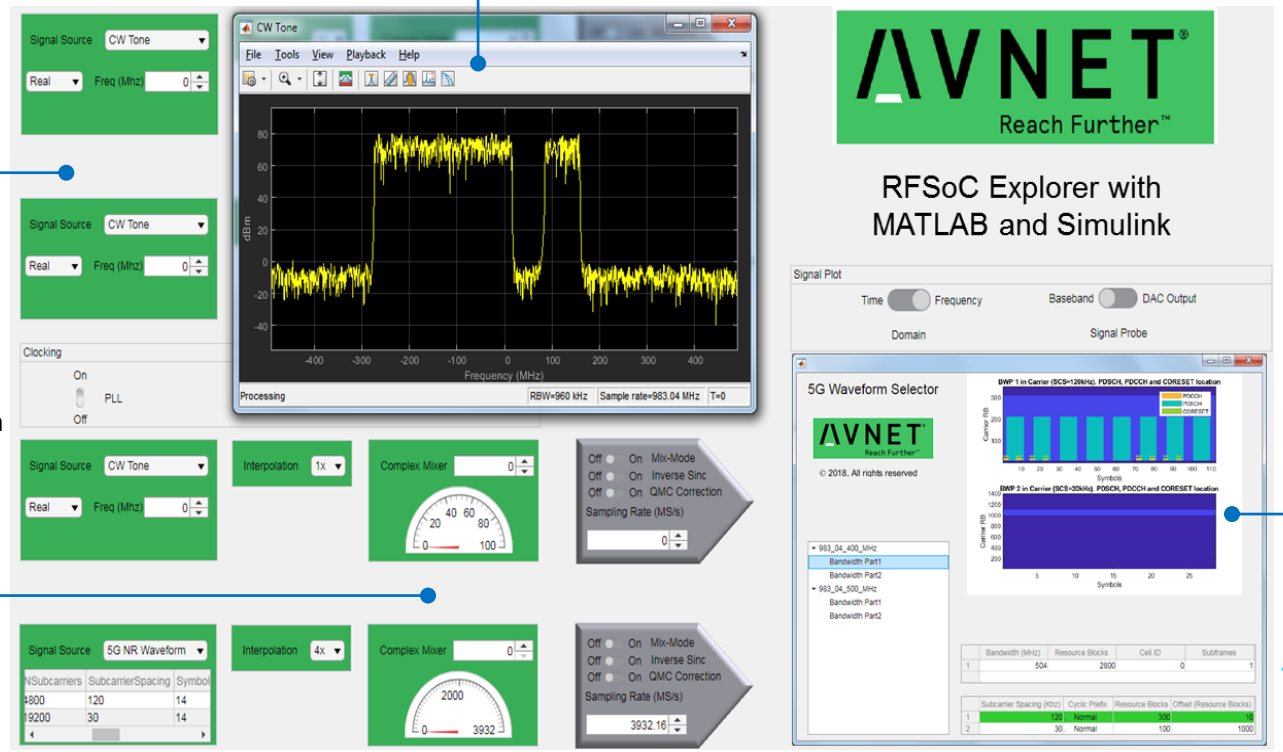


AVNET RFSOC EXPLORER WITH MATLAB AND SIMULINK

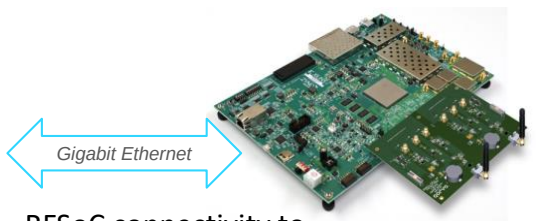
Generate signal stimuli within MATLAB
- real / complex sinusoids
- LTE / 4G waveforms
- 5G NR radio Release 15

Analyze signals in time and frequency domains

Control RFDC in MATLAB
- DAC / ADC settings
- Interpolation / decimation
- Complex mixer
- Sampling rate



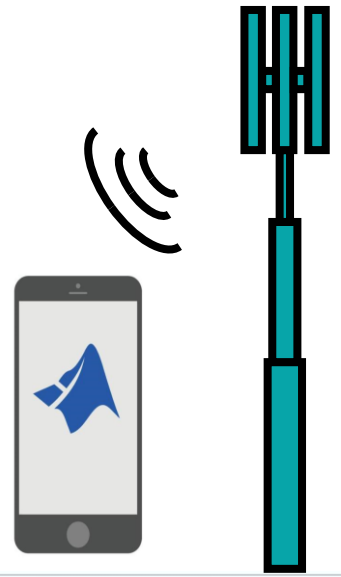
5G Toolbox from MathWorks
Simulate, analyze, and test the physical layer of 5G communications systems



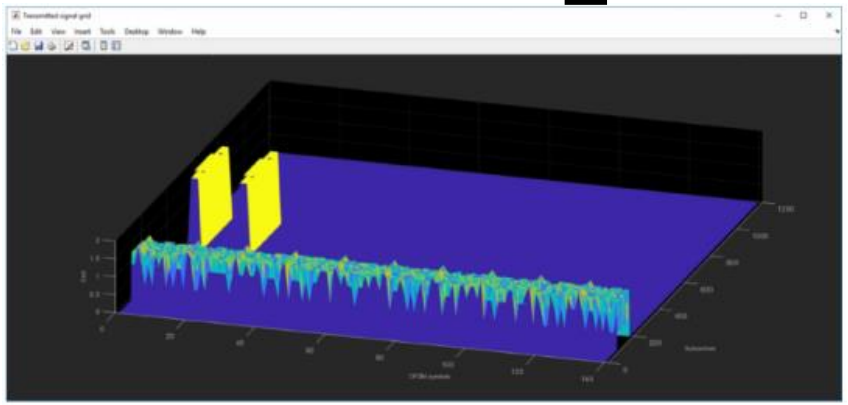
RFSoC connectivity to
MATLAB and Simulink

MathWorks®

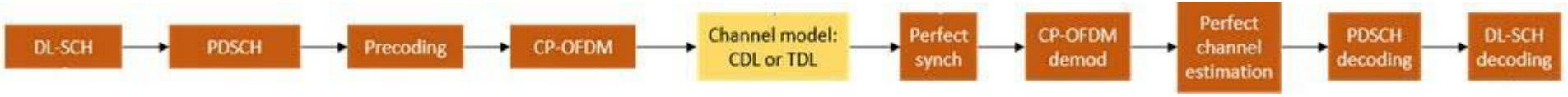
MATHWORKS 5G TOOLBOX™



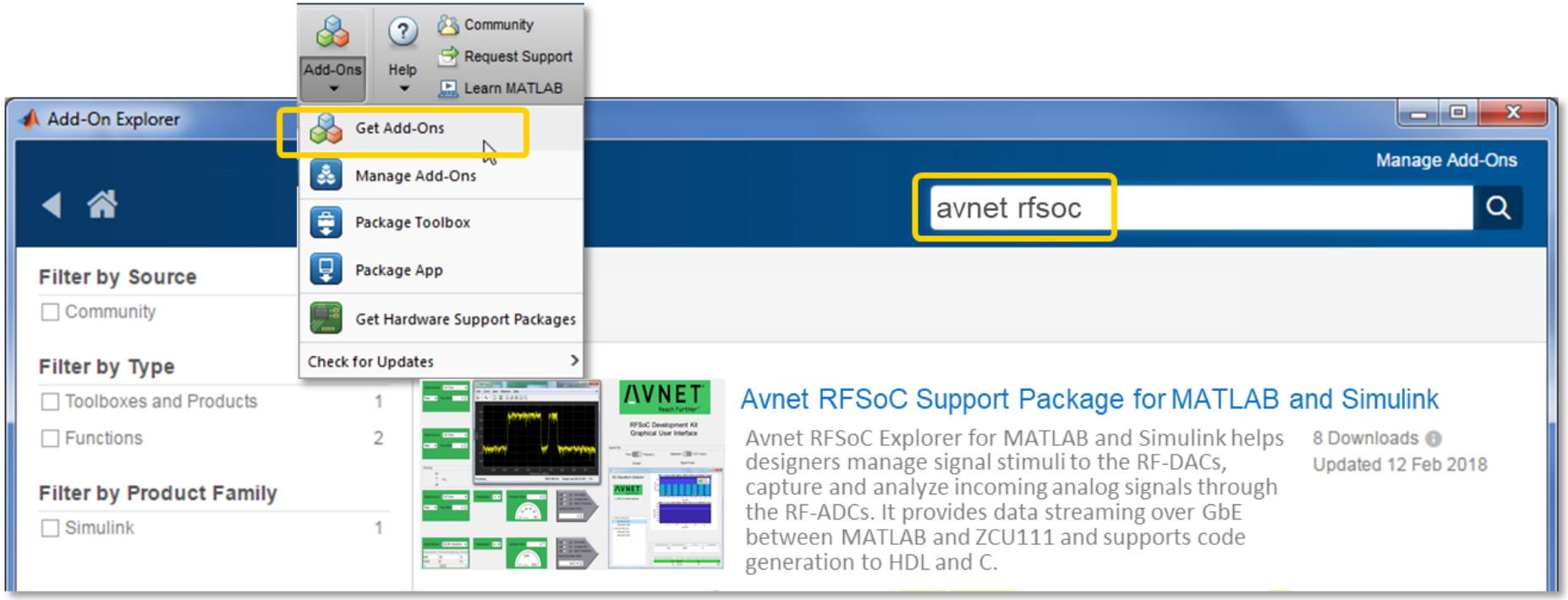
- Model, simulate, design and test 5G systems with MATLAB
- Waveform generation
- Downlink processing - Transmit and receive
- TDL and CDL channel models
- Physical channels and signals
- Link-level simulation & throughput measurements
- Synchronization Bursts
- Cell search procedures
- Reference designs as detailed examples



MathWorks®



RFSOC SUPPORT PKG IN MATLAB ADD-ON EXPLORER



- Works with Free MATLAB Trial Package for Wireless Communications

www.mathworks.com/rfsoc

AVNET ZYNQ ULTRASCALE+ RFSOC DEVELOPMENT KIT

Avnet extends the functionality of the groundbreaking Zynq® UltraScale+™ RFSoC ZCU111 Evaluation Kit with a Qorvo 2x2 LTE Band-3 RF front-end card, plus native connection to MATLAB & Simulink from MathWorks with support for 5G NR radio Release 15

Enables system-level design with:

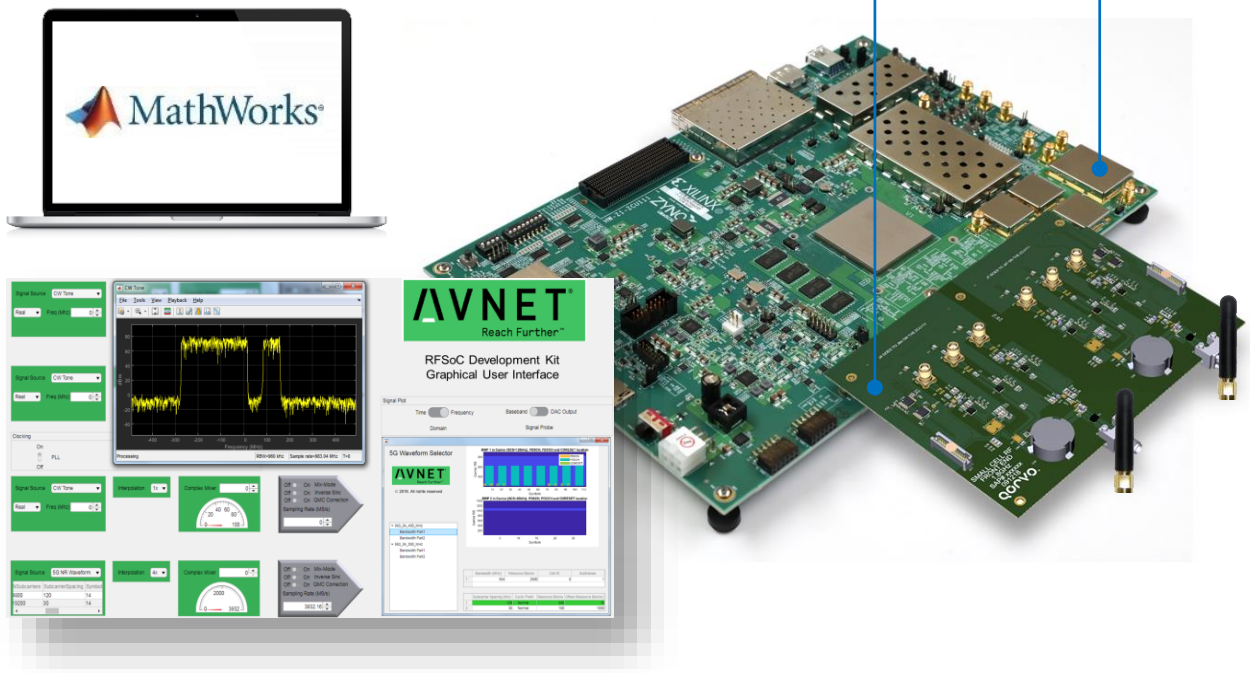
- Signal Capture & Analysis with MATLAB and Simulink
- Radio-in-the-loop co-simulation (Gigabit Ethernet)
- Over-the-air testing with 2x2 LTE Band-3 1800MHz FDD
- Direct-RF sampling without an external RF mixer

Kit includes:

- Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit
- Qorvo 2x2 LTE Band-3 RF front-end card
- Vivado System Edition (includes System Generator DSP)
- Avnet RFSoC Support Package for MATLAB & Simulink

Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit
Xilinx OEM kit including XM500, Filters, Cables, etc.

Qorvo Small Cell RF Front End
2x2 1800MHz FDD LTE Band 3



www.zedboard.org/rfsoc or www.mathworks.com/rfsoc

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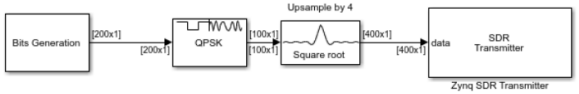
CONTINUITY — INNOVATION

APPENDIX

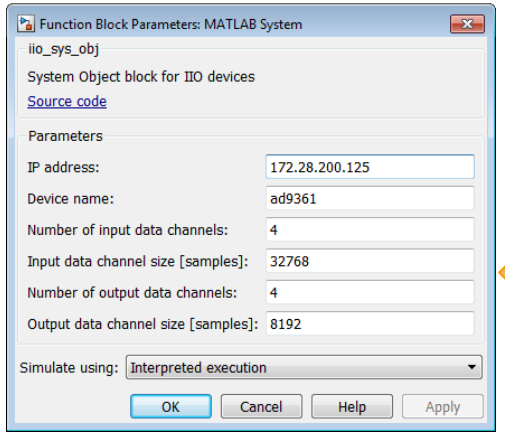
SYSTEM OBJECTS™ SIMPLIFY RFSOC USER INTERFACE

Algorithm Developer

MathWorks®

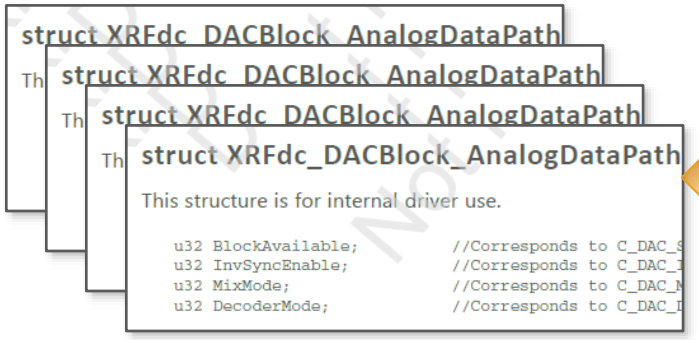


System Objects™

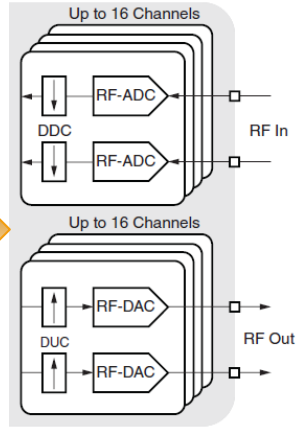


C Programmer

XILINX®



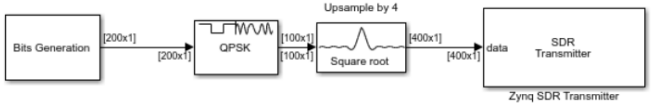
ZYNQ RFSoC



- MathWorks System Objects implement and simulate dynamic systems
- Custom System Object encapsulates functionality of RFSoC Data Converter Subsystem

CODE GENERATION WITH ZYNQ ULTRASCALE+ RFSOC

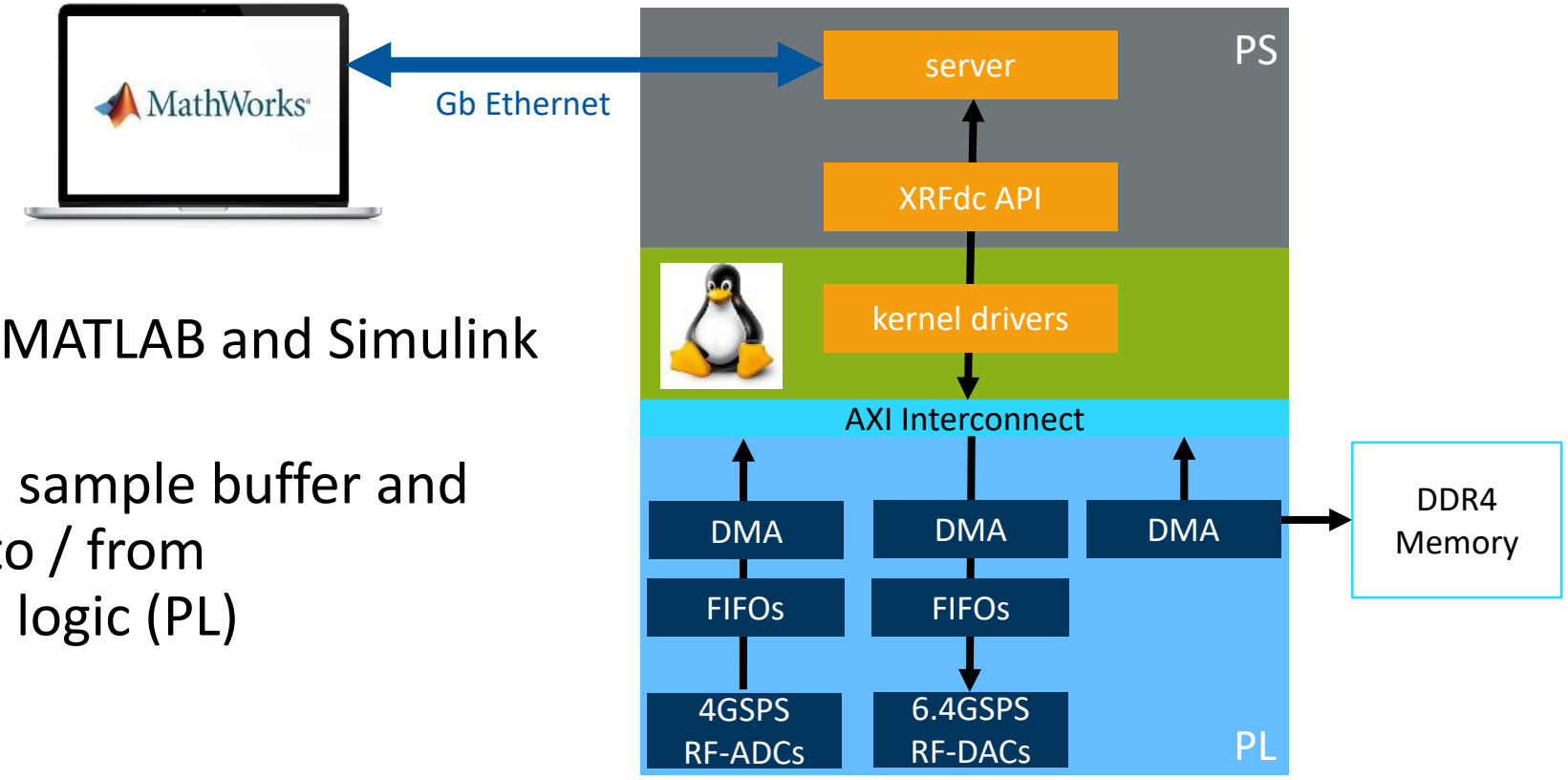
code generation



MathWorks

- HDL Coder & Embedded Coder for code generation
- Real-time execution on RFSoC board for over-the-air testing
- Runtime debug and instrumentation over Ethernet
- PetaLinux with open-source Linux drivers for product deployment

AVNET RFSOC SUPPORT PACKAGE FOR MATLAB AND SIMULINK



- Connection to MATLAB and Simulink over TCP
- Variable-depth sample buffer and DMA transfer to / from programmable logic (PL)