



**Radisys and Xilinx  
Collaboration for gNB  
Solution**

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September 2020

# Radisys Introduction

## DNA of Open Telecom Innovation

1987-1995

### Founded 1987

Vision: Bring Intel Silicon to Telecom  
IPO 1995  
Acquired IBM Open Platform division

2006-2011

### Acquired

Convedia: Media Server  
Continuous Computing: Trillium

2012

### Pivoted Strategy

Focus:  
Tier 1 Carrier - direct and indirect

2017

### Open Radisys

Open, Disaggregated access and media solution, dev ops methodology

Dec 2018

### A Reliance Industries company

Innovate, Scale, Expand and Disrupt with Open Solutions

### Headquarters:

Hillsboro, OR  
United States

Global sales and operations

### Centers of Excellence:

Bangalore (India)  
Hillsboro, OR (US)  
Frisco, TX (US)  
Guangdong (China)  
Shanghai (China)

Over 30 years of experience and leadership in networking

Leading contributor to open standards organizations and initiatives

### No. of Employees:

~900

# Open: Our Vision for the Networks of Tomorrow

*Creating new digital experiences*

## Disaggregated

Software / Hardware  
Network Functions  
Control / Media

## Intelligent

Software Defined  
Programmable  
AI/ML

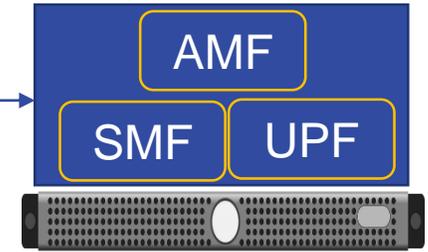
## Open

Software , Hardware, Interfaces



- Radisys and Xilinx play an important role in developing O-RAN compliant 5G solutions for OEM and ODM.
- Radisys provide complete 5G RAN Software protocol stack of CU ( Layer3+, PDCP/SDAP) and DU ( Layer 2+) modules where cryptographic algorithms and integrity protection also provided by Xilinx shall be used
- Radisys working towards developing all-programmable-scalable-reconfigurable FPGA Lower Phy solutions on State-of-Art Xilinx SoC Platforms
- Xilinx SoC platforms offer high performance programmable logic with accelerator blocks on Ethernet, CPRI and FFT enabling quicker implementation of 5G Solutions.
- Radisys designed & implemented Open Fronthaul Gateway (OFG) IP compliant to Split 7.2a ORAN FH CUS specification and interfaced with Radisys Trillium O-DU.
- Radisys OFG solution has been ported on Xilinx SoC & interoperability tested with various 3GPP/ORAN compliant O-DU Test Equipment.
- Radisys have a broad test suite for end to end OTA testing to enable customer with faster time-to-market.

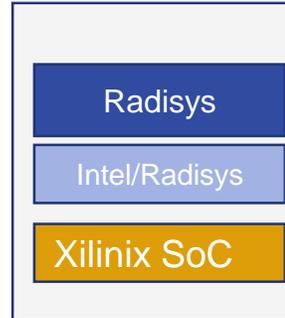
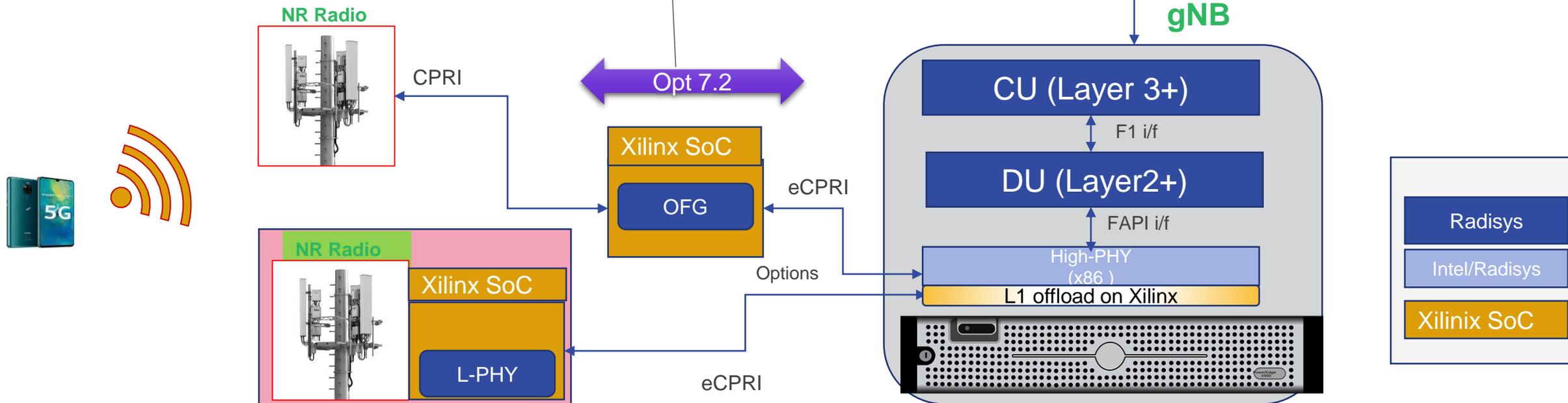
## 5GCore



Radisys offer gNB Software running on Xilinx SoC platform for

- using state-of-the-art accelerator cryptographic algorithms for cciphering and Integrity
- L1 upper offloading on Xilinx SoC
- Ported Open Fronthaul Gateway solution on Xilinx SoC
- Lower -PHY offload

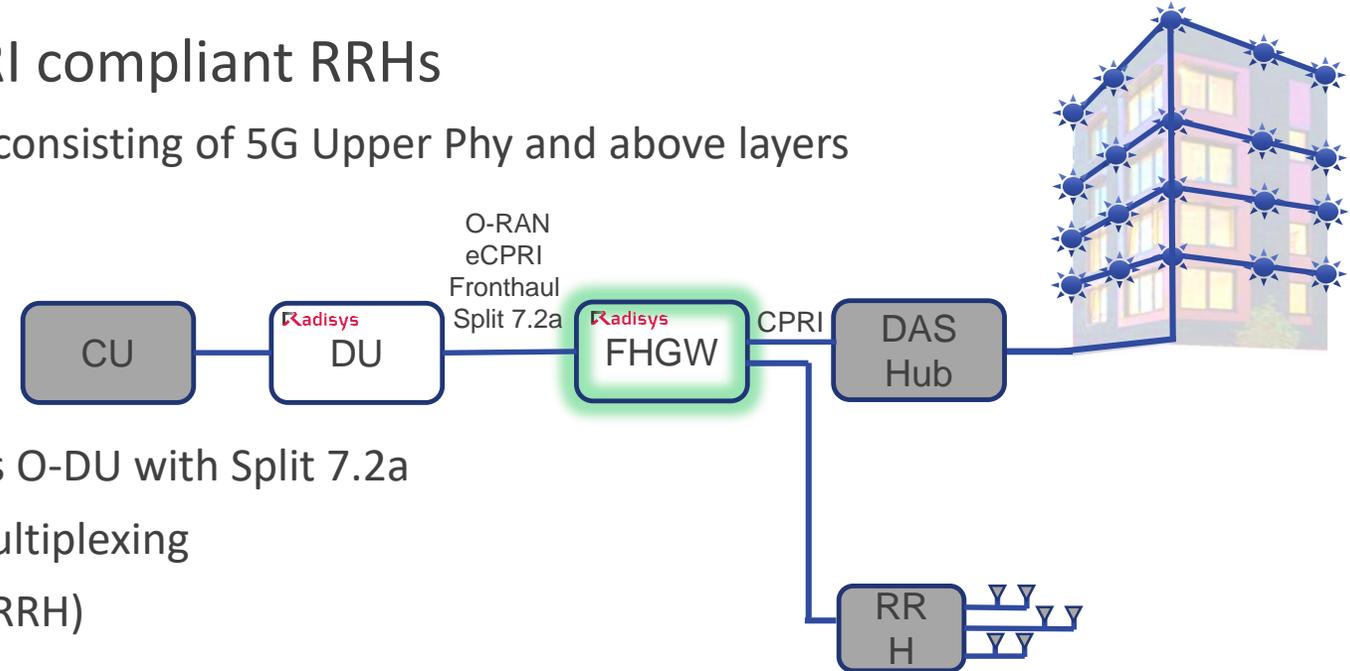
Fronthaul solution are compliant to 7.2x ORAN



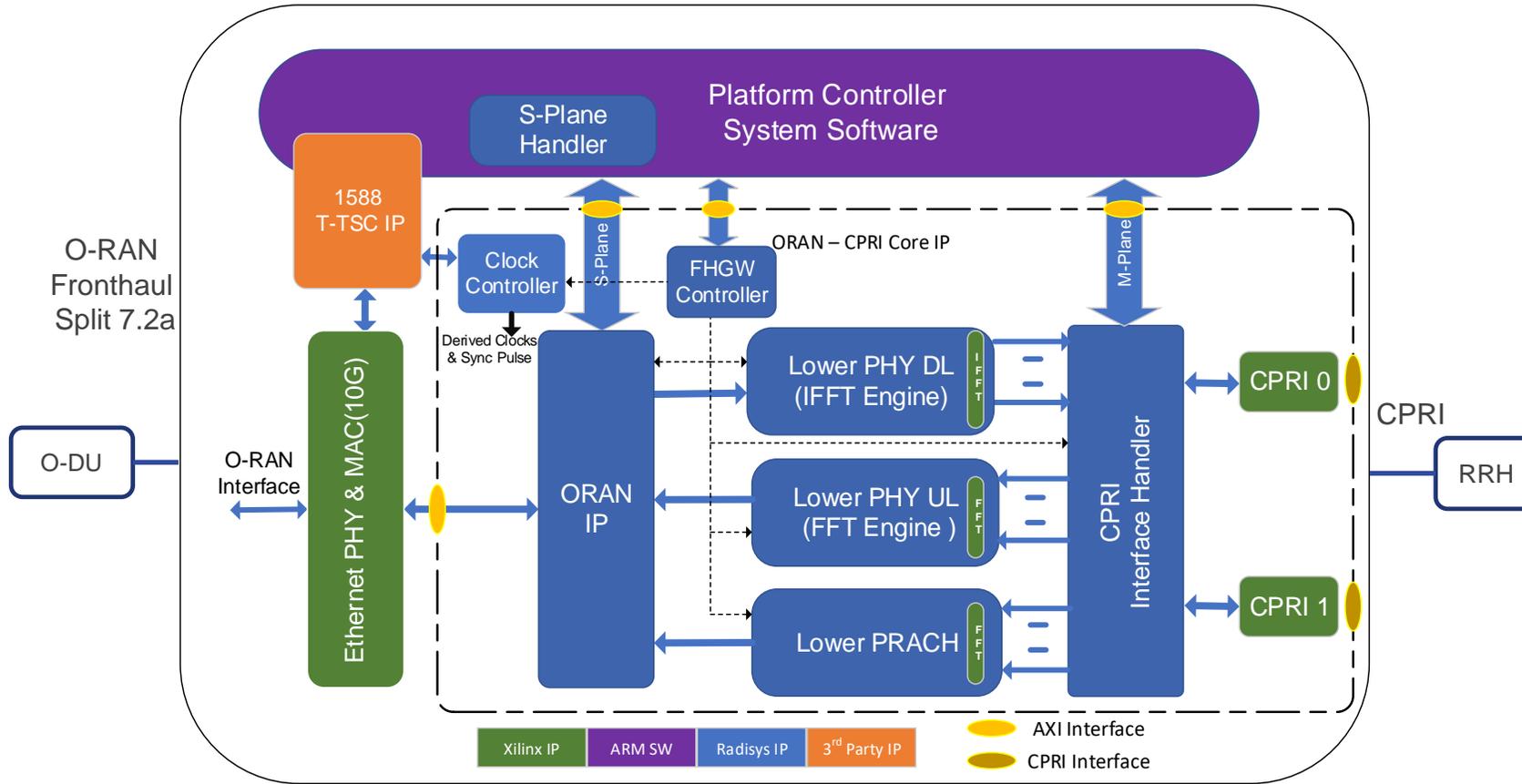
- OFG interfaces 5G NR O-DUs with CPRI compliant RRHs
  - O-DU: O-RAN FH compliant Distributed Unit, consisting of 5G Upper Phy and above layers
  - RRH: Remote Radio Head

- OFG Functionalities

- O-RAN compliant Fronthaul Interface towards O-DU with Split 7.2a
- Carrier, Antenna Stream Multiplexing / De-Multiplexing
- Lower Phy Functions (Not available in legacy RRH)
  - FFT / IFFT, CP Processing (DL & UL)
  - PRACH Pre-Processing
  - Synchronization, Stream Management
- CPRI Interface towards RRH (Single / Multi Carrier per RRH)
- Management Plane support with Platform Control Processor
- Dynamic Re-Configurability



# Block Diagram and Specification of FHGW



Feature	Specification
Split Point	7.2a
# Carriers	8
# Antenna	2
MIMO rank	Up to 2
Single carrier BW	5, 10, 15 or 20 MHz
Duplex mode	FDD
SCS	15 KHz
Frame structure	3GPP 5G NR
Cyclic prefix	Normal CP
PRACH processing	5G NR Short Format
4G & 5G Coexistence	No
IQ sample width	16
Synchronization	PTP 1588
Latency	DL – V.06, UL – R.08
Ethernet line rate	10G
Ethernet protocol	eCPRI
CPRI Output Ports	2
CPRI Line Rate	10.1 Gbps

Note: FFT/IFFT IP Core of L-PHY engine is a Xilinx IP



Compliant to OFH CUS Plane Specification v2.0



Section 1,3 support with up to 16 Sections per Carrier



Application layer Fragmentation, Jumbo Frame Support



Dynamically reconfigurable Carrier Configuration



Fiber offset compensation



3GPP 5G NR Compliant Air Interface



5G NR PRACH Short format support



CLI based Management

- Strong RTL Design Team
  - Coupled with expertise in Wireless Communication
  - Strong command in Verilog & SystemVerilog
- System Modelling with Matlab
  - End to End Reference model
  - Unit, Module & End-to-End Test Vectors at numerous reference points
- FPGA Development Tools
  - Xilinx Vivado, Intel Quartus Prime, Mentor Graphics QuestaSim
- HIL (Hardware In Loop) enabled Test Framework
  - Xeon Server based HIL Framework coupled with Reference Test Vectors
  - Unit, Module, on-board & DU Integration Test Case Support
- In-house O-DU Design Expertise
  - Interface proven with In-house O-DU
  - End to End Solution expertise

A nighttime panoramic view of the Shanghai skyline, featuring the Bund and the Huangpu River. The city is illuminated with various lights, and several glowing white arcs of light sweep across the sky, creating a sense of motion and connectivity. The Radisys logo is prominently displayed in the center.

# Radisys

Thank You