Launching Industry’s First 20nm Radiation Tolerant FPGA for Space Applications

Minal Sawant
Space System Architect

May 19, 2020
Space Industry Market Challenges & Requirements

- Downlink Bandwidth is limited
- Fast time to market
  - Platform Concept for reuse on multiple missions
- Low Latency and High Bandwidth
  - E.g. Seamless and reliable connectivity for broadband communications
- Machine Learning in orbit

- Need for capability to process on board a satellite vs ground station
  - Reduce Development Time to launch (2-3 years Vs 5-6 years)
  - Process hundreds of Gbps data streams in real time
- Flexible System Architecture
  - Change algorithms “on the fly”
- Reliable components for long mission life, extreme environments
- SWaP (Size, Weight and Power) Tradeoffs
Key Target Markets and Applications
For Reconfigurable Payloads

- Communication Payloads
  - Channelization
  - Beamforming
  - Phased Array Processing

- Earth Observation Payloads
  - Hyperspectral Cameras
  - Synthetic Aperture Radar

- Space 2.0 Constellations
  - Broadband Internet
  - High Speed Networks

- Science Missions
  - Display Modules
  - Instruments
  - Video Processing

Civil, Commercial & Defense Satellites

Signal Processing, HW/SW Reconfigurable, Robust Package, Space Grade Tested, On Orbit Flexible
Introducing the 20nm RT Kintex UltraScale FPGA
Building on 20+ Years of Heritage

Adaptive Computing for Ultra High Throughput, High Bandwidth Satellite Applications

- True Unlimited On-Orbit Reconfigurable Solution
- >10X DSP Compute increase for Processing Intensive Algorithms & Analytics
- Full Radiation Tolerance across All Orbits
- Machine Learning Ecosystem enables High Performance Edge Inference in Space
Radiation Tolerant Kintex UltraScale XQRKU060
Process, Analyze & Reconfigure
RT Kintex UltraScale Platform
High Bandwidth Compute Capability

Features

- 2760 DSP Slices: Multi-precision fixed and floating point modes
- 32 High Speed SERDES (12.5Gbps): 400Gbps aggregate BW
- Radiation Tolerance across all orbits TID >100Krad/si, SEL >80MeV·cm²/mg
- Robust 40x40 mm Ceramic Column Grid Array Packaging

Meets Next Generation on Orbit Processing Needs

- Protos, Mechanical Samples: NOW
- Vivado SW, XPE*, Datasheet: NOW
- Production (Class B, Class Y): Sept 2020

*XPE Xilinx Power Estimator Tool
TID = Total Ionizing Dose
SEL = Single Event Latchup
Simplified Development Environment
Vivado Design Suite

Next Gen Routing
- Redesigned routing architecture
- 2X routing resources, eliminates congestion

ASIC Like Clocking
- Flexibility for clock placement & balances skews

Intelligent 3D Analytical Placer
- Optimizes timing, congestion and wire length for efficient design placement
# Space Resilient
Radiation Tolerance & Reliability Across All Orbits

## Radiation Tolerance

<table>
<thead>
<tr>
<th>Radiation</th>
<th>Unit</th>
<th>LEO, MEO, GEO, Polar, Deep Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>&gt;100 krad(si)</td>
<td>√</td>
</tr>
<tr>
<td>Single Event Latchup</td>
<td>80 MeV·cm²/mg @125°C</td>
<td>√</td>
</tr>
<tr>
<td>SEU&lt;sub&gt;CRAM&lt;/sub&gt;</td>
<td>1 x 10&lt;sup&gt;-8&lt;/sup&gt; upset/bit/day</td>
<td>√</td>
</tr>
<tr>
<td>SEU&lt;sub&gt;BRAM&lt;/sub&gt;</td>
<td>2.7 x 10&lt;sup&gt;-8&lt;/sup&gt; upset/bit/day</td>
<td></td>
</tr>
</tbody>
</table>

## Silicon Reliability

<table>
<thead>
<tr>
<th>Silicon Reliability</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>20nm Family</td>
<td>&lt;1.2 ppm</td>
</tr>
<tr>
<td>Kintex Family</td>
<td>3.8 FIT &gt;3M Device Hours</td>
</tr>
<tr>
<td>XQRKU060</td>
<td>Passed 4000 Hours</td>
</tr>
<tr>
<td></td>
<td>Class Y (QML-Y Equivalent) per MIL-PRF38535 in Progress</td>
</tr>
</tbody>
</table>

## Package XQRKU060 Reliability

<table>
<thead>
<tr>
<th>Package XQRKU060 Reliability</th>
<th>Package XQR5QV Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNA1509</td>
<td>CNA1752</td>
</tr>
<tr>
<td>Construction, Materials Similar</td>
<td>Heritage in Space since 2009</td>
</tr>
</tbody>
</table>
Unlimited On Orbit Reconfiguration
Change-on-the-Fly Capability

On-Board Processing

Sensors
Rx

ADC
ADC
ADC

Rx

TMR MicroBlaze
System Monitor

DAC
DAC
DAC

Tx

DSP Slices
Block RAM

20nm Programmable Logic

True On-Orbit Reconfigurable

Signal Processing, Compression, Packetization, Format, Timing Control, Conversions, Filtering…

PCIe® Gen 3
High-Speed Serial Transceivers

High Range High Performance IOs

DDR3 DDR4

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Bringing Machine Learning to Space
“Process and Analyze” with Real-Time On-Board Processing

- Dense, power-efficient compute with scalable precision and large on-chip memory
- 5.7 TOPs peak INT8 performance (nearly 25X compared to prior generation space grade FPGAs)
- Triple Modular Redundant MicroBlaze™ supported by Xilinx Vitis™ Tools for ML-centric applications
Machine Learning on RT Kintex UltraScale
High Performance Neural Network Inference Acceleration

- Available flows today via open source compilers (FINN, HLS4ML)
- Low-latency, high-throughput performance with customizable pre/post-processing for CNNs & MLPs
- Supported ML frameworks include TensorFlow, Keras, PyTorch and others
- Multi-precision network support
  - Optimized for INT8 and below
- Future extensions to Vitis™ AI and Xilinx & Partner DPUs†

* Future Extension
† DPU = Deep Learning Processing Unit
Payload Use Case with RT Kintex UltraScale
Reconfigurable Telecommunication Satellite

Allows Operators to Change and Adapt Frequency Plans, Channelization Bandwidths and Routing Uplinks to Specific Downlinks
Payload Use Case with Unlimited On-Orbit Reconfiguration

An FPGA based on-board processor platform for space application**

Reconfiguration Can Be Done by

1. Storage of multiple bitstreams in the Non Volatile memory
2. On-Board Computer (OBC)
3. Ground Station

From satellite to earth

From earth to satellite

Non Volatile Memory

Configuration Manager

Payload

Xilinx XQRKU060 FPGA

Transponder

TTC

CDH (OBC)

Upload Compressed Bitstream

An FPGA based on-board processor platform for space application** Alexander Hofmann; Rainer Wansch; Robert Glein; Bernd Kollmannthaler, 2012 NASA/ESA Conference on Adaptive Hardware and Systems (AHS)
# Ecosystem of Solutions

Available Today

<table>
<thead>
<tr>
<th>Space Development Board</th>
<th>Alpha Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>Infineon Technologies</td>
</tr>
<tr>
<td>NVM</td>
<td>Infineon, Cobham</td>
</tr>
<tr>
<td>DDR3</td>
<td>3DPlus</td>
</tr>
<tr>
<td>MCU</td>
<td>Cobham</td>
</tr>
<tr>
<td>TMR Synthesis Tool</td>
<td>Mentor Graphics</td>
</tr>
<tr>
<td>IP</td>
<td>Star Dundee</td>
</tr>
<tr>
<td>Power Solutions</td>
<td>Texas Instrument</td>
</tr>
<tr>
<td>High Speed ADC</td>
<td>Texas Instrument, Teledyne e2V</td>
</tr>
</tbody>
</table>
# RT Kintex UltraScale Product Table

<table>
<thead>
<tr>
<th></th>
<th>XQRV4QV</th>
<th>XQRV5QV</th>
<th>XQRKU060</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Radiation Hardness</strong></td>
<td>Tolerant</td>
<td>Hard</td>
<td>Tolerant</td>
</tr>
<tr>
<td><strong>Process (nm)</strong></td>
<td>90</td>
<td>65</td>
<td>20</td>
</tr>
<tr>
<td><strong>Memory (Mb)</strong></td>
<td>4.1 to 9.9</td>
<td>12.3</td>
<td>38</td>
</tr>
<tr>
<td><strong>System Logic Cells (K)</strong></td>
<td>55 to 200</td>
<td>131</td>
<td>726</td>
</tr>
<tr>
<td><strong>CLB Flip-Flops (K)</strong></td>
<td>49.1 to 178.1</td>
<td>81.9</td>
<td>663</td>
</tr>
<tr>
<td><strong>CLB LUTs (K)</strong></td>
<td>49.1 to 178.1</td>
<td>81.9</td>
<td>331</td>
</tr>
<tr>
<td><strong>MGTs</strong></td>
<td>None</td>
<td>18 at 3.125 Gbps</td>
<td>32 at 12.5 Gbps</td>
</tr>
<tr>
<td><strong>User I/O</strong></td>
<td>640 to 960</td>
<td>836</td>
<td>620</td>
</tr>
<tr>
<td><strong>DSP Slices</strong></td>
<td>32 to 192</td>
<td>320</td>
<td>2,760</td>
</tr>
<tr>
<td><strong>Radiation (TID (krad/si), SEL (MeV cm²/mg))</strong></td>
<td>300, &gt;125</td>
<td>1,000, &gt;125</td>
<td>100, &gt;80</td>
</tr>
<tr>
<td><strong>Reliability (Package, Test)</strong></td>
<td>CNA1509; V-Flow</td>
<td>CNA 1752; B-Flow &amp; V-Flow</td>
<td>CNA 1509; B-Flow &amp; Y-Flow</td>
</tr>
</tbody>
</table>

**Comparison:**
- **10X**
- **5X**
- **8X**
20nm UltraScale in Reconfigurable Platform
Baselined in Application

- **Company**: SEAKR Engineering, Inc. Colorado
- **Product**: Reconfigurable Processor
- **FPGA**: 20nm UltraScale KU060
- **Function**: Interconnected with 12 Gbps SERDES links enabling high-throughput, flexible and reconfigurable modulation, demodulation, channelization and routing capability.
- **Application**: GEO SatCom

https://www.seakr.com/seakr-announces-new-rf-reconfigurable-processor-for-space-platforms/
Future Rollout for Space Applications

Radiation Tolerant: XQR
Defense Grade: XQ

Xilinx Class B, Class Y – Sept 2020
Xilinx DPU Support – Sept 2020
QML Class Y 2021-22

90nm
65nm
20nm
Next Gen Solution

Technology Nodes

Shipping Today
Shipping Today

Virtex XQR4QV
Virtex XQR5QV
Kintex XQRKU060

Directional Plan*
SIP, Higher Density FPGAs,
Next Gen Nodes
XQ Ruggedized, Machine
Learning, Vitis

* Xilinx evaluating these solutions

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Strong Adoption and Heritage for 20+ Years

PAST
- GRACE
- MER
- TerraSAR

PRESENT
- OSIRIS REx
- Iridium NEXT
- Curiosity Rover

FUTURE
- Perseverance MARS2020
- ExoMARS
- Next Gen Payloads
Key Takeaways

Industry’s First 20nm Radiation Tolerant (RT) FPGA Targeted for Ultra High Throughput & High Bandwidth Satellite Applications

True Unlimited On-Orbit Reconfiguration to Enable “Change-on-the-Fly” Capability in All Orbits Across Space

Complete Solution to “Process and Analyze” for Real Time On-Board Processing including Machine Learning
Thank You