Enabling Product Differentiation in the Digital Consumer Market

Product Differentiation: Separating your product from the competition.
Enhancing Technology: Adding innovation to existing chipset features.
Enabling Technology: Add entirely new features to open new markets.
Based upon both supplier and component criteria, designers choose Xilinx as a preferred vendor for low-power CPLD products. Weighing competitors not only by price, but by reputation of product, delivery, quality, and attention to special needs, Xilinx comes out on top.

According to HTC, the device features were what tipped the scale. Not only did the base power consumption meet or exceed power budgets, but key low-power enhancements played a large role in part selection. “HTC has received a substantial amount of performance capabilities in Xilinx products,” said Peter Chou, HTC’s president. ”Their combination of leading-edge technologies, complete programmable system design, and full technical service support are essential to the success of HTC.”
Why Designers are Using CoolRunner-II CPLDs
The Benefits of Xilinx CoolRunner-II CPLDs

Much more than logic and flip-flops

- **Product Differentiation.** Separating your product from the competition
- **Enhancing technology:** adding an innovation to existing chipset features
- **Enabling technology:** adding entirely new features to open up new markets
- **Increase brand awareness:** give your product something memorable

- **Low Power RealDigital Advantage**
  - DataGATE: lower power; requires no external devices

- **Flexibility**
  - Easily integrate the components that best meet your needs
  - Support modular configurations
  - Easy System Customization

- **Time-to-Market Advantage**
  - Free efficient and proven development tools (WebPACK)
  - Standard off-the-shelf components
  - Free Reference Designs

- **Fully Programmable and Re-Programmable**
  - Reduced exposure to risk, bugs, component shortages, evolving standards
  - Field upgradeable hardware

- **System Cost Management**
  - Logic consolidation: reduce the number of devices in your design

- **Efficient Life-Cycle Product Management**
  - Extremely effective at enabling derivative designs
  - Exploit market opportunities before your competition
  - Expand the market base of your ROI

- **Combine Functionality**
  - Level Shifting and I/O Pin Expansion and Logic Consolidation
  - Keypad scanner and other features in one device
Handsets

Pocket PC Phone

• DataGATE
• Level Shifter
• I²C to GPIO Expansion
• OTF Configuration
• Interrupt Controller
• CF Bus Switch
• Keypad Scanner
• LCD Timing Controller
• Logic Consolidation

DataGATE Blocking

• XAPP395 Using DataGATE in CoolRunner-II CPLDs
• WP227 The Real Value of CoolRunner-II DataGATE
Cell Phone with Camera Zoom

• Focus Control for Stepping Motor.
• Chipset Differentiation.

Pocket PC/Phone

• Keypad Scanner
• Logic Consolidation
Handset Application Note Support

• Free HDL Design Files Accompany Application Notes
• Proven Customer Design Use and Support
• www.xilinx.com/support/library.htm
**Portable Consumer**

**GPS Unit**
- Hard Disk Control
- GPIO Interface
- Timing Controller

**PDA Device**
- SD Card Interface
**Portable Satellite Radio and MP3 Player**

- Microprocessor Bug Fix
- SDRAM Timing Controller

**CoolRunner-II**

**Portable Satellite Radio and MP3 Player**

**Alcohol Analyzer**

- Display Control
- Logic Consolidation

**CoolRunner XPLA3 CPLD Under Piggyback Device**
**Wired Consumer**

**Digital Music Box**

- Port Expander/Interface
- DAC Interface

**Digital Wireless Interface**

- Port Expander/Interface
Photo Printer

• High Speed SRAM Controller
Xilinx CPLDs Offer More for Less

Get More
- Logic
- Features and Performance
- Security
- Flexibility

For Less
- Price
- Board area
- Power
- EMI

The Logic Consolidator demonstrates how Xilinx CPLDs can:
- Reduce component cost and manufacturing cost
- Reduce component count and PC board space
- Decrease time-to-market
- Increase reliability

Documentation
- WP202: The Advantages of Migrating from Discrete Logic Devices to CPLDs (PDF)
- WP214: TTL Burn Rate for Xilinx CPLDs (PDF)

Download the latest version of the CPLD Logic Consolidator now!
Documented Xilinx CPLD Applications

Digital Media Player

- XAPP328 Design of an MP3 Player Using a CoolRunner CPLD

Digital Camera

- XAPP390 Design of a Digital Camera with CoolRunner-II CPLDs
**Memory Control**

**Compact Flash Card Interface and Control**

- XAPP398 Compact Flash Interface for CoolRunner-II CPLDs

**SD Card Interface**

- XAPP906 Interfacing to Secure Digital Cards with CoolRunner-II CPLDs

**SDRAM Controller**

- XAPP384 Interfacing to DDR SDRAM with CoolRunner-II CPLDs
- XAPP394 Interfacing to Mobile SDRAM with CoolRunner-II CPLDs
Display Interface

LED Driver Block

• XAPP805 Driving LEDs with Xilinx CPLDs

![LED Driver Block Diagram]

LCD Module

• XAPP904 CoolRunner-II Character LCD Module Interface

![LCD Module Diagram]
Level Shifting

- XAPP785 Level Translation Using Xilinx CPLDs

Microcontroller Interface

- XAPP393 CoolRunner-II CPLD 8051 Microcontroller Interface

Serial Peripheral Interface Master

- XAPP386 CoolRunner-II Serial Peripheral Interface Master
- XAPP800 Configuring Xilinx FPGAs with SPI Flash Memories Using CoolRunner-II CPLDs
CoolRunner-II Advanced Features

DataGATE
Series switches on the inputs allow decoupling of internal logic from external “don’t care” transitions. Outputs are held at the last valid state when DataGATE is enabled.
- Reduces power consumption by eliminating ‘don’t care’ internal switching
- Supports hot plugging
- Reduces EMI
- Simplifies system debug

Clock Division
- Even/Odd clock generation
- Duty cycle correction
- Multiple clock nets

DualEDGE Flip Flops
Each flip-flop can switch on the rising, falling or both edges of the clock
- Higher-resolution PWM
- Motor control
- LCD contrast
- Power conversion
- Position indication
- Increased timer resolution

Advanced Security
Four levels of design security
- Prevents design theft or accidental overwrite
- Ideal for mobile phones and PDAs and other wireless applications

I/O Banking
Multiple I/O banks, each with independently selectable voltage levels
- System voltage interfacing
- Bridging standards
- Bus multiplexing

500mV Input Hysteresis
- Improved noise immunity
- Reduced power consumption (fewer false transitions)
- Superior signal integrity

In System Programming and On The Fly Reconfiguration
- Reprogram the design post-deployment
- Reprogram the CPLD with a new pattern while the existing pattern is operational
- Multiple design patterns from a single CPLD

CoolRunner-II

DataGATE Decoupling Switch

INPUT PIN

To Internal Logic

DIV2
DIV4
DIV8
DIV16

Global Clock (GCK2)

External Sync Reset

2.5V SRAM

3.3V SRAM

1.5V µP

1.8V I/O

2.5V SRAM

CoolRunner-II

To Internal Logic

Hysteresis Buffer

INPUT PIN

To Internal Logic

CoolRunner-II

To Internal Logic

16
Industry’s Lowest Power CPLDs.

So low-power, CoolRunner-II CPLDs even run on Apples!

- XAPP381 CoolRunner-II Demo Board

CPLD Battery Life Comparison
- CoolRunner-II CPLDs with DataGATE dramatically extends battery life

**CPLD Battery Life Comparison**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Battery Life (Hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoolRunner-II CPLD with DataGATE</td>
<td>1200</td>
</tr>
<tr>
<td>CoolRunner-II 1.8V CPLD</td>
<td>1000</td>
</tr>
<tr>
<td>Brand L 1.8V “zero power” CPLD</td>
<td>800</td>
</tr>
<tr>
<td>Brand L 1.8V CPLD</td>
<td>600</td>
</tr>
<tr>
<td>Brand A 1.8V CPLD</td>
<td>400</td>
</tr>
</tbody>
</table>

**Hours of Dynamic Operation**

*Note*: 256 macrocell devices at 100% duty cycle with 2 AA batteries, populated with 16 bit counters at 20 MHz.
## CoolRunner-II CPLD Selection Guide

<table>
<thead>
<tr>
<th>Device</th>
<th>XC2C32A</th>
<th>XC2C64A</th>
<th>XC2C128</th>
<th>XC2C256</th>
<th>XC2C384</th>
<th>XC2C512</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>750</td>
<td>1500</td>
<td>3000</td>
<td>6000</td>
<td>9000</td>
<td>12000</td>
</tr>
<tr>
<td>Macrocells</td>
<td>32</td>
<td>64</td>
<td>128</td>
<td>256</td>
<td>384</td>
<td>512</td>
</tr>
<tr>
<td>Product Terms per Macrocell</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
</tr>
<tr>
<td>Maximum I/O</td>
<td>33</td>
<td>64</td>
<td>100</td>
<td>184</td>
<td>240</td>
<td>270</td>
</tr>
<tr>
<td>Minimum Pin-to-Pin Logic Delay (ns)</td>
<td>3.8</td>
<td>4.6</td>
<td>5.7</td>
<td>5.7</td>
<td>7.1</td>
<td>7.1</td>
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<tr>
<td>DualEDGE Registers</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input Hysteresis</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>DataGATE and Clock Divide</td>
<td>—</td>
<td>—</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Global Clocks</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
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<tr>
<td>Product Term Clocks per Function Block</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

### Packages

<table>
<thead>
<tr>
<th>Packages</th>
<th>Size</th>
<th>Maximum User I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFG32</td>
<td>5x5 mm</td>
<td>21</td>
</tr>
<tr>
<td>VQ44</td>
<td>12x12 mm</td>
<td>33</td>
</tr>
<tr>
<td>PC44</td>
<td>17.5x17.5 mm</td>
<td>33</td>
</tr>
<tr>
<td>QFG48</td>
<td>7x7 mm</td>
<td>37</td>
</tr>
<tr>
<td>CP56</td>
<td>6x6 mm</td>
<td>45</td>
</tr>
<tr>
<td>VQ100</td>
<td>16x16 mm</td>
<td>64</td>
</tr>
<tr>
<td>CP132</td>
<td>8x8 mm</td>
<td>100</td>
</tr>
<tr>
<td>TQ144</td>
<td>22x22 mm</td>
<td>100</td>
</tr>
<tr>
<td>PQ208</td>
<td>30.6x30.6 mm</td>
<td>173</td>
</tr>
<tr>
<td>FT256</td>
<td>17x17 mm</td>
<td>184</td>
</tr>
<tr>
<td>FG324</td>
<td>23x23 mm</td>
<td>240</td>
</tr>
</tbody>
</table>

### Low-cost Small Form-Factor Packaging

- **Package Type:** QFG32, CP56, QFG48, CP132, FT256
- **Dimensions:** 5x5mm, 6x6mm, 7x7mm, 8x8mm, 17x17mm
- **Board Area:** 25mm², 36mm², 49mm², 64mm², 289mm²
- **Max. I/O:** 21, 45, 37, 106, 212
Take the Next Step

The Xilinx CPLD Design Kit contains everything you need to design and debug your next CPLD design, including:

- ISE WebPACK software
- Prototype board with pre-programmed CoolRunner-II and XC9500XL CPLDs
- Download cable
- Training material
- Resource CD

www.xilinx.com

Design Faster with CoolRunner Reference Designs.

Xilinx CPLD reference designs make designing much easier than with other solutions. These drop-in, ready-to-use functions are comprised of HDL design code and application notes that allow to finish your design faster. You can also increase product flexibility and user advantages with our comprehensive reference designs.

www.xilinx.com/cpld/ref-designs

CPLD QuickStart Applications.

Xilinx CoolRunner-II CPLDs are shown in a wide range of design examples, with presentations and demonstrations to show how you can complete your design faster, with lower power and lower cost.

www.xilinx.com/cpld/quickstart