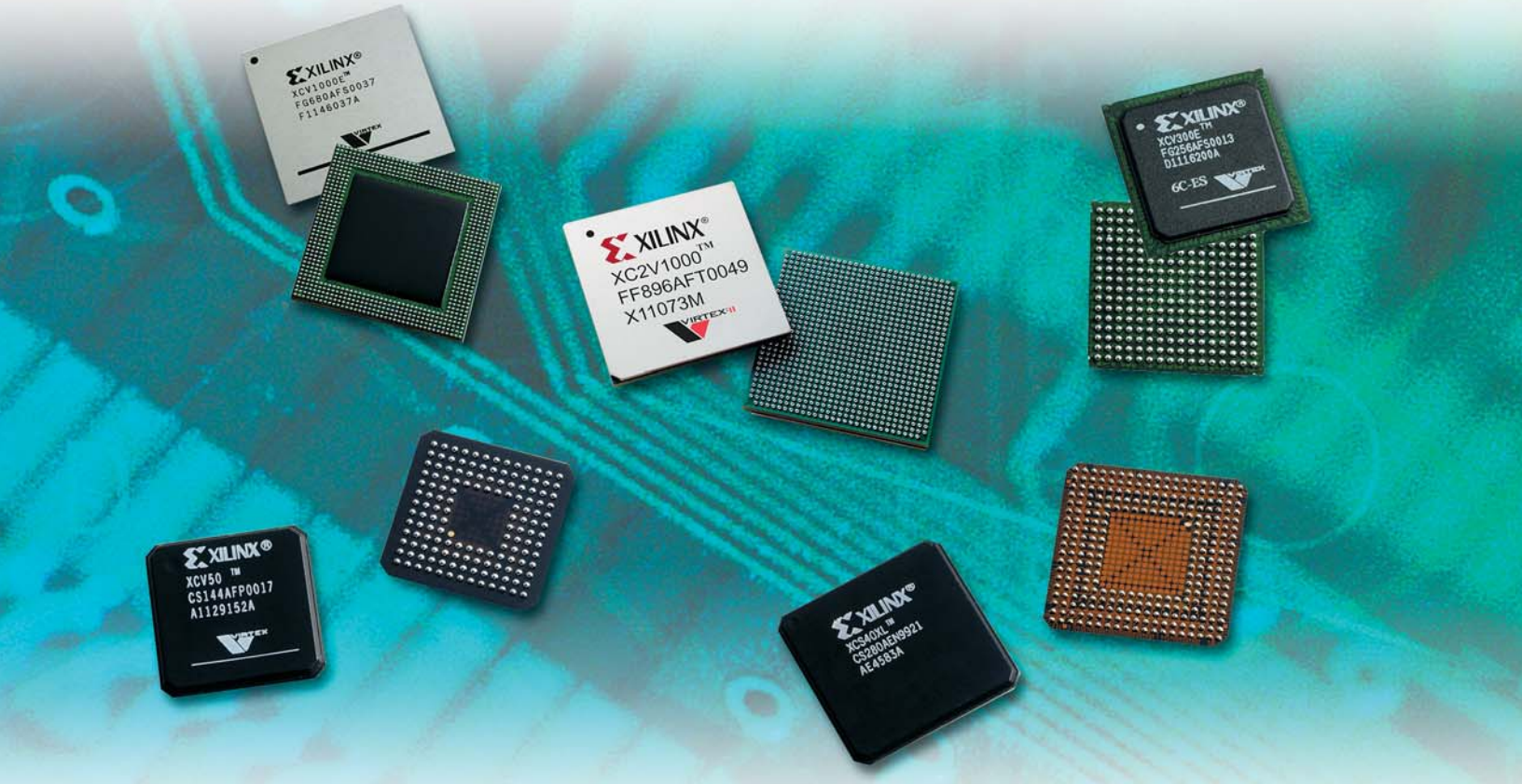
Xilinx Advanced Packaging

Chip Scale Packages/Quad Flat No-Lead/Plastic BGAs/ Cavity-Down BGAs/Flip-Chip BGAs/Flip-Chip CCGAs/Pb-Free



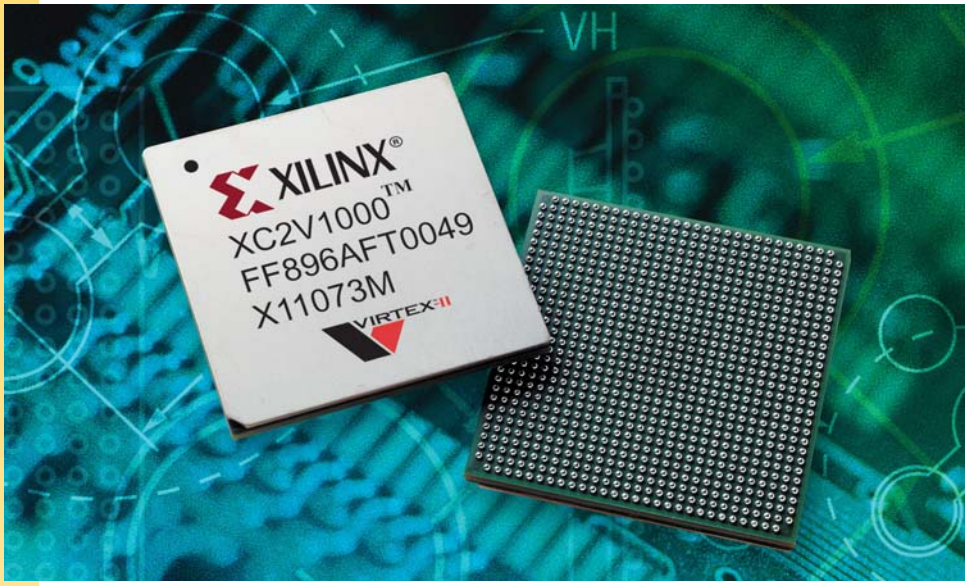
Now Offering Green Packaging Solutions

Earth Friendly

Xilinx Advanced Packaging

Electronic packages are the interconnect housings for semiconductor devices. They provide electrical interconnections between the IC and the board, and they efficiently remove the heat generated by the device.

Device feature sizes are constantly shrinking, resulting in an increased number of available transistors. Today's submicron technology is also enabling large scale functional integration, moving toward system on-a-chip-solutions. To keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance. In addition, electronic packages must address the high pin counts, reduced pitch, and form factor requirements that today's advanced applications demand. At the same time, packages must be reliable and cost effective.



Packaging Technology at Xilinx

At Xilinx, a wide range of leaded as well as array packages have been developed to meet the design and performance requirements of today's advanced IC devices. Xilinx advanced package offerings, such as standard overmolded PBGAs, thermally enhanced Cavity-down BGAs, high performance Flip-Chip BGAs and Flip-Chip CCGAs, Quad Flat No-Lead packages, and small form factor CSPs (Chip Scale Packages) are offered to address various pin counts and density requirements, while offering superior electrical performance as compared to their leaded counterparts. Pb-free packages are also available.

"Green" Packaging Solutions from Xilinx

Xilinx has also developed packaging solutions that are safer for the environment. Today, standard packages from Xilinx do not contain substances that have been identified as harmful to the environment including cadmium, hexvalent chromium, mercury, PBB, and PBDE. Pb-free solutions take that one step further and also do not contain lead (Pb). This makes Pb-free solutions from Xilinx RoHS (Reduction of Hazardous Substances) compliant. Xilinx refers to these products as "green". Pb-free packages from Xilinx are also JEDEC STD-20 compliant meaning that the packages have been made to be more robust so they are capable of withstanding higher reflow temperatures. Xilinx is now ready to support the industry requirements for Pb-free packaging solutions.

For more information on Xilinx packaging, refer to **xilinx.com/packaging**.

Pb-Free Packages

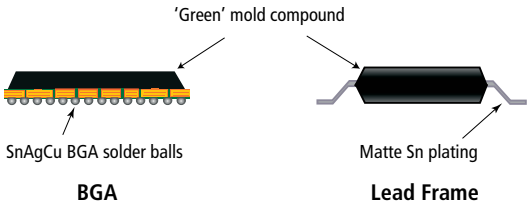
Xilinx proactively worked with suppliers, customers, and industry consortia to develop and qualify suitable material sets and processes for Pb-free applications. The Xilinx Pb-free initiative was driven in response to legislative mandates banning Pb from electronic products and to meet the growing needs of our valued customers to supply environmentally friendly products.

Xilinx sources the best material sets for Pb-free applications. Material sets are reliable, environmentally friendly, and robust to meet the requirement of the higher reflow temperature (245° – 260° C). The mold compound used for Pb-free packages is "green" meaning they are free of bromine and antimony substances and comply with the RoHS Directive which bans Pb, mercury, cadmuim, hexvalent chromium, and PBDE and PBB flame retardants.

Features

- RoHS compliant
- MSL3 Classification
- Compliant to JEDEC-J-020 standard for peak reflow temperature (245°C– 260°C)
- Packages marked with Pb-free identifier
- Lead frame packages are compatible with Sn/Pb soldering process

Package Construction



Package Offering

Pb-free solutions will be available for all current packages. Contact your Xilinx sales representative for specific availability.

Part Number

Pb-free products are differentiated from standard products by the package code. A "G" character is added after the package designator and before the pin count on all Pb-free packages.

Thermal Performance

Thermal performance for Pb-free packaging is equivalent to that for standard (non Pb-free) packages. Refer to the thermal performance information specified on specific packages in this brochure.

Reliability

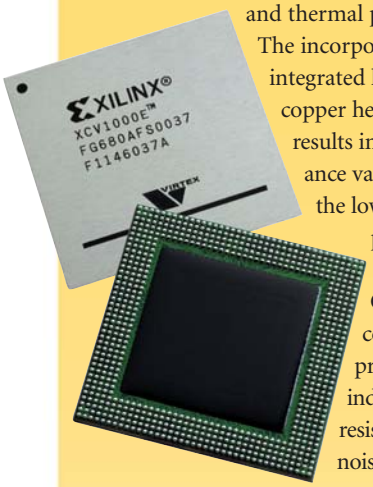
Temperature Cycles (-55°C – 125°C)	⩾1000 Cycles
THB	85°C/85 R.H., Biased, 1000 hrs
Unbiased 85/85	85°C/85 R.H., 1000 hrs
Moisture Sensitivity Level	3 (4 for flip-chip BGAs)

Pb-free Materials

Plating (lead-frame packages)	100% Matte Sn
Solder Balls (BGAs)	SnAgCu

Cavity-Down BGA

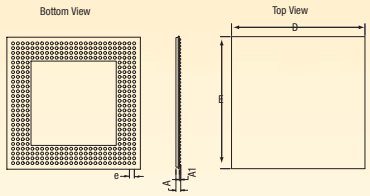
Cavity-down BGAs are high performance packages that offer superior electrical and thermal performance. The incorporation of the integrated high conductivity copper heat spreader results in thermal resistance values that are the lowest among the packages offered by Xilinx. Optimized construction also provides low inductance, low resistance, low noise performance.



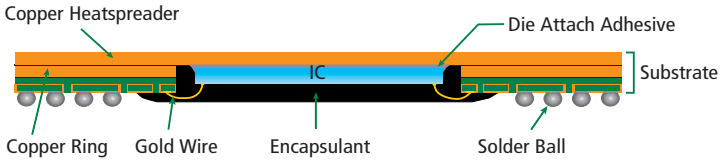
Xilinx cavity-down BGAs are available in two different ball pitches (1.27 mm and 1.00 mm) and are in standard JEDEC body sizes. This packaging technology uses established materials and processes to ensure reliable performance. All cavity-down BGA packages are qualified for JEDEC Level 3 moisture sensitivity level.

Features

- Superior electrical performance
- Lowest thermal resistance (θ_{JA}<15°C/W)
- Low profile and light weight
- Fine pad pitch support (to 54 microns)
- Passes JEDEC Level 3
- Available in 1.27 mm pitch and 1.00 mm pitch
- Uses established materials and processes
- Excellent board level reliability



Package Construction



Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
BG 352	35x35	1.27	0.6	1.40
BG 432	40x40	1.27	0.6	1.40
BG 560	42.5x42.5	1.27	0.6	1.38
FG 680	40x40	1.00	0.5	1.60
FG 860	42.5x42.5	1.00	0.5	1.95

Thermal Performance

Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
BG 352	35x35	12.5	4L/2P - SMT
BG 432	40x40	11.4	4L/2P - SMT
BG 560	42.5x42.5	11.0	Estimated
FG 680	40x40	11.0	4L/2P - SMT
FG 860	42.5x42.5	10.5	4L/2P - SMT

Reliability

Temperature Cycles	-55°/+125°C, 1000 cycles
Pressure Pot	96 hrs/121°C/2 Atm
Temperature/Humidity	85°C/85% RH, 1000 hrs
Moisture Sensitivity	JEDEC Level 3

Standard Materials

Substrate	BT
Die Attach	Silver Filled Epoxy
Bond Wires	0.9-1.3 mils Gold
Encapsulant	Liquid Encapsulant
Heat Sink	Copper
Solder Balls (Standard)	Eutectic Sn/Pb
Solder Balls (Pb-free)	SnAgCu

Chip Scale Packages

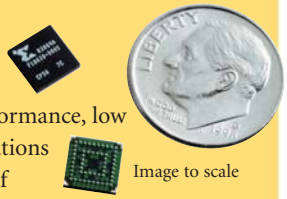


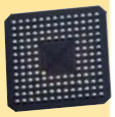
Image to scale

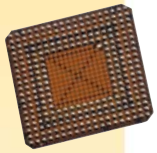
Xilinx Chip Scale Packages (CSP) are perfect for high performance, low cost portable applications where real estate is of utmost importance, miniaturization is key, and power consumption is low. The Xilinx line of CSP packages include both the flex-based substrate as well as rigid BT-based substrate with 0.5 mm and 0.8 mm ball pitch. The wire bonded interconnection and die-up configuration with an overmolded body indicate the use of mature and advanced assembly processes and material sets. This configuration also makes the package immune to die shrink, therefore, avoiding retooling costs.

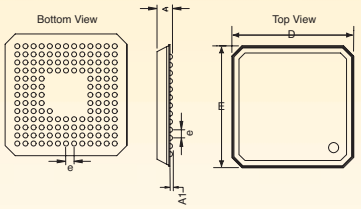
With a small form factor and high I/O counts, Xilinx CSP packages are the ultimate solution for portable applications, such as wireless, notebook, telecom, and cellular systems.

Features

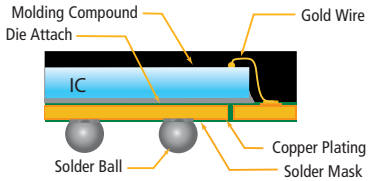
- Low package height
- Small form factor and light weight
- Good immunity to die shrink
- 0.5 mm and 0.8 mm ball pitch
- 6 x 6 to 17 x 17 mm body size
- Uses mature assembly processes and material sets
- Single metal flex substrate and two metal BT substrates



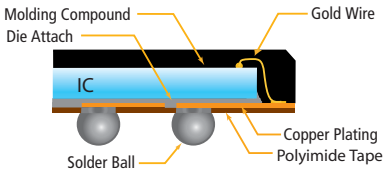




Package Construction



BT - Based CSP



Flex - Based CSP

Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
CP 56	6x6	0.5	0.2	1.35
CP 132	8x8	0.5	0.2	1.00
CS 48	7x7	0.8	0.4	1.50
CS 144	12x12	0.8	0.4	1.20
CS 280	16x16	0.8	0.4	1.20
FS 48	6x8	0.8	0.3	1.20
FT 256	17x17	1.0	0.4	1.40

Thermal Performance

Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
CP 56	6x6	65	Estimated
CP 132	8x8	67.2	4L/2P – SMT
CS 48	7x7	45	Estimated
CS 144	12x12	34	4L/2P - SMT
CS 280	16x16	31	Estimated
FS 48	8x9	60.1	Estimated
FT 256	17x17	31.0	4L/2P – SMT

Reliability

Temperature Cycles	-55°/+125°C, 1000 cycles
Temperature/Humidity	85°C/85% RH, 1000 hrs
Pressure Pot	96 hrs/121°C/2 Atm
Moisture Sensitivity	JEDEC Level 3

Standard Materials

Substrate	BT/Polyimide (flex based)
Die Attach	Silver Filled Epoxy
Bond Wires	1.0-1.2 mil Gold
Mold Compound	Epoxy Novolac
Solder Balls (Standard)	Eutectic Sn/Pb
Solder Balls (Pb-free)	SnAgCu

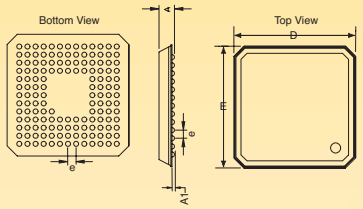
Quad Flat No-Lead Packages

Xilinx Flat No-Lead (QFN) package is a robust and low profile leadframe based plastic package that has several advantages over traditional leadframe packages. The exposed die attach paddle enables efficient thermal dissipation when directly soldered to the PCB. Additionally, this near chip scale package offers improved electrical performance, smaller package size, and an absence of external leads. Since the package has no external leads, coplanarity and bent leads are no longer a concern.

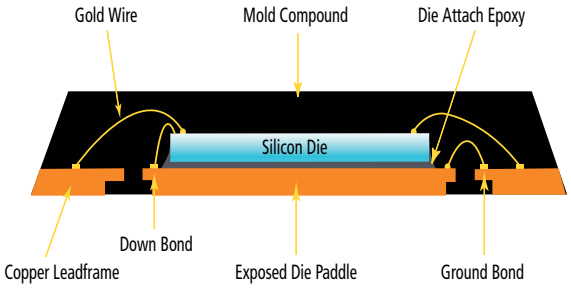
Xilinx QuadFlat No-Lead packages are ideal for portable applications where size, weight, and performance matter.

Features

- Small size and light weight
- Excellent thermal and electrical performance
- Compatible with conventional SMT process
- Less than 1.0 mm package height



Package Construction



Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
QF 32	5x5	0.50	0.02	0.90
QF 48	7x7	0.50	0.02	0.90

Thermal Performance

Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
QF 32	5x5	35.5	Estimated
QF 48	7x7	31.2	Estimated

Reliability

Temperature Cycles (-55°C – 125°C)	≥ 1000 Cycles
THB	85°C/85% RH, Biased, 1000 hrs
Unbiased 85/85	85°C/85% RH, 1000 hrs
Moisture Sensitivity	JEDEC Level 3

Standard Materials

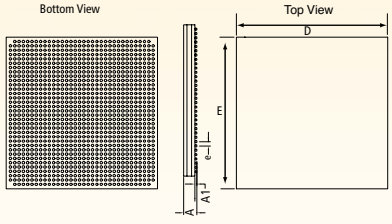
Leadframe Substrate	Copper
Die Attach Epoxy	Silver Epoxy
Bond Wires	1.0 mil Gold
Mold Compound	Epoxy Novolac
Plating (Standard)	100% Matte Sn (Pb-free)

Plastic Overmolded BGAs

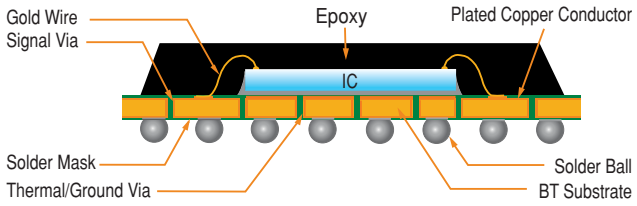
Ball Grid Array (BGA) is a plastic packaging technology that uses area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably as compared to leaded products. Xilinx BGAs are assembled with high-quality materials and use mature processes for high performance and reliability. The substrate is a multilayer BT epoxy-based material with signal, power, and ground planes. This configuration provides enhanced electrical and thermal performance. The package is offered in an overmolded die-up format with a ball pitch of 1.27 mm and 1.00 mm (fine pitch). The fine-pitch option provides a significantly increased number of I/Os.

Features

- Improved electrical performance (short wire length)
- Enhanced thermal performance
- Fine die pad pitch support (to 54 microns)
- Multilayer with ground and power planes
- High board assembly yield/SMT compatible
- Low profile and small footprint



Package Construction



Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
BG 225	27x27	1.50	0.5	2.15
BG 256	27x27	1.27	0.5	2.30
BG 492	35x35	1.27	0.6	2.55
BG 575	31x31	1.27	0.6	2.33
BG 728	35x35	1.27	0.6	2.33
FG 256	17x17	1.00	0.5	1.73
FG 320	19x19	1.00	0.5	2.00
FG 324	23x23	1.00	0.5	2.25
FG 456	23x23	1.00	0.5	2.20
FG 676	27x27	1.00	0.5	2.25
FG 900	31x31	1.00	0.5	2.25
FG 1156	35x35	1.00	0.5	2.33

Thermal Performance

Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
BG 225	27x27	30	4L/2P - SMT
BG 256	27x27	27	4L/2P - SMT
BG 492	35x35	17	4L/2P - SMT
BG 575	31x31	14.4	Estimated
BG 728	35x35	14.1	Estimated
FG 256	17x17	25.9	4L/2P – SMT
FG 320	19x19	30	Estimated
FG 324	23x23	32.5	4L/2P – SMT
FG 456	23x23	19	4L/2P – SMT
FG 676	27x27	17	4L/2P – SMT
FG 900	31x31	14	4L/2P – SMT
FG 1156	35x35	13	Estimated

Reliability

Temperature Cycles	-55°/+125°C, 1000 cycles
HAST	100 hrs/130°C/3 Atm
Pressure Pot	96 hrs/121°C/2 Atm
Moisture Sensitivity	JEDEC Level 3

Standard Materials

Substrate	BT
Die Attach	Silver Filled Epoxy
Bond Wires	0.9-1.5 mils Gold
Mold Compound	Epoxy Novolac
Solder Balls (Standard)	Eutectic Sn/Pb
Solder Balls (Pb-free)	SnAgCu

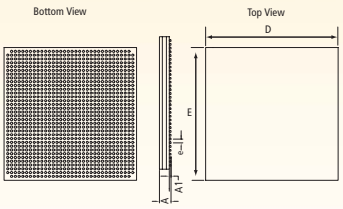
Flip-Chip BGAs

Flip-chip is a packaging interconnect technology that replaces peripheral bond pads of the traditional wire bond interconnect technology, with area array interconnect at the die/substrate interface. Unlike traditional packaging, in which the die is attached to the substrate face up and the connection is made by using wire, the solder bumped die in a flip-chip package is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

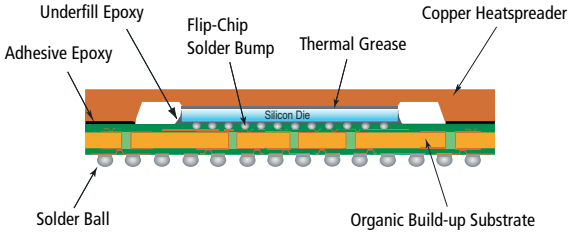
Xilinx Flip-Chip Packages are assembled on high-density, multi-layer organic laminate substrates. Since the flip-chip bump pads are in area array configuration, very fine lines and geometry on the substrates are required to successfully route the signals from the die to the periphery of the substrates. Multi-layer build up structures offer this layout flexibility on flip-chip packages as well as providing improvements in power distribution and signal transmission characteristics. This packaging technology is used exclusively for Xilinx high performance, high pin count FPGA products.

Advantages of Flip-Chip Interconnect

- Easy access to core power/ground and shorter interconnect, resulting in better electrical performance
- Elimination of wire bond results in lower inductance, for better noise control
- Excellent thermal performance (direct heatsinking to backside of the die)
- Higher I/O density because bond pads are in area array-format



Package Construction



Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
BF 957	40x40	1.27	0.60	3.25
FF 668/672	27x27	1.00	0.50	2.65
FF 896	31x31	1.00	0.50	3.20
FF 1148/1152	35x35	1.00	0.50	3.20
FF 1513/1517	40x40	1.00	0.50	3.20
FF 1696/1704	42.5x42.5	1.00	0.50	3.20
SF 363	17x17	0.80	0.40	1.89

Thermal Performance

Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
BF 957	40x40	10.9	JESD - 2S/2P
FF 672	27x27	14.6	JESD - 2S/2P
FF 896	31x31	11.7	JESD - 2S/2P
FF 1152	35x35	11.0	JESD - 2S/2P
FF 1517	40x40	11.1	JESD - 2S/2P
FF 1704	42.5x42.5	8.0	JESD - 2S/2P

Reliability

Temperature Cycles (-40° C - 125° C)	1000 Cycles
THB	85°C/85 RH, biased, 1000 hrs
Unbiased 85/85	85°C/85 RH, 1000 hrs
Moisture Sensitivity	JEDEC Level 4

Standard Materials

Substrate	Multi-layer Organic Laminate
Heatspreader	Copper
Flip-Chip Bumps	Eutectic Sn/Pb
Solder Balls	Eutectic Sn/Pb
Thermal Die Attach	Thermal Grease

Note: Pb-free solution in development

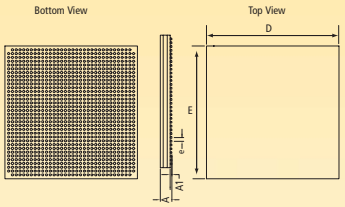
Flip-Chip CCGA Package

Ceramic Column Grid Array (CCGA) package is a surface mount compatible package that uses high temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. This package is assembled with a high density, multilayer ceramic substrate. When combined with flip-chip interconnects, this packaging technology offers a high-density, higher pin count, and reliable package solution.

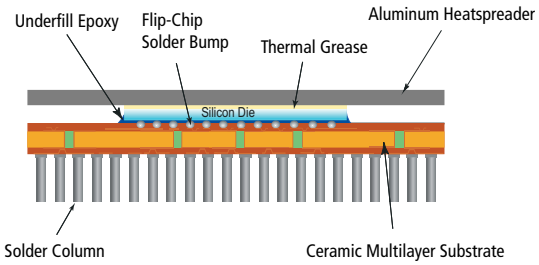
Xilinx flip-chip CCGA package is best suited for applications that require high performance and high reliability. The CF 1144 is the first introduced flip-chip CCGA package.

Features

- Excellent package and solder joint reliability
- Excellent thermal/electrical performance
- JEDEC Level 1 Moisture Sensitivity



Package Construction



Package Offering

Package Code	Body Size D&E (mm)	Ball Pitch e(mm)	Stand off A1 (mm)	Package Height A (mm)
CF 1144	35x35	1.00	2.20	6.65

Thermal Performance

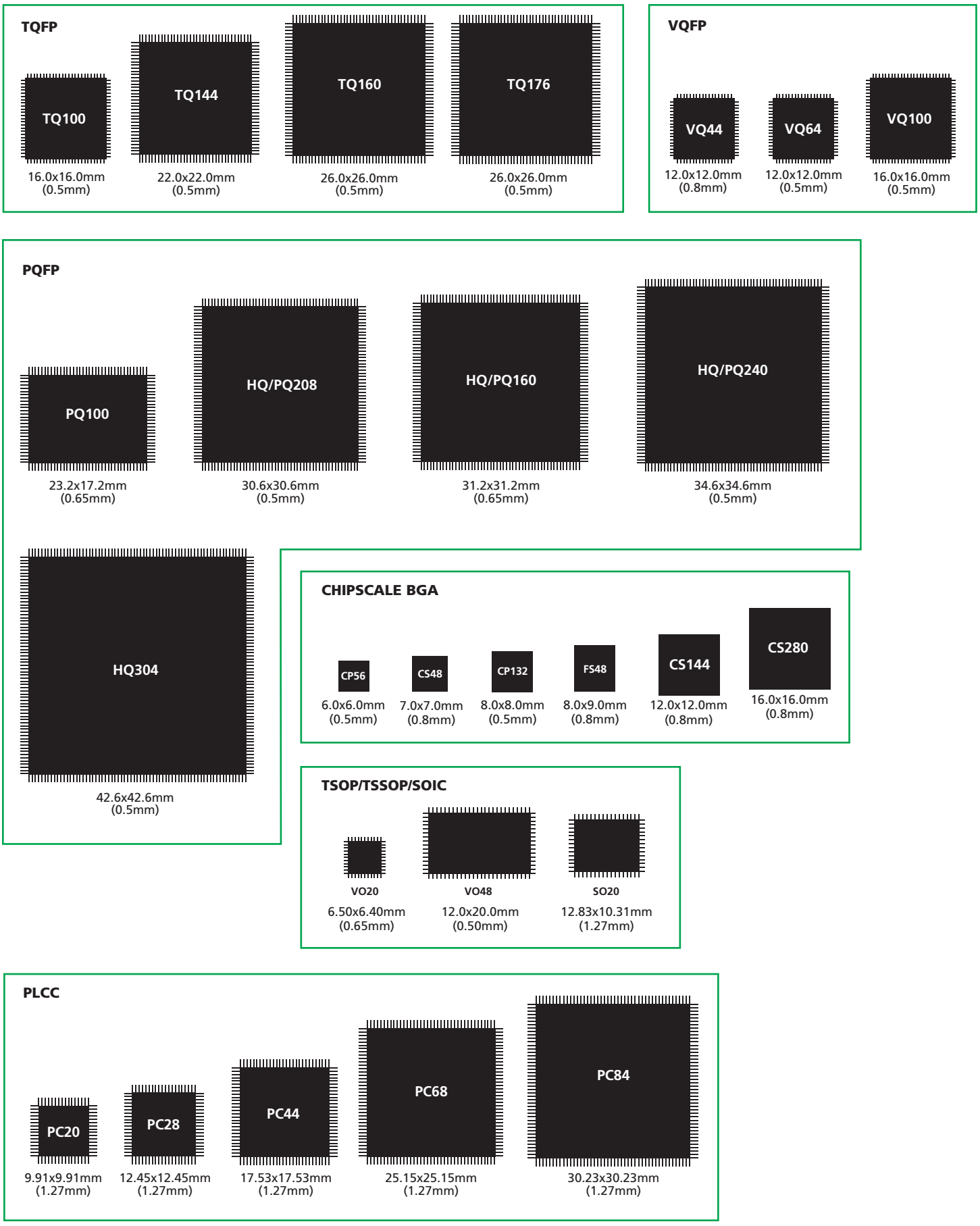
Package Code	Body Size (mm)	θ_{JA} (C/W) Still Air	Comments
CF 1144	35x35	36.0	Estimated

Reliability

Temperature Cycles (-55° C -125° C)	≥1000 Cycles
Unbiased 85/85	85°C/85 RH, 1000 hrs
Moisture Sensitivity	JEDEC Level 1

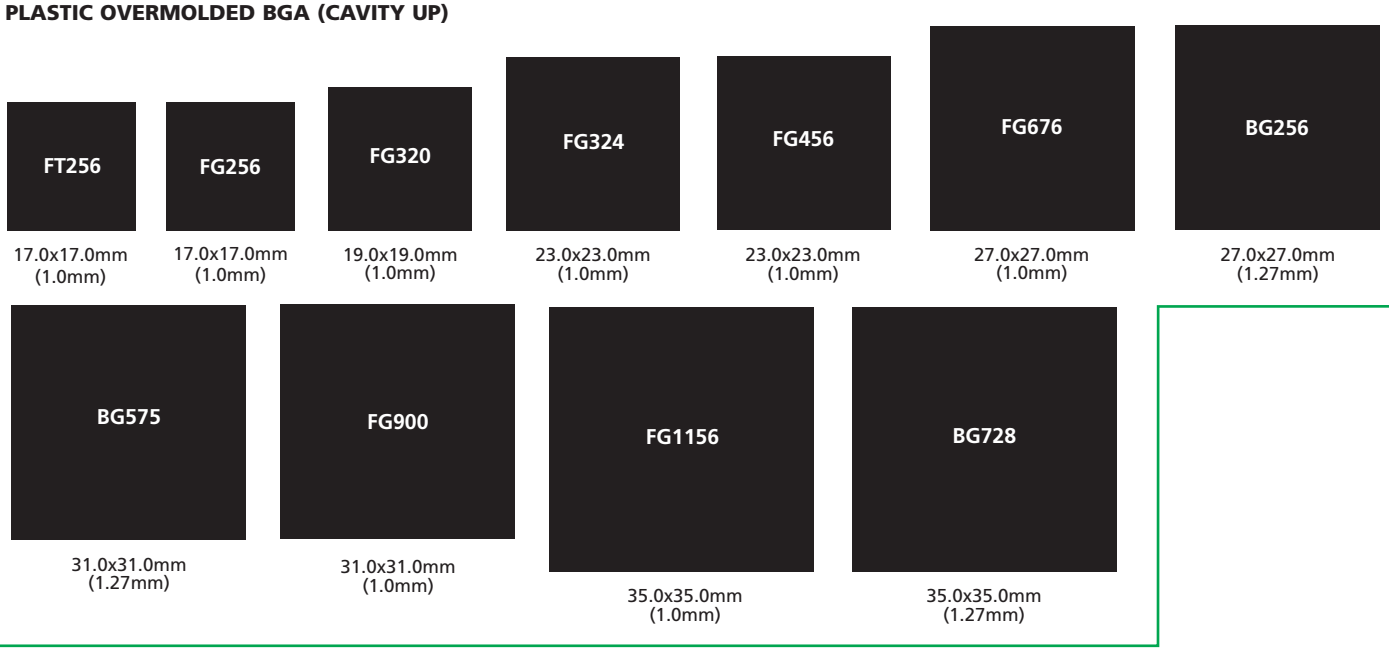
Standard Materials

Substrate	Multi-layer Cermaic
Heatspreader	Aluminum Plate
Flip-Chip Solder Bumps	95Pb5Sn
Solder Columns	90Pb10Sn
Adhesive	Epoxy



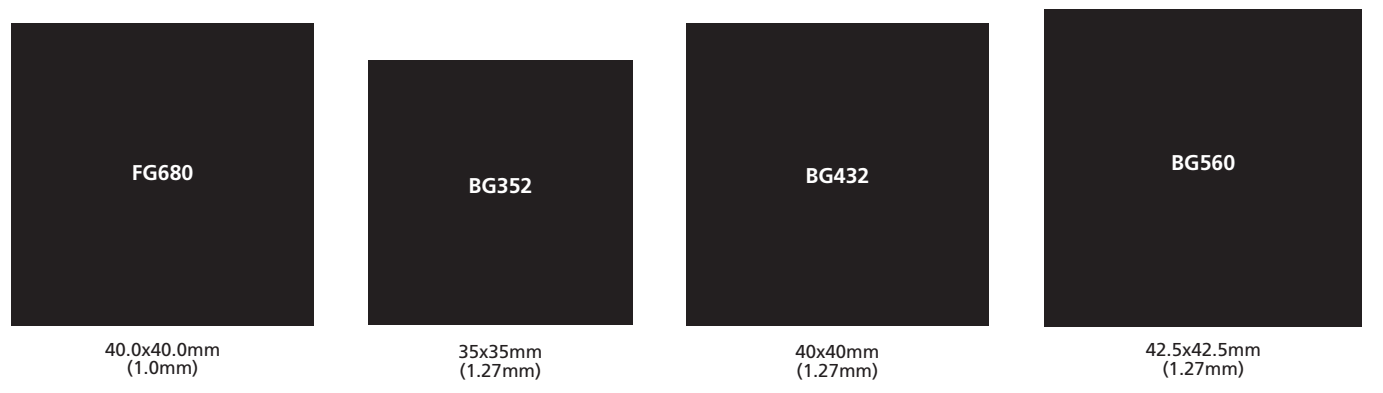
Note: 1. Package outlines shown are actual size.
2. For lead-frame packages, dimensions (D & E) shown are inclusive of leads. Dimensions in parenthesis represent package pitch.
3. The dimensions of the Pb-free package is identical to the standard package version.

PLASTIC OVERMOLDED BGA (CAVITY UP)



FLIP-CHIP BGA

METAL BGA (CAVITY DOWN)



Note: 1. Package outlines shown are actual size.
2. Dimesions referenced in parenthesis represent package pitch.

Recommended PCB Design Rules

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of your board layout so you can design the board pads to match the component-side land geometry. The typical values of these land pads are described in Figure 1 and summarized in Table 1.

For Xilinx BGA packages, NSMD (Non Solder Mask Defined) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 1. The space between the NSMD pad and the solder mask, and the actual signal trace widths depends on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller

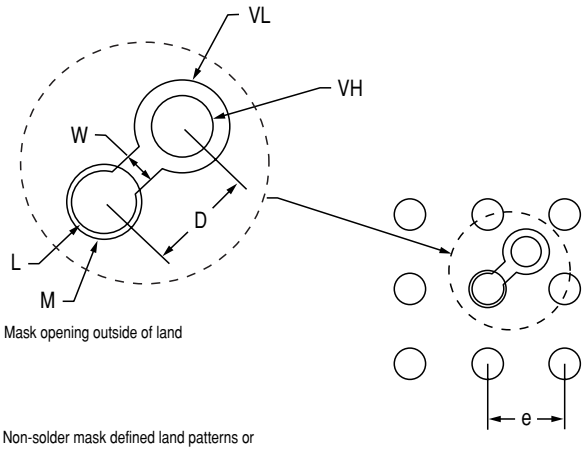


Figure 1: Suggested board layout of soldered pads[1]

Table 1

(Dimensions in millimeters.)	FG256	FG456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Component Land Pad Diameter(SMD)[2]	0.45	0.45	0.45	0.50	0.50	0.45	0.45	0.58	0.58	0.58
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.50	0.50	0.50
Opening in Solder Mask (M) Diameter	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.60	0.60	0.60
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole(VH), Diameter	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Pad Array	Full	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34	30 x 30	34 x 34	39 x 39
Periphery Rows	-	7[3]	-	5	6	-	-	-	-	-

	BG225	BG256	BG352	BG432	BG560	BG575	BG728	BF957	CS144	CP56
Component Land Pad Diameter(SMD)[2]	0.63	0.63	0.63	0.63	0.63	0.61	0.61	0.61	0.35	0.30
Solder Land (L) Diameter(NSMD)	0.58	0.58	0.58	0.58	0.58	0.56	0.56	0.56	0.33	0.27
Opening in Solder Mask (M) Diameter	0.68	0.68	0.68	0.68	0.68	0.66	0.66	0.66	0.44	0.35
Solder (Ball) Land Pitch (e)	1.50	1.27	1.27	1.27	1.27	1.27	1.27	1.27	0.80	0.50
Line Width Between Via and Land (w)	0.300	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.13	0.13
Distance Between Via and Land (D)	1.06	0.90	0.90	0.90	0.90	0.90	0.90	0.90	0.56	-
Via Land (VL) Diameter	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.51	0.51
Through Hole(VH) Diameter	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.250	0.250
Pad Array	Full	-	-	-	-	Full	Full	Full	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	24 x 24	27 x 27	31 x 31	13 x 13	10 x 10
Periphery Rows	-	4	4	4	5				4	1

Notes

1 3 x 3 matrix for illustration only, one land pad shown with via connection.

2 Component land pad diameter refers to the pad opening on the component side (solder mask defined).

3 FG456 package has solder balls in the center in addition to periphery rows of balls.

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