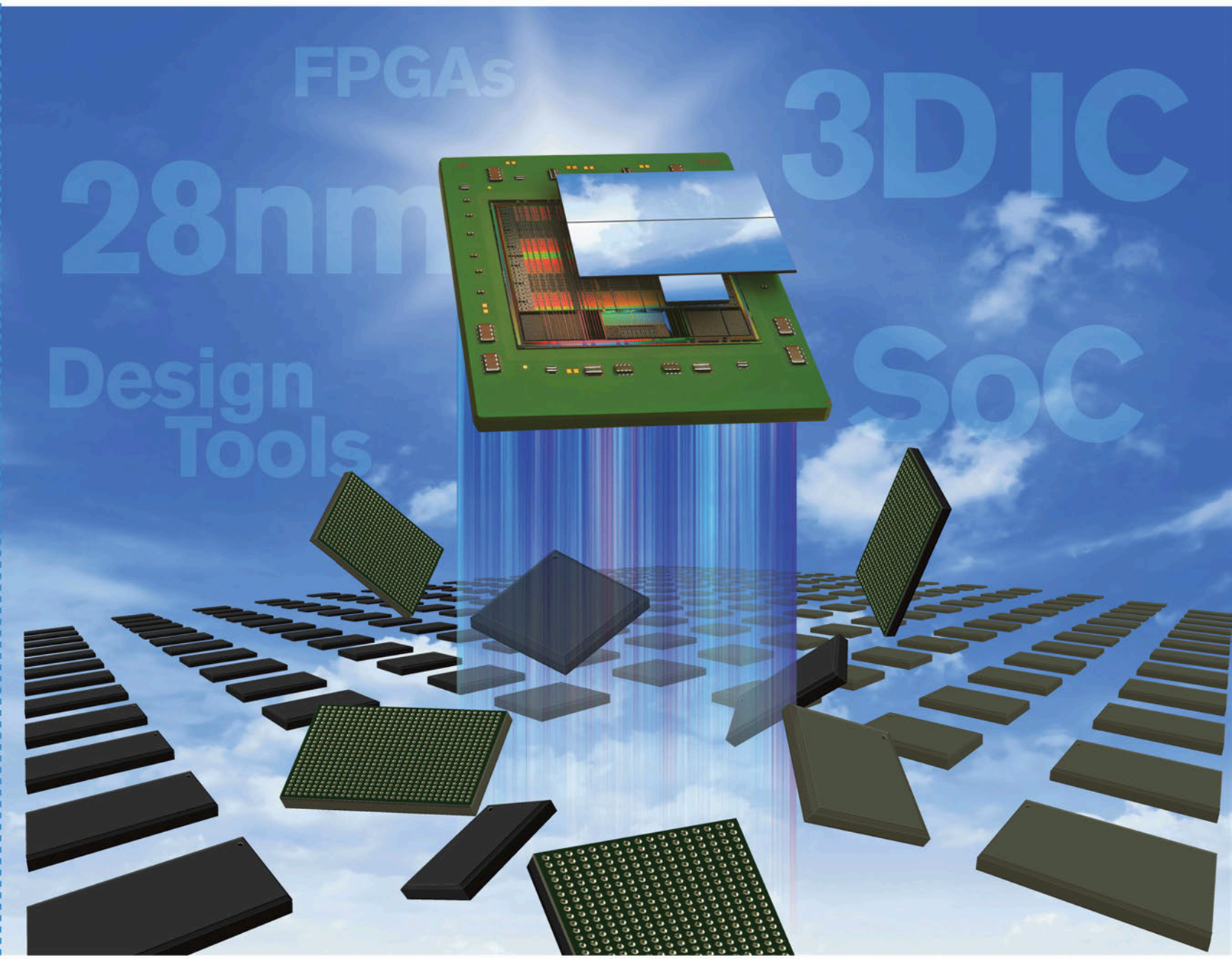
ABSOLUTE QUALITY

Unleashing the Possible



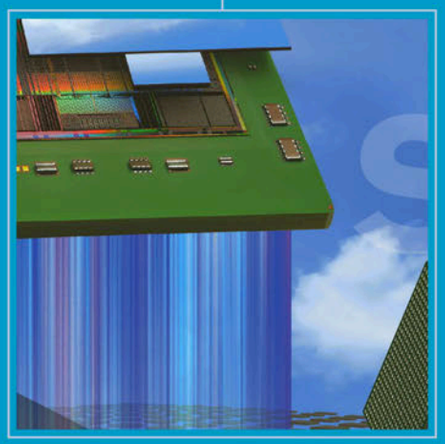
ANNUAL QUALITY REPORT

MARCH 2013

XILINX

ALL PROGRAMMABLE™

ABOUT OUR COVER DESIGN



FOR XILINX, THIS YEAR WAS ALL ABOUT BREAKTHROUGHS. BY SHATTERING RESTRICTIONS INHERENT WITH ASICs AND ASSPs, XILINX LEFT THE COMPETITION BEHIND AND DELIVERED ON THE PROMISE OF OUR ALL PROGRAMMABLE VISION. THE ABSOLUTE QUALITY OF THE NEW PORTFOLIO UNLEASHES THE POSSIBLE, AND ENABLES OUR CUSTOMERS TO MOVE THEIR PRODUCTS A GENERATION AHEAD.

THIS YEAR'S REPORT SHOWCASES SEVERAL OF THE GLOBAL XILINX ENGINEERING TEAMS. THEIR COLLECTIVE AND COORDINATED EFFORTS, AND COLLABORATIONS WITH XILINX CUSTOMERS AND PARTNERS, ARE RESPONSIBLE FOR THE MANY MILESTONES SUCCESSFULLY REACHED AT 28NM.

ABSOLUTE QUALITY defines the Xilinx commitment to excellence. This year, we have delivered on this commitment with the rollout of our 28nm portfolio. It took more than five years, almost a half-billion dollars, and the unwavering focus of our engineering teams—a level of effort that allowed us to be first at 28nm, first with heterogeneous 3D ICs, and first with All Programmable SoCs.

The investments, engineering innovation, and collaborations that led to these successes were unprecedented, and we are extremely pleased with the results. By going "all in" on our All Programmable vision and meeting the most stringent release criteria to date, our products moved a generation ahead of the competition.

This year's Quality Report explains our results in terms of:

- **28nm EXECUTION,** based on our HPL process, third-generation new product introduction (NPI) criteria, and advanced wafer-level reliability
- **3D Packaging INNOVATION,** including stacked-silicon interconnect technology that breaks through Moore's Law and advanced test and manufacturing methodologies for known-good die selection
- **SoC INTEGRATION,** for simplifying SoC solutions and elevating quality at the system level
- **Design Tools PRODUCTIVITY,** which pushes ease of use to new levels with proven design methodologies, predictable QoR, and significantly improved user experiences
- **Quality that BUILDS TRUST,** with knowledge sharing that drives quality for our suppliers, partners, and customers, driving success throughout the All Programmable ecosystem
- **20nm LEADERSHIP,** which extends Xilinx momentum to future generations of All Programmable devices and promotes growth of Xilinx within the industry

These are exciting times—our vision is coming to life and benefiting next-generation systems. Xilinx has forged alternatives to ASICs and ASSPs that are changing the way engineers approach challenges in technology-dependent fields. With absolute quality at 28nm and beyond, Xilinx All Programmable devices and design methodologies are enabling unprecedented customer innovation with shorter time to market and lower costs.

With confidence and pride,

Moshe Gavrielov
President & CEO
Xilinx, Inc.

Vincent Tong
Senior Vice President, Quality & New Product Introductions
Xilinx, Inc.
Board of Directors, Global Semiconductor Alliance

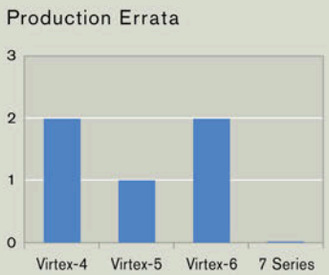
Xilinx Milestones

- First to go "all in" at 28nm on HPL
- "Zero-defect" mindset extended beyond silicon to design tools and IP
- First to production for 28nm, with flawless results
- Third-generation new product introduction, enabling 15 new products to launch in less than six months
- First to deliver a rearchitected, SoC-strength development environment and tool suite
- Zero production errata on the 7 series

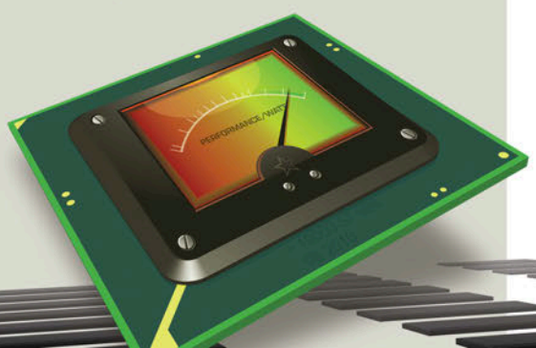
28nm EXECUTION

NUMBERS TELL THE STORY. The results are in and have ended all debate. Xilinx is a generation ahead at 28nm. The company embraced a hallmark zero-defect mentality, going "all in" on the HPL process and one foundry partner. The Xilinx focus on quality and reliability—which spans design, process development, assembly, and test—was guided by third-generation new product introduction (NPI) processes and the most stringent release criteria to date.

28nm Execution Proof Points: Zero Production Errata



- 100% of goals met at each release milestone, with very aggressive specifications
- Stable process, with excellent yield, quality, and reliability, and zero production errata
- Earlier first silicon compared with prior generation, 12 months from samples to production
- Scalable optimized architecture, for rapid rollouts: Virtex® released a week after Kintex™; Artix™ taped out three months ahead of plan
- 50x more samples for verification and characterization compared with previous generation
- Lifetime goals met: 10 years @ 100°C Tj, or 20 years @ 85°C Tj
- Yield ahead of road map for more than one year



HPL Wins

Success starts with strong foundational disciplines. At 28nm, this meant starting by matching the available processes with the technologies Xilinx needed to deliver. Xilinx chose the High-Performance Low-power (HPL) process at TSMC, and thereby avoided many of the pitfalls other companies experienced at this node. More significantly, HPL allowed Xilinx to deliver industry-leading performance per watt *(see Figure 1)*. The tightly controlled HPL process, earlier customer engagements, and real-world design rules ultimately yielded:

- A proven supplier engagement model, including technical engineering and executive-level involvement
- Process and Performance Learning Vehicles (PPLVs), which resolved many complex issues to accelerate NPI and increase design confidence *(see Figure 2)*
- Functional margin, moving from 40nm tri-Tox to 28nm dual-Tox
- A high-k/metal gate process with much lower gate current compared with SiON/PG, resulting in fewer issues and faster time to market

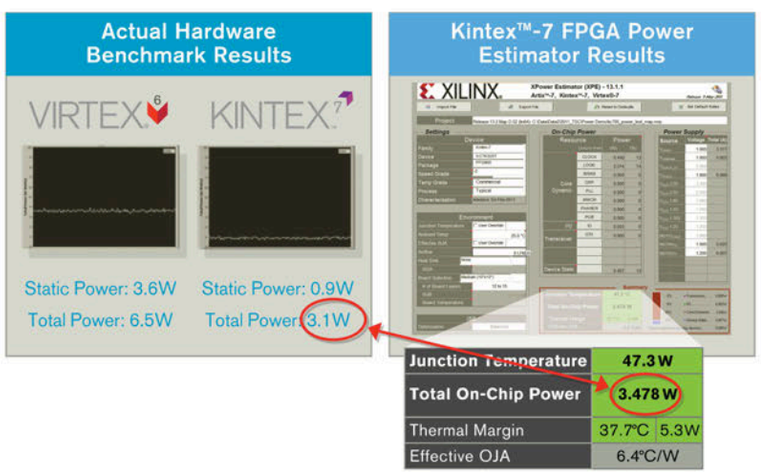


Figure 1: The Xilinx Power Estimator tool was tuned continuously using targeted simulation based on test vehicle results and early architectural learning, giving designers highly accurate results.

Driving Success Generation after Generation

Xilinx engineers have proven that they verify, characterize, test, and qualify devices better and faster than anyone else in the industry, all while achieving absolute quality. For three generations, Xilinx's advanced NPI methodology and milestone criteria *(see Figure 2)* have been tightened to keep ahead of increasing device complexity. At 28nm, the advancements improved data collection, verification, and characterization with:

- Highly automated design flows and timing analysis
- Verification and characterization processes for earlier identification of issues and earlier corner material (12 weeks sooner than previous generation)
- Test coverage exceeding 99.7%, with earlier data collection
- More tracking tools, for daily metrics reporting and sharing across functional teams

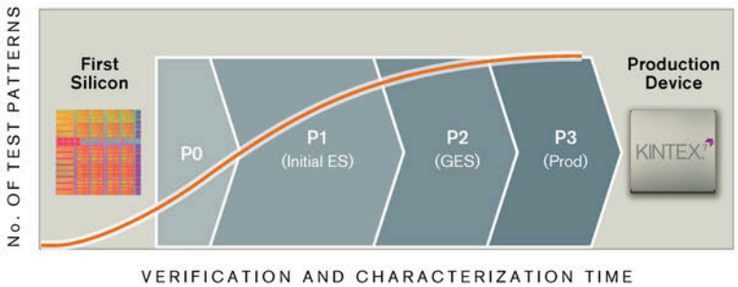


Figure 2. From first silicon to production material ship, Xilinx has redefined its verification and characterization process to drive early discovery to release 7 series with zero errata.

Robust Technology Reliability

Xilinx reliability methodologies overcame the shrinking reliability margins at the current process node. By leveraging early learning and in-depth tools expertise, Xilinx engineers shortened development processes from months to days, and accommodated the extra iterations required at 28nm. As a result, Xilinx devices are meeting the stringent requirements of the most reliability-sensitive applications in industrial, automotive, aerospace, and defense industries *(see Figure 3)*:

- Enhanced Design-for-Reliability (DFR) guidelines have proven a FIT rate less than 17 at production.
- Improved outlier elimination and new DFR methodology are combating the "shrinking bathtub" curve at 28nm.
- Xilinx engineering and quality assurance programs have yielded proven, predictable, and very-low failure rates over extended device lifetimes. The 28nm devices were released to production with power and defect density (DD) beating previous estimations.

Wear-Out Test Summary

Mechanism	Conditions of Quoted Results	Conditions of Quoted Results	Lifetime at Junction Temperature			Remarks
			85°C	100°C	125°C	
VRDB	B mode≤D (<1/cm²)	B mode: V_{CC} <V_{IN} <2.5V ($_{max}$) 1.8V <V_{IO} <4.1V (I/O)	Pass	Pass	Pass	
P2ID	Gate Oxide TDDB	Maximum operating voltages (see the 7 series FPGAs FPGAs data Sheets[15])	TDDB lifetimes are calculated for each product in Table A-4	181 years for XC7V585T	139 years for XC7V585T	129 years for XC7V585T	Typical product-level lifetime[16]
				66 years for XC7V585T	54 years for XC7V585T	52 years for XC7V585T	Worst-case product level lifetime[17]
Electromigration	Hot Carrier Injection		Checked by MOSRA[15] Worst at cold for I/O transistors and hot for other transistors	433 years	522 years	685 years	Typical product-level lifetime[16] (38 years @ -40°C)
5M				124 years	149 years	195 years	Worst-case product level lifetime[17] (11 years @ -40°C)
BEOL TDDB	PBTI		Checked by MOSRA[15] and product HTOL	222 years	113 years	41 years	Typical product-level lifetime[16]
				59 years	30 years	11 years	Worst-case product level lifetime[17]
	NBTI		Checked by MOSRA[15] and product HTOL	285 years	84 years	13 years	Typical product-level lifetime[16]
				112 years	33 years	5 years	Worst-case product level lifetime[17]

Figure 3. 28nm wafer-level reliability exceeds transistor and interconnect market requirements to deliver industry-leading device FIT.

Unleashing Silicon Development

"Our 28nm 7 series, Zynq, and Vivado design suite deliver the leadership value our customers have come to expect from us. Our strategy of designing our All Programmable products with TSMC's high-performance, low-power 28HPL technology, together with our scalable optimized 7 series architecture, and leveraging our industry-leading stacked silicon interconnect technology have put us a full generation ahead of the competition. We co-optimized the 7 series FPGAs and Zynq All Programmable SoC with the Vivado Design Suite to deliver a high-quality, compelling user experience. Achieving these multiple breakthroughs is a testament to our talented employees and their commitment to creating high-value, high-quality innovative products for our customers. We went "all in" at 28nm to give our customers a huge boost in building compelling products faster, and we delivered."

VICTOR PENG
SVP, Programmable Platforms Group
XILINX, INC.

3D Packaging

INNOVATION

STACKING SILICON PUSHES THE LIMITS, and allows Xilinx to set new standards for capacity and performance. 3D packaging has driven devices beyond the confines of Moore's Law, both for monolithic and heterogeneous devices. To mitigate the risks associated with stacked silicon and meet quality goals for breakthrough 28Gb/s devices, Xilinx used earlier learning from lead-free flip-chip test vehicles (ranging from 90nm to 28nm) and leading-edge modeling and manufacturing methodologies that address the increased complexity.

Innovation Proof Points

- The microbumps (~200,000) and C4 bumps (~20,000) passed all criteria for reliability, solder inelastic strain, and fatigue.
- The 2000T has passed all qualification requirements including power cycling at 28nm, with 6.8 billion working transistors.

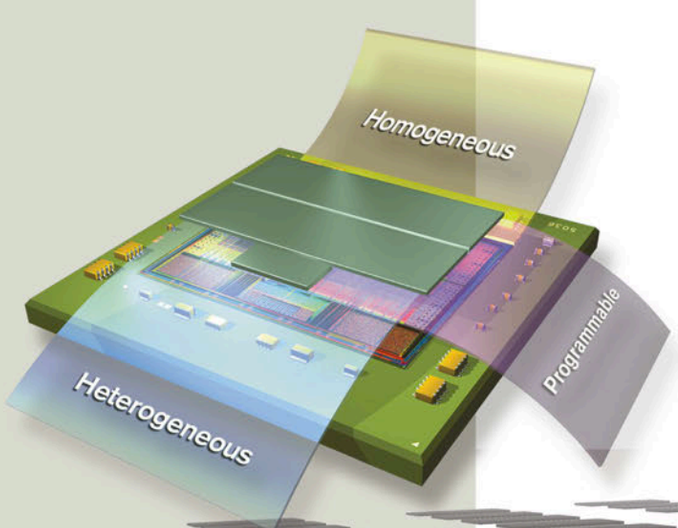
Stress	Conditions	Criteria
HTOL	T=125°C, Vccmax, Dynamic	Pass
PC	3x Reflow	
	Ramp up 30°C to 130°C in 3 minutes	
	Hot Dwell 6 minutes at 127°C - 130°C	
	Ramp down: 130°C to 30°C in 3 minutes	
	Cold Dwell: 6 minutes at 27°C - 30°C	
THB	MSL4; Ta= 85°C, RH= 85%, Alternative Bias	
TH	MSL4; Ta= 85°C, RH= 85%	
HTS	3x Reflow, Ta= 150°C	
TC-B	MSL4, -55°C / +125°C	

More and More… than Moore

More on a chip and more chips in a package—for more advanced systems. The world's first 3D FPGA *(see Figure 1)*, the Xilinx Virtex-7 2000T, represents a breakthrough in all of these dimensions that required very stringent qualification and test. The industry's first heterogeneous 3D IC required further advancements, including:

- Low-temperature co-fired ceramic (LTCC) packaging for optimal signal integrity
- Optimization of package substrate material and interposer resistivity to achieve 28Gb/s system channel characteristics
- Design and timing verification of high-performance inter-die interconnects
- 3D thermal-mechanical modeling and analysis for package reliability, addressing package co-planarity issues and stresses introduced by the interposer

To learn more about these Xilinx advancements, please read the 3D Packaging datasheet that is included with this Annual Quality Report and located at www.xilinx.com/quality.



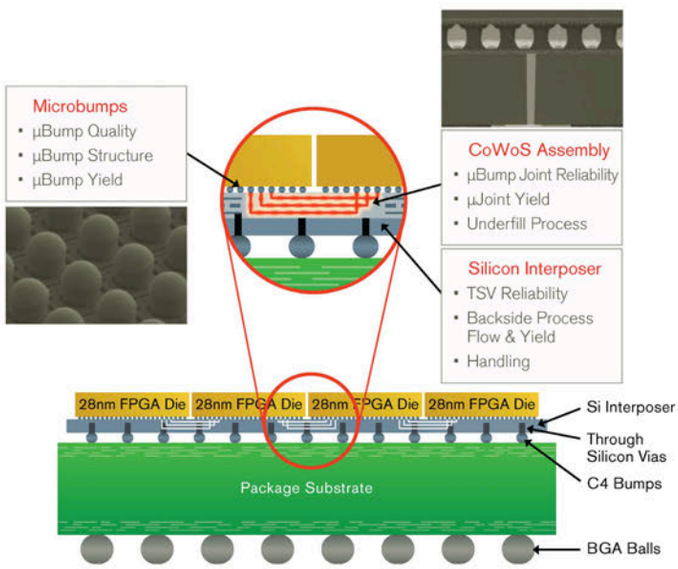


Figure 1. SSIT cross-section showing key quality considerations on a typical qualified SSI device using TSMC's CoWoS process.

Known-Good Die

Stacked silicon offers the inherent advantage of selecting "like" products in terms of power consumption and speed, which means more predictable results than monolithic silicon. A comparison of simulated and actual eye diagrams demonstrates this exceptional quality *(see Figures 2 and 3)*. The methodologies behind the industry's first 28nm 28Gb/s 3D heterogeneous devices include known-good die selection to meet performance and specifications. Selection starts with solid test and manufacturing methodologies at the assembly site, and includes:

- Ensuring multiple-die performance by adding system timing check to characterization process
- DFM rules that provide performance advantages
- Enabling power die optimization during selection, through known-good die testing at wafer sort at 0°C, now standard across the 7 series
- FPGA self-diagnostic capabilities for higher test coverage confidence
- Reliability prediction, using a custom hierarchical, end-to-end tool that draws on a Xilinx design database (physics of failures/wear-out from foundries)
- Expanded wafer qualification using three additional elements for assembly testing: electrical, thermal, and mechanical

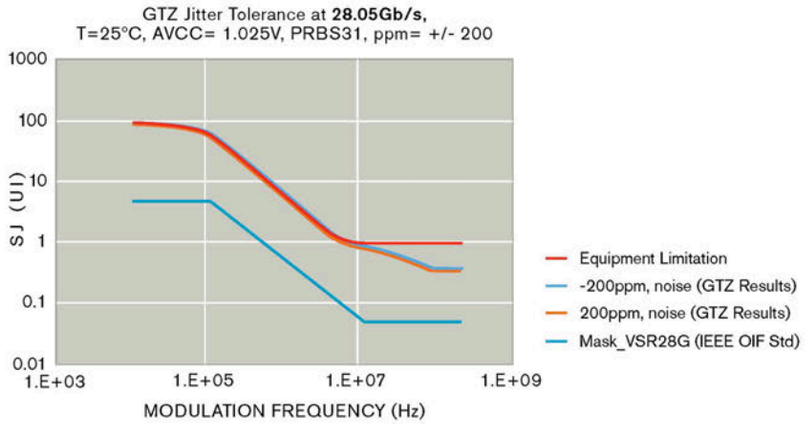


Figure 2. Heterogeneous SSIT packaging makes it possible to exceed IEEE standards for high-speed channel quality in the Xilinx GTZ SerDes at 28Gb/s.

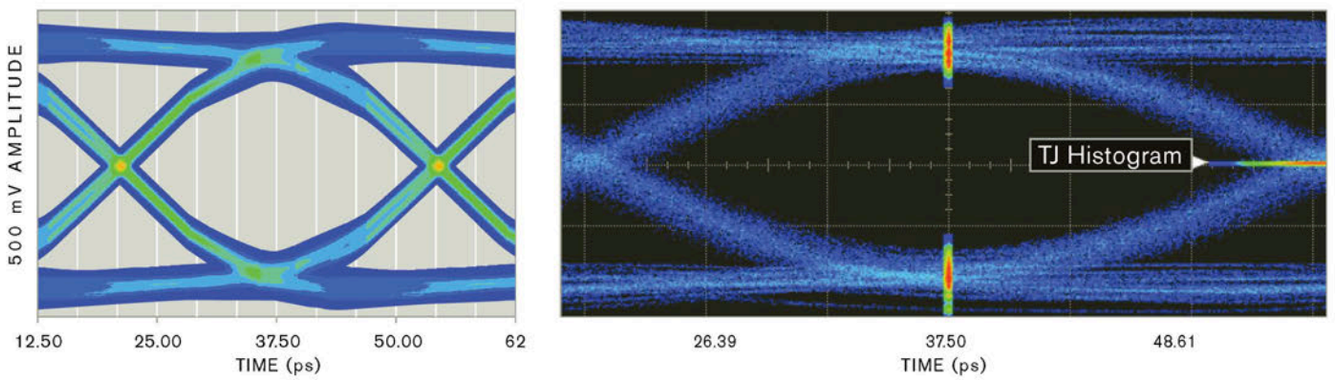


Figure 3. Collaborating with TSMC and using test vehicles to learn from real-world process data allowed development modeling to achieve 28Gb/s design milestones as shown in the simulated (left) and actual (right) eye diagrams.

Unleashing Stacked Silicon

"To push beyond conventional thinking and break through Moore's Law in delivering our 3D IC solution, we needed to deliver a superb level of engineering excellence. In doing so, we opened up a new frontier for combining technology building blocks, from cost-effective component die. This could not have been accomplished without a laser focus on prevention and flawless engineering execution from Xilinx and our supply partners."

LIAM MADDEN
VP, FPGA Development and Silicon Technology
XILINX, INC.

SoC INTEGRATION

IT TAKES MORE THAN LOGIC. Xilinx has redefined integration by wrapping industry-leading logic and I/O fabric around an ARM® processor subsystem. This industry first leveraged learning that began more than 10 years ago with the Virtex-II Pro and continued through Virtex-4 and Virtex-5 PowerPC designs. Xilinx proprietary approaches for testing and characterizing FPGA and processor interactions now yield an advanced, robust SoC that simplifies design and unleashes future generations of All Programmable systems.

SoC Characterization and Verification

- Carried out under conditions that align with the most stringent customer requirements
- Block characterization improvements for GTX and for BRAM:
  - New Verilog flow
  - Customization of build-in self-test (BIST) march sequence
- Tests run using memory test boards, varying attributes, and test conditions that exceed specifications by 10%
- Additional corner-case and system-level testing
- 3x increase in the number of targeted reference designs* (TRDs) compared with previous generation
- 3x increase for exercising non-processing areas (connectivity, DSP, AMS, etc.)

** The Vivado tools are used for design testing, which makes this testing part of the critical release criteria for the tools themselves.*

Simplifying SoC Solutions

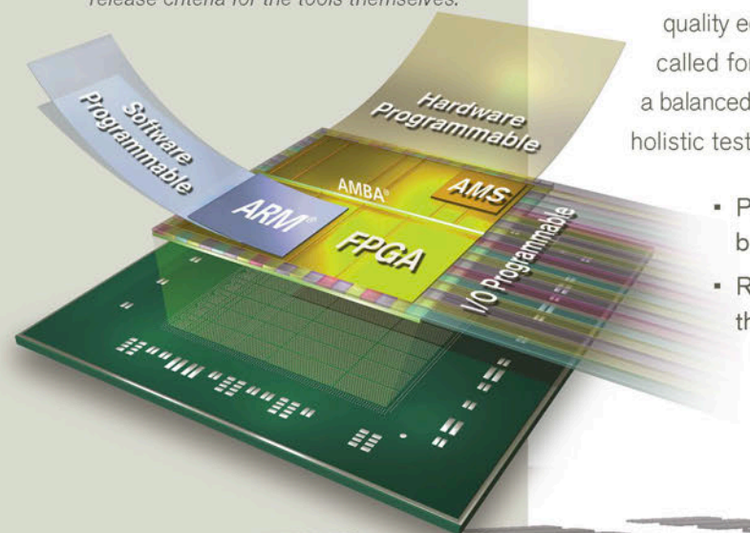
The Zynq™-7000 All Programmable SoC replaces chip-to-chip latencies with high-speed FPGA-processor connections, and gives designers the latest Xilinx advancements such as 7 series SerDes to support maximum throughput and capacity for SoC designs. Engineers and system architects can leverage SoC capabilities, implement accelerators in software or hardware, and bring more complex designs to market with confidence in the quality of the total solution.

Besides leveraging learning and enhancing design tools, Xilinx introduced new mechanisms for integrating system-level verification of target specifications for the processor subsystem, logic, and IP *(see Figure 1)*. The scalable optimized architecture and common blocks across the 7 series FPGAs and SoCs contributed to absolute quality and accelerated rollout of devices. After verification of the first Kintex-7 325T device, many 28nm devices went straight into production after the first tapeout.

Quality at the System Level

The role of FPGAs has evolved from "glue logic" and rapid prototyping to the hub at the heart of advanced systems. Device testing has similarly evolved to track more advanced applications, with system-level testing being a significant component in the Xilinx quality equation. Zynq-7000 quality, while benefiting from many proven practices, called for further refinements at every stage of development and was driven by a balanced focus on silicon verification, system-level performance, and extensive, holistic testing:

- Prior to silicon, extensive emulation leveraged the EDK platform and booted operating systems such as Linux for emulation.
- Rearchitected verification and characterization approaches solidified the on-chip FPGA fabric.



- Randomized continuous testing of the processor subsystem exercised the SoC-unique feature set:
  - Guidelines stem from the Xilinx embedded software initiative, aimed at processor-IP testing
  - Verification IPs for all Xilinx interfaces (e.g. DDR, USB, Ethernet MAC, etc.)
  - Constrained-random and random test generation
  - Compliance testing for interface standards
  - Results: catching more than just Xilinx device issues (external bugs in other components such as PCI Express® chipsets)
- Processor-FPGA interactions were tested, during which the processor subsystem is the master.
- Additional SoC-specific characterization and verification were performed, such as Open Verification Methodologies (OVM).
- Stringent coverage and metric-driven verification performed on the SoC *(see Figure 2).*

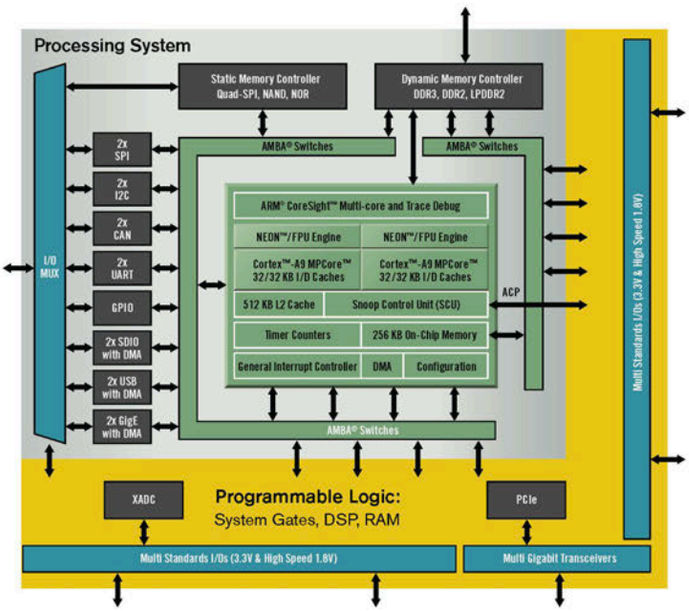
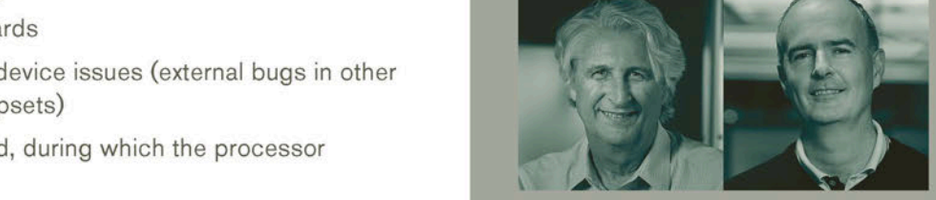


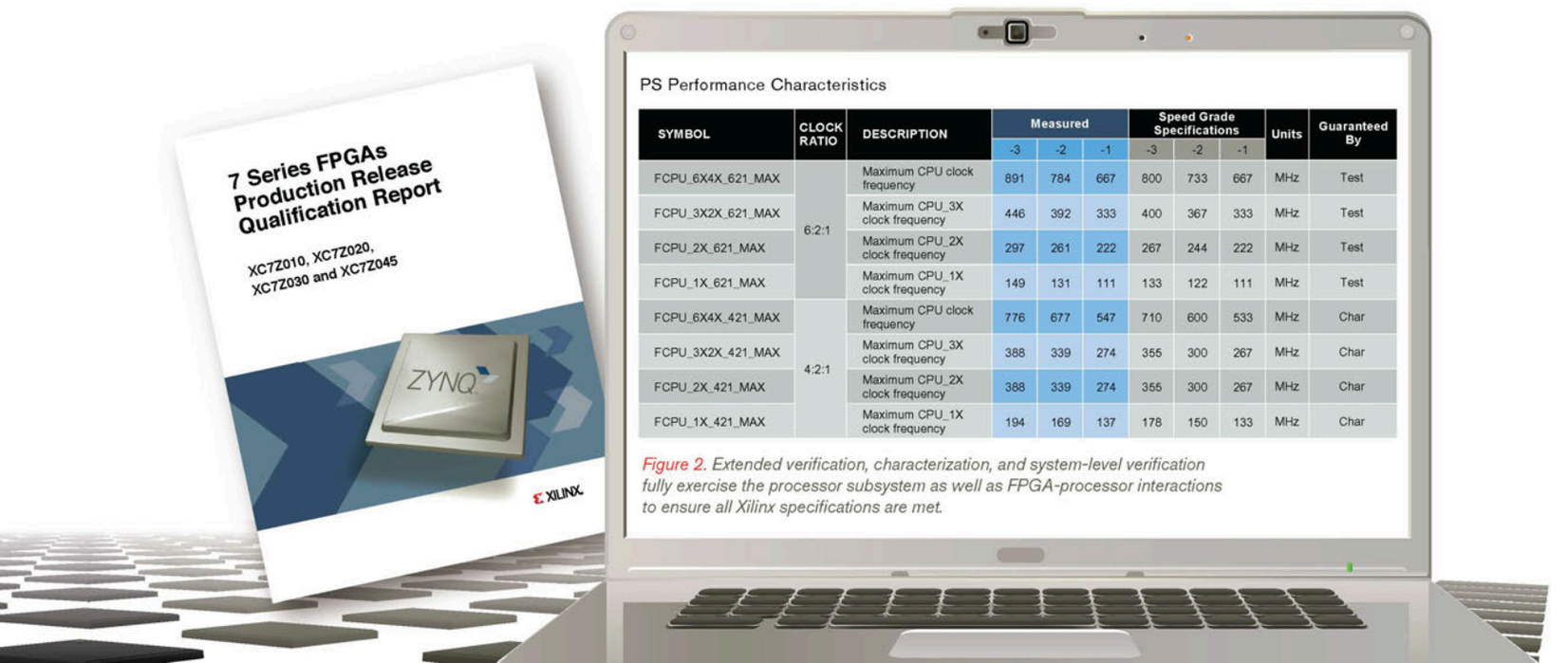
Figure 1. Leveraging the FPGA learning from our scalable optimized architecture, Xilinx was able to de-risk the Zynq evaluation and to launch in record time.



Unleashing Customer Acceleration

"As design complexity and integration increase, our customers demand top-quality system solutions to accelerate their design capabilities. The Zynq platform provides a fully verified prebuilt processing system completely validated along with its associated software and tools. With this platform, Xilinx delivers the highest level of performance and quality, which our customers expect."

VIDYA RAJAGOPALAN
VP, Processing Solutions
XILINX, INC.



PS Performance Characteristics

SYMBOL	CLOCK RATIO	DESCRIPTION	Measured			Speed Grade Specifications			Units	Guaranteed By
			-3	-2	-1	-3	-2	-1		
FCPU_6X4X_621_MAX	6:2:1	Maximum CPU clock frequency	891	784	667	800	733	667	MHz	Test
FCPU_3X2X_621_MAX		Maximum CPU_3X clock frequency	446	392	333	400	367	333	MHz	Test
FCPU_2X_621_MAX		Maximum CPU_2X clock frequency	297	261	222	267	244	222	MHz	Test
FCPU_1X_621_MAX		Maximum CPU_1X clock frequency	149	131	111	133	122	111	MHz	Test
FCPU_6X4X_421_MAX	4:2:1	Maximum CPU clock frequency	776	677	547	710	600	533	MHz	Char
FCPU_3X2X_421_MAX		Maximum CPU_3X clock frequency	388	339	274	355	300	267	MHz	Char
FCPU_2X_421_MAX		Maximum CPU_2X clock frequency	388	339	274	355	300	267	MHz	Char
FCPU_1X_421_MAX		Maximum CPU_1X clock frequency	194	169	137	178	150	133	MHz	Char

Figure 2. Extended verification, characterization, and system-level verification fully exercise the processor subsystem as well as FPGA-processor interactions to ensure all Xilinx specifications are met.

Design Tools
PRODUCTIVITY

TIME IS MONEY. Even breakthrough innovations such as Xilinx All Programmable devices require the right tools to achieve maximum value and deliver the highest level of quality. In 2012, the launch of the graphical Vivado Design Suite raised productivity by 2x to 5x with predictable user experiences. The integrated, highly automated design flow and intuitive GUI boost quality while also speeding integration and implementation. This results in better efficiency and predictability, and promotes design reuse and plug-and-play IP.

An Expanded Testing Base

For Vivado, verification teams took advantage of a much larger number of boards to expand testing:

- Larger beta base for 2012.1 compared with ISE beta tests
- 500+ customers participating in 2012.2 release beta test
- Releases slowed to emphasize focus on quality and zero-defect goal (.2 and .3 releases)
- Beta opened earlier to the web audience for 2012.4 (new feature testing)

Ecosystem Participation in Release Testing

- Early partner/ecosystem participation
- Real-time debugging, using partner IP, for testing and improved quality of first release
- Extended requirements and tier definitions for ecosystem partners to include Vivado training and proficiency
- Results: Hundreds of products already on 7 series; more than 50 partner IP cores supporting AXI

Bringing a Design Vision to Life

Based on a single data model, Vivado represents a major advancement in ease of use for All Programmable developers. The new architecture offers fast convergence and timing closure, and highly efficient memory utilization at 28nm *(see Figure 1)*, as well as for future families with more than 10M logic cells. For the quality team, Vivado represented an unprecedented project in terms of scale and complexity, which called for expanded beta testing with partners and customers, more stringent metrics and tracking, and numerous process enhancements. Highlights of the 2012 Vivado quality results include:

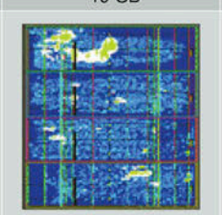
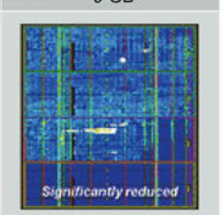
	ISE	Vivado
P&R Runtime	13 Hours	5 Hours
Memory Usage	16 GB	9 GB
Reduced Wire Length & Congestion		
Concurrently Optimizes Timing, Device Utilization		

Figure 1. The Xilinx design suite was rearchitected to enhance the customer experience and provide superior quality of results. Customer summary data reflects success based on these goals, and will drive further advancement of Vivado.

- Higher-than-expected adoption of the tool suite, including the IP Integrator, which drives up the level of abstraction for IPs for improved ease of use.
- Faster feedback mechanisms allowed more iterations of testing, resulting in fewer customer-discovered bugs.
- The Tcl API is shortening design cycles by identifying critical issues before place and route. Designers have the flexibility of working in a scripted Tcl environment, an interactive Tcl shell, or a graphical project tool. Tcl allows much more in-depth testing (better coverage) of implementation tools.
- Pre-qualified IP has enhanced tool testing methodology, and helped identify more bugs prior to release.

Predictable User Experiences and Design Methodology

The Xilinx zero-defect mindset was applied to the Vivado tool suite from the beginning and feedback from customer surveys indicates that Vivado quality has consequently exceeded expectations. Besides 20% more stringent release criteria, the quality was a result of more and earlier testing (*see Figure 2*), and real-time feedback that accelerated iterations. Builds were done daily, along with metrics tracking, and testing leveraged expanded libraries that included more complex targeted designs and real customer-submitted designs. Other key factors that reduced bugs:

- C and standards-based IP integration with fast verification (100x faster C verification; 4x faster C to verified RTL; 4x faster IP reuse and time to IP integration)
- Hierarchical implementation and advanced closure automation (4x faster design closure; 3x faster incremental ECO; 20% better LUT utilization)

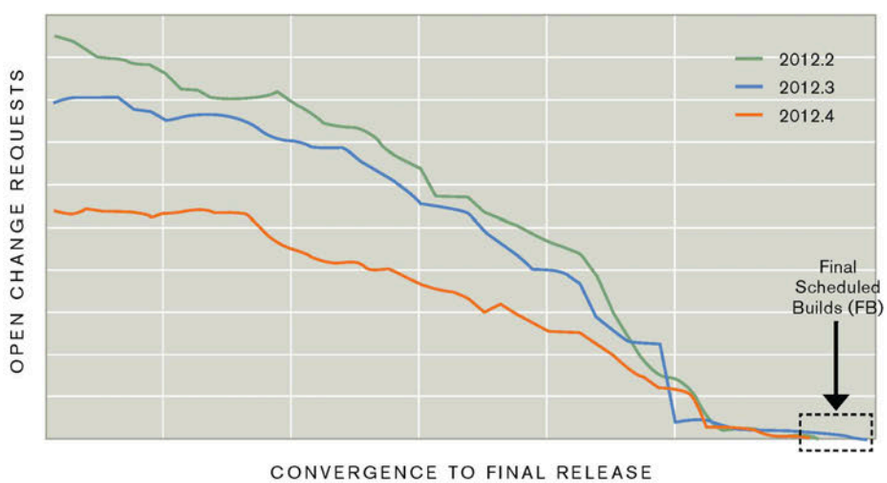
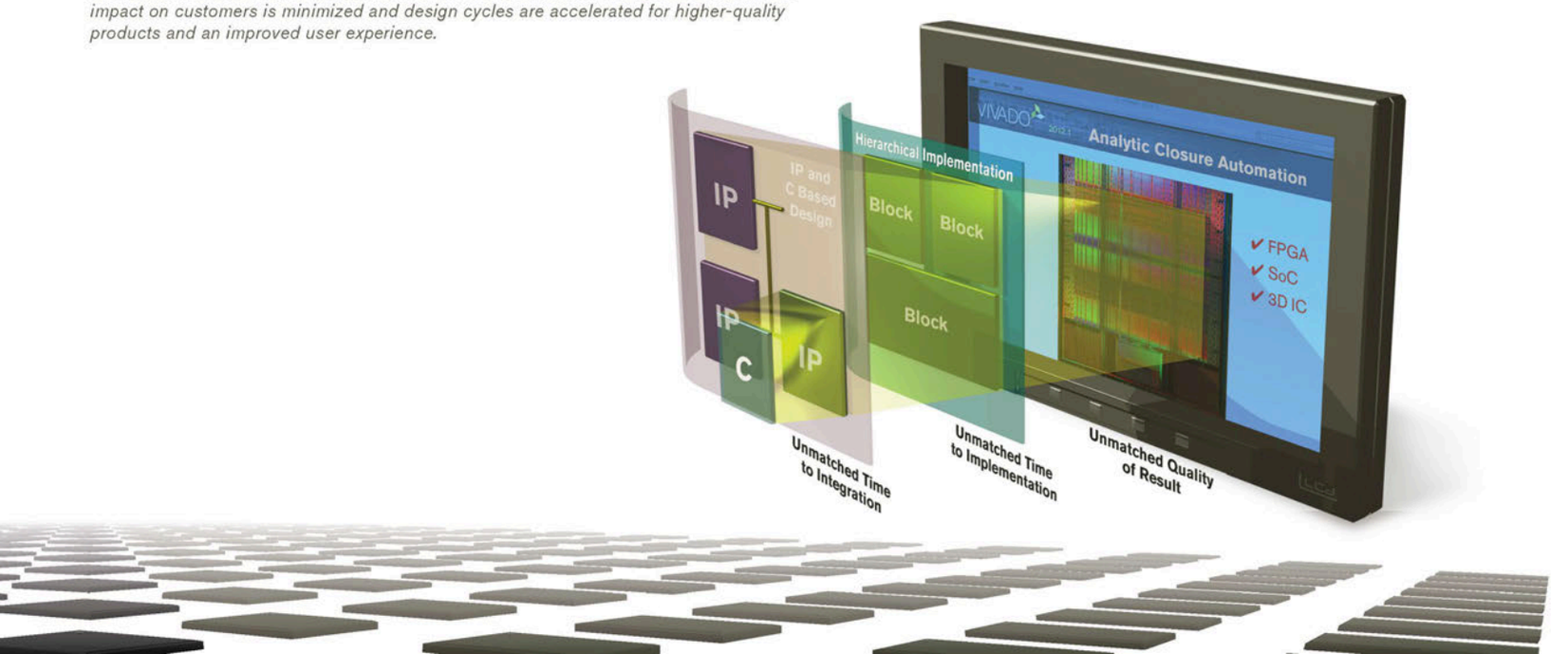


Figure 2. Earlier and more stringent testing and verification mitigate the risks that stem from increasing complexity. Testing with higher-level customer designs increased the prerelease discovery and resolution of issues. With more issues identified during development, the impact on customers is minimized and design cycles are accelerated for higher-quality products and an improved user experience.

Unleashing FPGA Possibilities

"As design complexity increases, in step with quantum increases in capacity and performance of integrated solutions, the need for a revolutionary design environment has become compelling. Over four years ago, we set out to build a completely new platform of design tools, architected around a shared, scalable data model. The results in 2012 already show the success of this strategy and ensure the continued adoption with higher-quality results for all customers."

SALIL RAJE
VP, Software and IP Products Development
XILINX, INC.



Quality
BUILDING TRUST

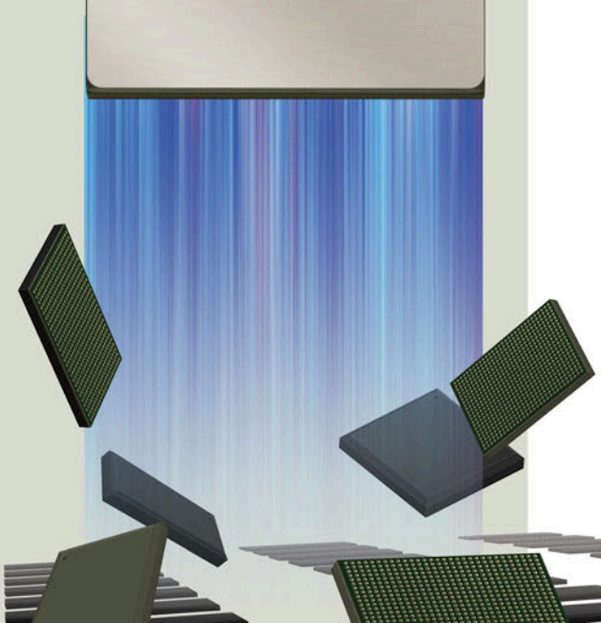
TRUST IS EARNED over time, by performing consistently and delivering results that exceed expectations. Xilinx enjoys strong working relationships with customers because of an unwavering commitment to quality. The evidence of this commitment—the true testimonial to Xilinx quality—is the real-world data that focuses on end-user experiences and design results.

Quality Proof Points

- RMAs reduced by >60% since 2008
- 55% of customer RMA issues resolved in the field for 2012
- Customer scorecard has remained above 9.0 since Q1 2009
- No major excursion recall for the past six years
- All Xilinx products meeting <10PPM

2012 Quality Awards

- Excellent Core Partner (Huawei)
- Scorecard Performance Award in the area of Quality (National Instruments)
- Supplier of the Year (Spirent)



Full-Circle Support and Feedback

Regardless of the amount of in-house testing, analysis, and issue resolution, the most credible and meaningful measures of quality are those that come back from customers. From top to bottom, Xilinx executives, managers, and engineers diligently focus on customers and adjust Xilinx products, programs, training, and support to deliver optimal results. Key customer-centric feedback includes:

- Validated customer returns (RMAs), which are tracked against products shipped and which show an overall rate of <10PPM *(see Figure 1)*
- Since 2008, closed-loop customer root cause shows that only 19% of RMA cases stem from Xilinx issues *(see Figure 2)*
- Customer feedback (NPS), based on RMA case data which show exceptionally high customer satisfaction

Frequent and extensive knowledge sharing also helps optimize Xilinx customer successes. Discussions and information sharing, which often include partners and suppliers, provide a high level of transparency regarding:

- Unique device DNA for more timely device analysis
- Design checklists and development methodology
- Design margins, with validated results from design evaluation samples
- Design issue mitigations, offered at early stages and prior to production release for early adopters

Spartan FPGA		
Product	Technology Node	PPM
Spartan-II/IIE	.22µm/.18µm/.15µm	0.0
Spartan-3	90nm	0.3
Spartan-3E	90nm	0.0
Spartan-3A/3AN	90nm	0.4
Spartan-6	45nm	0.7

Virtex FPGA		
Product	Technology Node	PPM
Virtex/-E	.25µm/.18µm	0.0
Virtex-II/IIP	.15µm/.13µm	0.6
Virtex-4	90nm	1.8
Virtex-5	65nm	4.6
Virtex-6	40nm	4.9
7 series	28nm	0.0

Figure 1. Based on customer return data, CY2012 product PPM demonstrated the Xilinx zero-defect mindset.

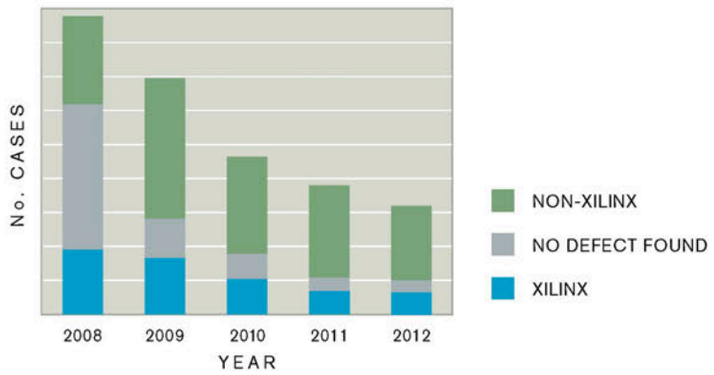


Figure 2. Over the last four years, RMAs have been reduced by >60% as a result of product quality, customer support, and direct engagement for issue resolution.

The Bottom Line

Xilinx and customers—with support from technology suppliers and partners—make up a tightly linked community. The entire ecosystem must succeed to drive up the quality of the end solutions enabled by Xilinx innovations. Periodic quality scorecards provided by customers are therefore the true measure of Xilinx quality *(see Figure 3)*.

Additional Xilinx customer-facing quality hallmarks include:

- Closed-loop focus on root cause
- On-line RMA portal for real-time customer support
- Transparent change management and data reporting including horizon reports, reliability, SEU, RMA, and automatic notifications
- Executive commitment to improving customer satisfaction

Unleashing Customer Confidence

"For the 28nm portfolio, our quality was achieved on the basis of work that began with a clear strategy and a chain of decisions made years ago. The development teams all embrace complete ownership of their results and this ensures that quality emanates from the very source of the innovation. At 20nm, we look forward to maintaining our position of being A Generation Ahead."

JACK ELWARD
VP, Worldwide Quality Systems and Customer Support
XILINX, INC.

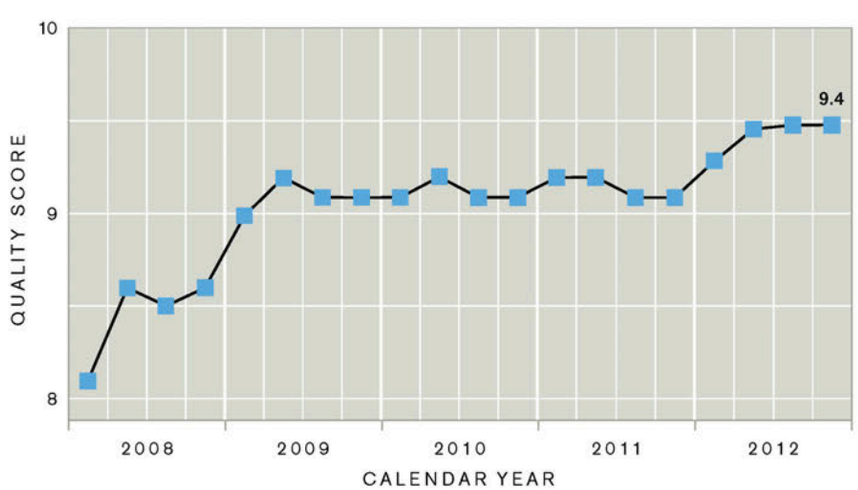
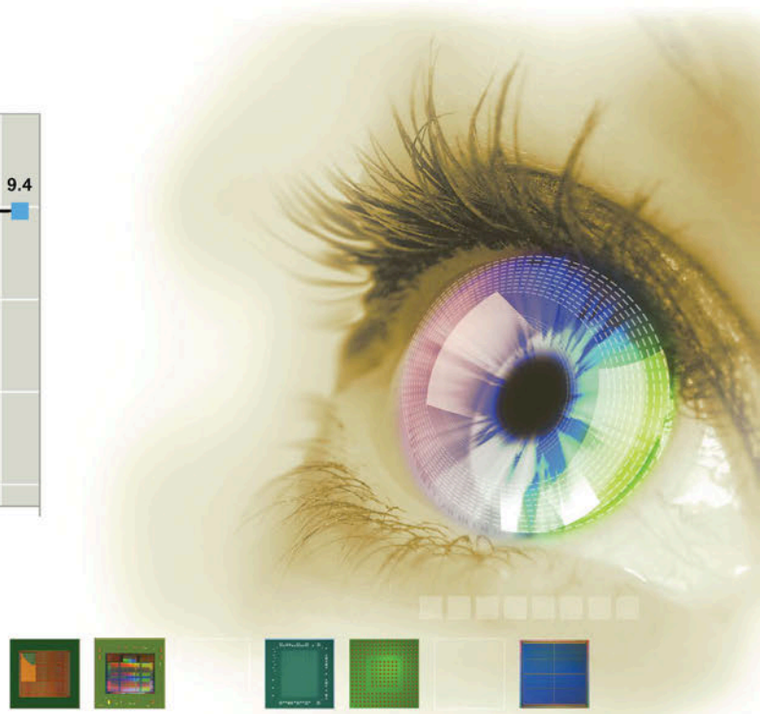
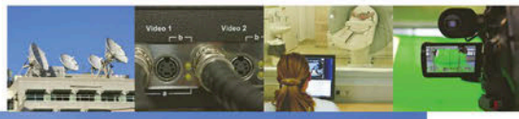


Figure 3. Top management focus on customer feedback and flawless results continue to drive positive customer results.





20nm LEADERSHIP

CHALLENGES GIVE RISE TO INNOVATION. With each generation of devices, Xilinx introduces technology advances that overcome existing limitations, allowing engineers to build more value into electronic systems. At 20nm, the Xilinx 8 series will include second-generation All Programmable FPGAs, 3D ICs and SoCs that build on the momentum and market leadership established at 28nm.

Unleashing the Next Generation

"Since the FPGA was introduced in 1984, Xilinx innovation, culminating with 28nm execution, shows that Moore's Law is not 'The Limit.' Technology limits will endure, but innovations will continue to drive through those barriers needed for the next-generation challenge."

IVO BOLSENS
SVP, Chief Technology Officer
XILINX, INC.

20nm Proof Points

- Leveraging 28nm learnings and a scalable, optimized architecture
- Second-generation SSIT/PS architecture leveraging proven technology
- Second-generation high-k/MG reduced process variation (i.e., gate-last, high-k-last)
- NMOS elevated source/drain, PMOS eSiGe to boost performance
- Intact design, verification, and integration teams to carry forward HPL expertise

Staying a Generation Ahead at 20nm

Xilinx began developing 20nm in 2010. Before shipping the first 28nm device, a rigorous approach for 20nm was well under way. Since then, the lessons learned at 28nm have helped Xilinx refine 20nm process and product qualification methodologies, including extended temperature testing and a renewed focus on wear-out data and reliability estimations. In addition, Xilinx is introducing major testing changes stemming from early DFT specifications. The new opportunities for Xilinx leadership and innovation at 20nm will include double-patterning lithography, gate dielectric scaling, increasing I/O and packaging complexity, scaling power, and overall changes to testability and reliability.

A World-Class Team

In collaboration with TSMC, Xilinx is driving solutions to all of the 20nm challenges, and the extended ecosystem will continue to play an expanding role in the introduction of the next-generation devices. In addition, our "Voice of the Customer" initiative continues to grow as IP, design tools, and silicon become more integrated solutions. Supporting the world-class Xilinx extended team is a solid foundation of engineering achievements based on learning from previous generations.

On Track

Data from 20nm results indicate that Xilinx, together with its leading foundry partner, is on track to deliver the next-generation technology solutions. The next generation will build on proven foundations including second-generation SSIT and embedded ARM processor architecture. Xilinx validation is on track to deliver on performance and power. The successful demonstration of Xilinx technology, quality, and reliability at 20nm will continue to motivate every Xilinx team to build on this momentum to excel with each new generation.

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe

Xilinx Europe
2020 Bianconi Avenue
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific

Xilinx Asia Pacific Pte. Ltd.
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

For more information about Xilinx and its All Programmable solutions, visit:
www.xilinx.com/quality

XILINX
ALL PROGRAMMABLE™

Printed in the U.S.A. PN 2538

DATASHEET COLOR KEY

INNOVATION

QUALITY

CASE STUDIES

"For more than 10 years, Xilinx has been a trusted supplier of programmable logic devices and solutions for space applications. Boeing appreciates the long-term collaboration it has had with Xilinx and their commitment to delivering quality products and services to Boeing and its programs."

DAVID A. SUNDERLAND
Senior Technical Fellow
BOEING SPACE &
INTELLIGENCE SYSTEMS

"We're pleased to see the success of the Xilinx Zynq-7000 All Programmable SoC. Our teams worked side-by-side with Xilinx to ensure the highest verification and quality and that their tapeout was successful. The breakthrough devices ideally serve high-end embedded applications that require high performance with low power consumption."

PETER MIDDLETON
Vice President of Engineering, Processor Division
ARM LTD.

"Anritsu business expansion has occurred mainly in the information and communication field by providing test and measurement solutions indispensable to the development, manufacture, and maintenance of a range of communication systems as typified in mobile phones and the Internet on a global scale. Advanced high-performance FPGAs which are provided by Xilinx contribute significantly to the realization of our solutions."

HIROYUKI FUJIKAKE
Senior Manager, Procurement Department
ANRITSU CORP.