

NOEL-V/GRLIB RISC-V 64-bit Processor



Introduction

The NOEL-V is a synthesizable VHDL model of a 64-bit processor that implements the RISC-V architecture. The processor is the first released model in Cobham Gaisler's RISC-V line of processors that complement the LEON line of processors.

The NOEL-V is dual-issue, allowing up to two instructions per cycle to be executed in parallel. To support the instruction issue rate of the pipeline, the NOEL-V has advanced branch prediction capabilities. The cache controller of the NOEL-V supports a store buffer FIFO with one cycle per store sustained throughput, and wide AHB slave support to enable fast stores and fast cache refill.

The NOEL-V is interfaced using the AMBA 2.0 AHB bus (subsystem with Level-2 cache and AXI4 backend is also available) and supports the IP core plug&play method provided in the Cobham Gaisler IP library (GRLIB). The processor can be efficiently implemented on FPGA and ASIC technologies and uses standard synchronous memory cells for caches and register file.

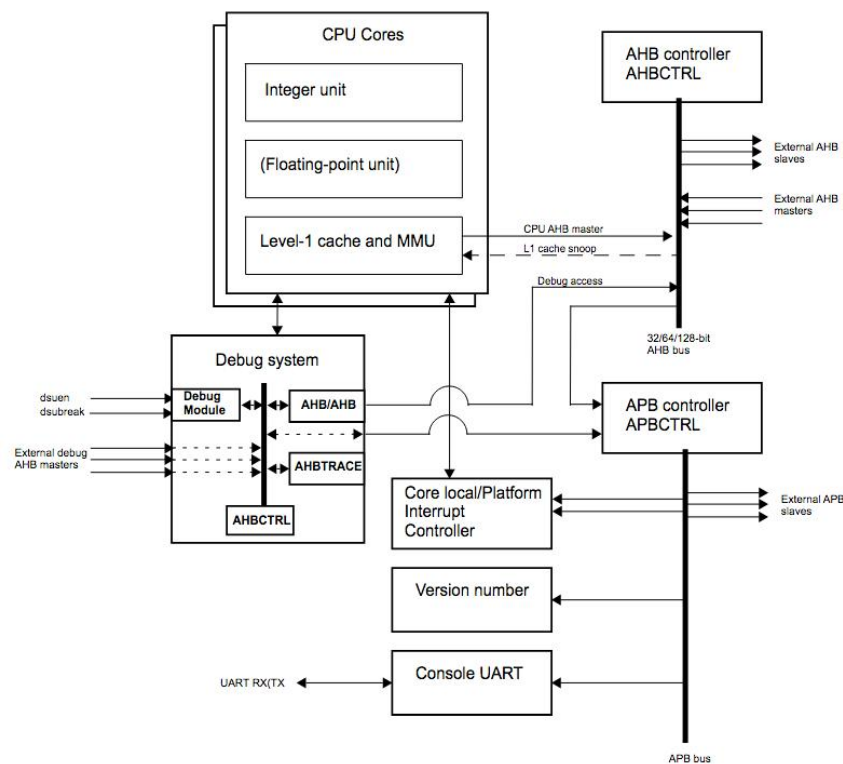


Figure 1 NOEL-V subsystem

The processor model is available as part of the GRLIB IP Library. The GRLIB IP Library is an integrated set of reusable IP cores, designed for system-on-chip (SOC) development. The IP cores are centered around the common on-chip bus, and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique plug&play method is used to configure and connect the IP cores without the need to modify any global resources.

The library includes a wide range of peripherals, including cores for AMBA AHB/APB control, the LEON SPARC processors, 32-bit PC133 SDRAM controller with EDAC, DDR2/3 SDRAM controller with EDAC, 32-bit PCI bridge with DMA, 10/100/1000 Mbit Ethernet MAC, 8/16/32-bit PROM and SRAM controller, 16/32/64-bit DDR/DDR2 controllers, USB 2.0 host and device controllers, CAN controller, SpaceWire controllers, SpaceFibre controllers, TAP controller, SPI, I2C, UART with FIFO, modular timer unit, interrupt controller, and a 32-bit GPIO port.

Features

The NOEL-V processor has the following features:

- RISC-V RV64GC
 - 64-bit architecture
 - Hardware multiply and divide units
 - Compressed (16 bit) instruction support
 - Atomic instruction extension
 - 32/64 bit floating point extensions using non-pipelined area efficient FPU or high-performance fully pipelined IEEE-754 FPU
 - Machine, supervisor and user mode. RISC-V standard MMU with configurable TLB.
 - User level interrupts
- RISC-V standard PLIC
- RISC-V standard PMP (physical memory protection)
- RISC-V standard external debug support
- Advanced 7-stage dual-issue in-order pipeline
- Dynamic branch prediction, branch target buffer and return address stack
- Four full ALUs, two of them late in the pipeline to reduce stalls
- Separate instruction and data L1 cache (Harvard architecture) with snooping
- Optional L2 cache: 256-bit internal, 1-4 ways, 16 KiB - 8 MiB
- Native AMBA 2.0 AHB bus interface, 32-, 64- or 128-bit wide.
- Subsystem including processor and Level-2 cache with AXI4 backend also available.
- Robust and fully synchronous single-edge clock design
- Extensively configurable
- High Performance: CoreMark*: 4.03 / 4.69** CoreMark/MHz

*-march=rv64im -mabi=lp64 -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20 using GCC 9.2.0 under RTEMS 5

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

Availability

The NOEL-V IP core is available as part of the GRLIB VHDL IP Core library.

Additional information

NOEL-V Processor Model product page: www.gaisler.com/NOEL-V

NOEL-V on Xilinx Kintex Ultrascale: www.gaisler.com/NOEL-XCKU