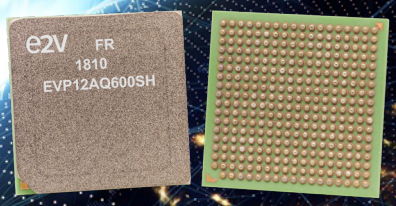
TELEDYNE e2v | Semiconductors
Everywhereyoulook™

EV12AQ600 – Product Brief

Space Grade 6.4 GSps 12-bit Quad ADC interoperable with XQRKU060



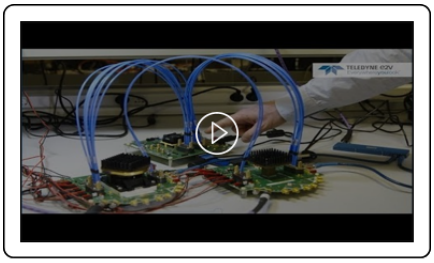
- **Cross-Point Switch**: option to assign ADC inputs to different ADC cores to perform time interleaving or not and have simultaneous sampling instead.
  - Built-in **Cross-Point Switch** (CPS) enabling 1, 2 or 4 channel mode at **6.4 GSps / 3.2 GSps / 1.6 GSps**
  - The only 4-channel space qualified available
- **Designed for space applications**, suitable for most common orbits. Hardened by Design and Layout.
  - QML Class-Y qualification flow
- Input frequency bands covered: **L, S, C-bands**
  - No frequency converters needed
- **Supports large multi-channel systems** with 4 channels per ADC.
  - Exclusive Synchronization chaining scheme and SYNC metastability management
  - Eased synchronization resource layout
- ADC reconfigurability to be used in **multi-mission systems**
  - One device qualified for multiple platforms: time and cost savings
- **License-free** and **hardened** serial data interface **protocol**: ESIstream (reduced FPGA resources)

Added values:

- Flexibility
- Reconfigurability
- Multi ADC Synchronization
- Multi-channel
- Multi-mission

QML Class-Y

ESIstream The Efficient Serial Interface

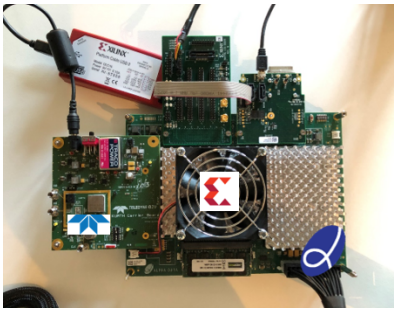


Click to Learn about multi-ADC synchronization in only 7 minutes!

L-BAND | S-BAND | C-BAND | X-BAND | Frequency Bands

DIRECT DIGITIZATION

- Interoperability proven with Xilinx KU060 on ADA-SDEV-KIT2 from AlphaData
- 12.5 Gbps data throughput on each of 8 lanes
- Logic resource utilization
  - 32-bit: 1.07% of LUTs, 0.38% of FFs
  - 64-bit: 1.60% of LUTs, 0.64% of FFs
- RX IP VHDL code available on ESIstream.com



XILINX

ALPHA DATA

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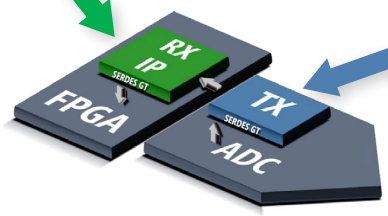
ESIstream The Efficient Serial Interface



- Hardening by design and layout on the ADC
  - Scrambling PRBS is tripled with voters
  - Possible PRBS integrity monitoring using
  - 2 Control Bits available in the frame header

www.teledyne-e2v.com/AQ600
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