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Optimal SelectIO Interface V_{REF} Generation Circuits

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Summary

A variety of PCB SelectIO™ interface V_{REF} generation circuits are used in FPGA design. Sometimes, large amounts of noise (200–400 mV) can be found on V_{REF} pins even with a PCB V_{REF} generation circuit that has been successful in previous designs. The presence of large amounts of V_{REF} noise can lead to loss of design margin with high performance SelectIO interfaces, such as wide DDR3 memory interfaces. This application note examines the source of this V_{REF} noise and recommends optimized PCB SelectIO V_{REF} generation circuits.

V_{REF} Input

Figure 1 shows a simplified view of a V_{REF} circuit inside the FPGA. The circuit is powered by the V_{CCO} rail of the SelectIO bank containing the V_{REF} pin. The FPGA comparator circuit presents a high-impedance input load (from a DC view).

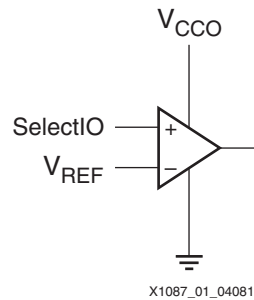


Figure 1: Simplified View of the FPGA V_{REF} Circuit

Tracking Requirement

In general, the V_{CCO} voltage for a SelectIO band has low-amplitude, high-frequency noise from multiple sources (such as SelectIO switching activity and switching power supply harmonics). For maximum noise margin, this requires the V_{REF} voltage generated by the PCB circuit to track the changes on V_{CCO} ($V_{REF} == \text{tracking } V_{CCO}/2$) in real time. This is easily achieved with a resistor divider, as shown in Figure 2.

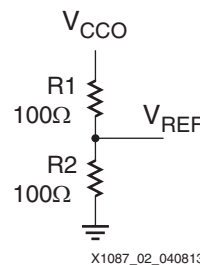


Figure 2: Resistor Divider for V_{REF} Generation

A standard voltage regulator should not be used for V_{REF} generation. Voltage regulators are designed to remove variation in the output voltage as a function of variation in the input voltage. In normal voltage regulator applications, this is a desirable feature. However, this is an

undesirable characteristic for V_{REF} applications in which the V_{REF} output is intended to track V_{CCO} changes.

In addition to degrading performance due to lack of tracking, a standard voltage regulator adds expense. It is not required to source the very small V_{REF} current load (~1 μ A typical value) and does not prevent V_{REF} noise.

Special DDR3 reference voltage regulators are designed to create V_{REF} voltages and track variations in V_{CCO} (e.g., Texas Instruments TPS51200). These voltage regulators can be used, but they can add unnecessary expense.

V_{REF} Noise Root Cause

Noise problems have the common attributes of an “aggressor” noise source, coupling mechanisms, and a so-called “victim” circuit. For SelectIO V_{REF} noise, the source of the noise is most frequently the switching frequencies (and harmonics) of the SelectIO interface switching activity.

Coupling mechanisms exist through the voltage rail and direct coupling to the V_{REF} trace leading to the FPGA V_{REF} pin.

The most insight into the root cause of V_{REF} noise comes from a more detailed look at the victim circuit, the V_{REF} input, in Figure 3. This more detailed view of the V_{REF} input shows some of the FPGA die and package parasitic elements.

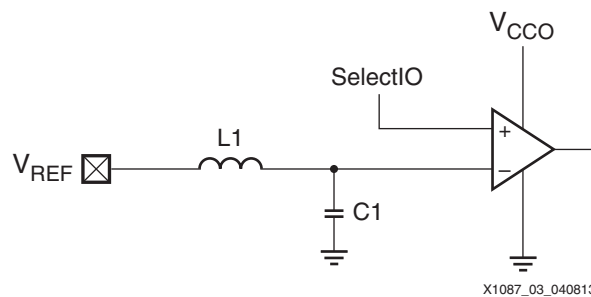


Figure 3: FPGA Die and Package Parasitic Elements on the V_{REF} Input

L1 is the package inductance from FPGA ball to die and varies significantly across package types (e.g., wire bond CSG and flip-chip FFG packages). L1 also varies from pin to pin. C1 is the die input capacitance, which has some variation across FPGA process nodes. The value of L1 can be obtained from the package files, and C1 from the RLGIC IBIS models. For purposes of illustration, Table 1 shows a selection of values for some V_{REF} pins in the 7 series XC7VX485T-FFG1761 device on the 28 nm process node in a flip-chip package.

Table 1: Representative L1 and C1 Values for Some V_{REF} Pins on XC7VX485t-FFG1761

Pin	Net	Type of SelectIO	L1 (nH)	C1 (pF) (HP SelectIOs) ⁽¹⁾
B18	IO_L6N_T0_VREF_38	HP ⁽²⁾	6.9	4.67
L11	IO_L19N_T3_VREF_39	HP	3.8	4.67

Notes:

1. The average die capacitance for HR SelectIO on 7 series devices on the 28 nm node is ~7.5 pF.
2. High performance.

In addition, PCB construction contributes small amounts of additional stray inductance and capacitance from via construction, PCB stack-up, and ground clearance topologies (typical values are ~½ nH and ~1 pF, respectively).

Neglecting these small additional PCB contributions, L1 and C1 form a resonant victim circuit. Any small, sustained, input signal with frequencies near the resonance defined by L1 and C1

excite that resonance and build up large voltage amplitudes limited only by small resistive parasitic components embedded in the largely reactive structure. This resonant behavior of L1 and C1 is the root cause of excessive V_{REF} noise.

Typical Victim Resonant Frequencies

Table 2 shows typical resonant frequencies at representative V_{REF} pins in the XC7VX485T-FFG1761 device. The resonant frequency for an LC circuit is $1/(2\pi(LC)^{1/2})$.

Table 2: Typical Resonant Frequencies at Some Representative V_{REF} Pins on XC7VX485T-FFG1761

Pin	Net	Type of SelectIO	L1 (nH)	C1 (pF) (HP SelectIO)	Resonant Frequency (MHz)
B18	IO_L6N_T0_VREF_38	HP	6.9	4.67	887
L11	IO_L19N_T3_VREF_39	HP	3.8	4.67	1195

The resonant frequency of ~800 MHz is the most troublesome. DDR3 interfaces run at rates with rich frequency content near this frequency. For example, DDR1600 is a common interface rate with a base clock rate at 800 MHz, very close to the victim resonant frequency of 887 MHz for the V_{REF} pin B18, as shown in Table 2. A substantial amount of energy can be coupled to the victim resonant circuit, creating large amounts of V_{REF} noise.

Another application area that can see V_{REF} noise generation is the area of high-speed LVDS interfaces. These interfaces can run in the range of 1.2 Gb/s to 1.5 Gb/s. There is a significant frequency content at the base clock frequency and at 3x the base clock frequency (third harmonic frequency). An 800 Mb/s DDR interface would have third harmonic content at 1.2 GHz. From Table 2, these LVDS DDR interfaces could see V_{REF} noise build up.

Design-to-Design Variation

The discussion to this point has identified several variables that contribute to the presence or absence of V_{REF} noise. Some of these variables, such as SelectIO switching frequencies, package parasitics (including pin-to-pin variations), and IC process parameters have variations between design generations that are not obvious. These variations lead to PCB circuits that provide quiet V_{REF} reference rails for one design and noisy V_{REF} pins in another design.

Optimal V_{REF} Circuit

This section discusses an example of an 887 MHz resonance on V_{REF} pin B18, assuming that a DDR3 interface is running at 1.6 Gb/s. One approach to minimizing V_{REF} noise is to attach a capacitor with minimum impedance at ~887 MHz to the V_{REF} pin. This capacitor should be physically placed as close as possible to the V_{REF} pin. Figure 4 shows the characteristics of such a capacitor.

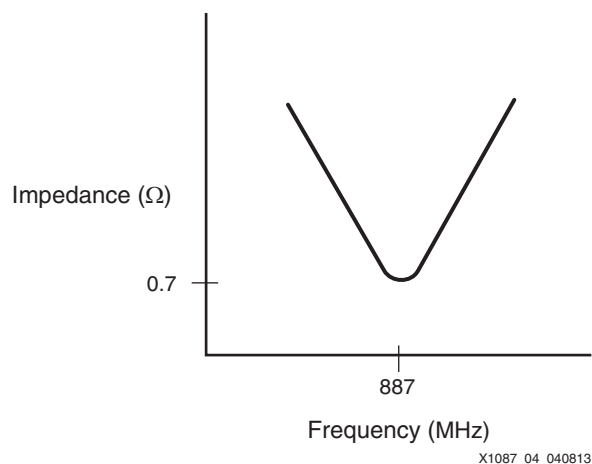


Figure 4: Impedance vs. Frequency Characteristics of the Murata (GRM033B11C151KA01) Capacitor

The 150 pF 0201 body size capacitor from Murata (GRM033B11C151KA01) shown in Figure 4 has very low impedance (0.7Ω) near ~ 887 MHz, the capacitor's self-resonant frequency. (Murata has an online tool that shows capacitor self-resonance and other capacitor characteristics at http://www.murata.com/products/design_support/simsurfing/index.html). Although this capacitor eliminates high-frequency noise near 887 MHz, the resonant frequency still exists and has been shifted to some other frequency. This shifted resonant frequency range could still be excited by some customer specific data pattern, potentially creating a difficult issue to debug. It would be possible to extend this approach with a series of capacitors with a range of capacitance values and a corresponding range of minimum impedances. However, it becomes impractical to physically locate the quantity of capacitors required close enough to the FPGA V_{REF} ball/pin.

The recommended circuit schematic is shown in Figure 5, and the corresponding physical layout is shown in Figure 6.

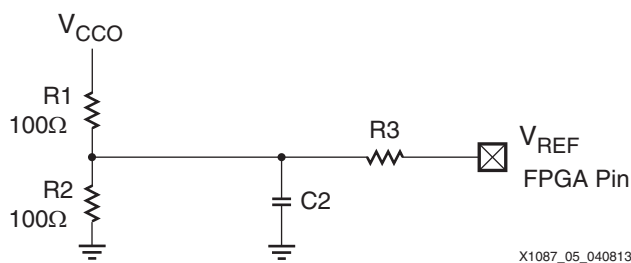
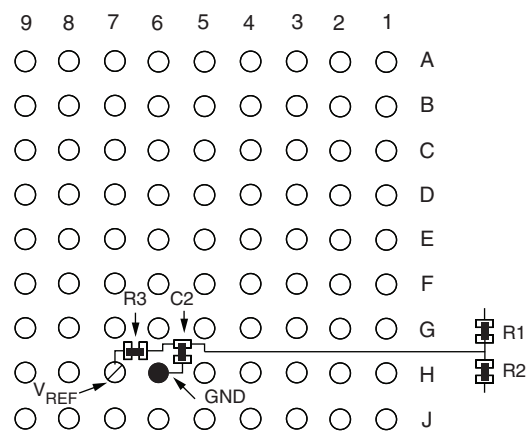


Figure 5: Recommended Circuit schematic for V_{REF}

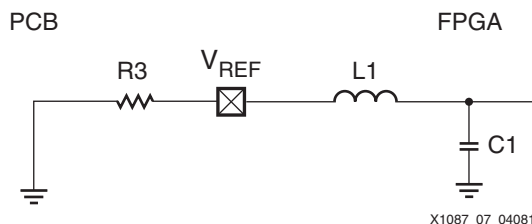


Zynq XC7Z020 CLG484
(Corner of Package - Bottom View)

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Figure 6: Recommended Physical Layout for V_{REF}

This circuit introduces resistive element R3 to dampen the reactive oscillations. Capacitor C2, being larger than C1, effectively shorts one end of R3 to ground at high frequency, inserting R3 into the reactive circuit composed of L1 and C1 internal to the FPGA. The circuit behavior at high frequency can be approximated by the circuit shown in Figure 7.



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Figure 7: V_{REF} Circuit Representation at High Frequency

A package with 0.8 mm ball pitch might cause the designer to avoid using some of the FPGA balls to make room for the 0201 discrete parts near the V_{REF} pin.

With the layout in place, the values of R3 and C2 can be tuned to fit the application. This circuit approximates a second order resonant circuit. R3 and C2 should be chosen so that the circuit is critically damped, or if that is not possible, overdamped. The underdamped condition should be avoided.

The value of R3 can now be chosen so that the circuit is critically damped. $R3 = 2 (L/C)^{1/2}$, in this case. For the V_{REF} pin B18 from the earlier example, $R3 = 2 \times (6.9 \text{ nH}/4.67 \text{ pF})^{1/2} = 77\Omega$.

The physical layout of this circuit is important. R3 and C2 need to be located physically as close as possible to the V_{REF} ball of the FPGA, as shown in Figure 7. Table 3 shows the component specifications to achieve critically damped characteristics on V_{REF} pins B18 and L11 on the XC7VX485T-FFG1761 device.

Table 3: Component Specifications for Critically Dampened Characteristics on V_{REF} Pins B18 and L11

Pin	Net	Type of SelectIO	L1 (nH)	C1 (pF) (HP SelectIO)	Resonant Frequency (MHz)	Critical Dampening Resistance R3 (Ω)
B18	IO_L6N_T0_VREF_38	HP	6.9	4.67	887	77
L11	IO_L19N_T3_VREF_39	HP	3.8	4.67	1195	57

Conclusion

As FPGA SelectIO pins increase in frequency, noise on V_{REF} pins occurs more frequently. An optimized V_{REF} generation circuit similar to the circuit presented in this application note provides protection from the issue of V_{REF} noise as SelectIO switching rates continue to improve.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/24/2013	1.0	Initial Xilinx release.

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