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CTLE Adaptation Logic for 7 Series FPGAs GTX Transceivers

Author: David Mahashin

Summary

The 7 series FPGA GTX receiver in DFE mode contains an automatic gain control (AGC) block and a continuous time linear equalizer (CTLE) block to compensate for channel loss. Both AGC and the CTLE wide-band gain stages aim to boost frequencies within the operating frequency range of the GTX transceiver to optimize the eye height of the received signal.

Although AGC is auto-adaptive, the CTLE wide-band stage is not. By default, the user adjusts the wide-band gain by analyzing the channel loss. For more information, see the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).

This application note introduces a module implemented in the FPGA logic for automatically adjusting CTLE wide-band gain. The one-time calibration is performed after deassertion of GTRXRESET, RXPMARESET, or RXDFELPMRESET.

By using this calibration module, the user is no longer required to perform channel analysis to set the CTLE wide-band gain. Furthermore, in cases where the channel connected to the GTX receiver might be dynamically changed, the module adjusts the wide-band gain to compensate for any difference in insertion loss, provided the appropriate reset is asserted.

The module is included in the 7 series FPGAs Transceivers Wizard design as an optional feature.

Design Overview

Figure 1 shows an RX datapath containing AGC and CTLE blocks.

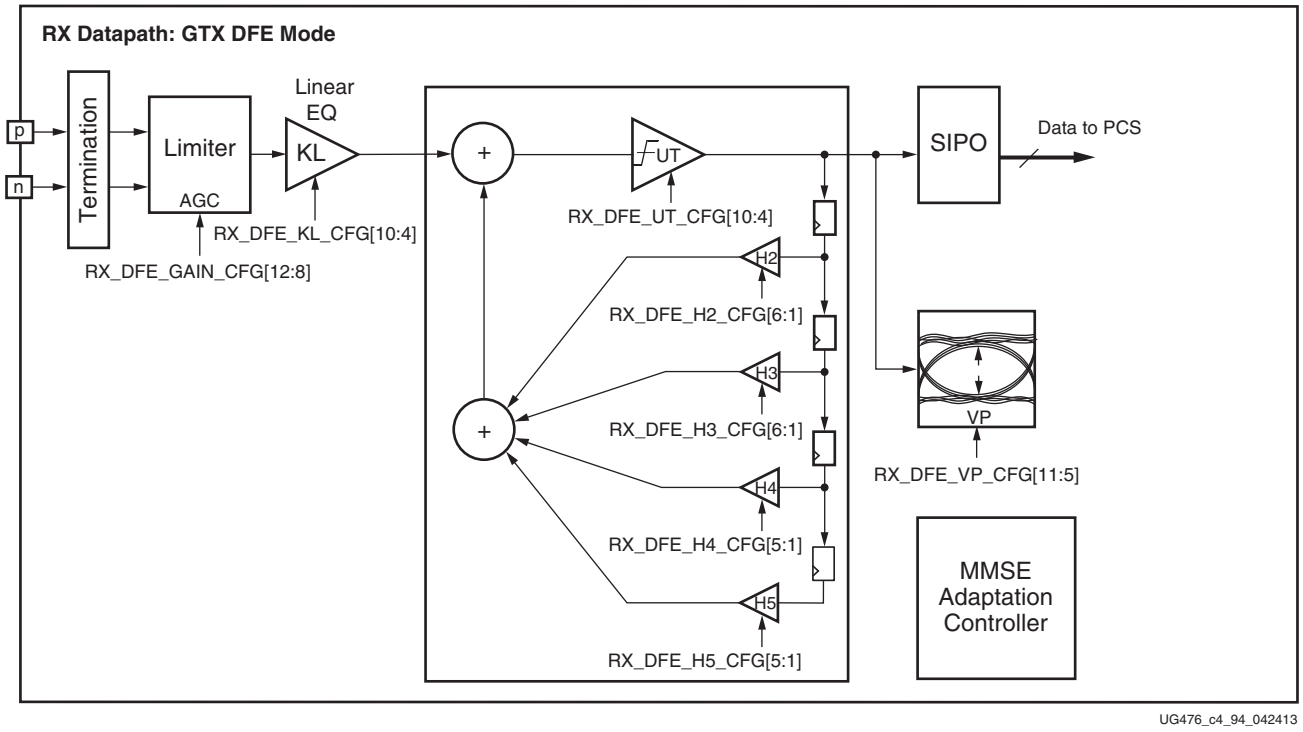

Figure 1: **GTX RX Datapath in DFE Mode**

The module adaptation logic adjusts the CTLE wide-band gain to keep the AGC from railing to its maximum or minimum value. If the signal at the receiver is highly attenuated, the maximum AGC gain might not be sufficient to open the eye. In this case, CTLE wide-band gain is steadily increased until AGC no longer saturates. Conversely, if the signal at the receiver is too large and AGC rails to its minimum value, CTLE wide-band gain is decreased to optimize internal signal swing. The one-time calibration process is performed after a GTRXRESET, RXPMARESET, or RXDFELPMRESET event. After the calibration process finishes, the wide-band gain value is held until the next time GTRXRESET, RXPMARESET, or RXDFELPMRESET is asserted. This calibration does not affect the lock time specification for clock recovery and adaptation loops (T_{DLOCK}). The signal at the RX pins must be stable for proper calibration.

The Wizard example design includes an optional module, `ctle_agc_comp`, that performs this described procedure. This option is available only for DFE mode.

Implementation Details

The adaptation state machine follows the flowchart shown in Figure 2. CTLE3 gain is adjusted only if AGC rails to its maximum or minimum value. The adaptation finishes if either of the following conditions are met:

- AGC does not reach its maximum or minimum value
- CTLE3 reaches its maximum or minimum value

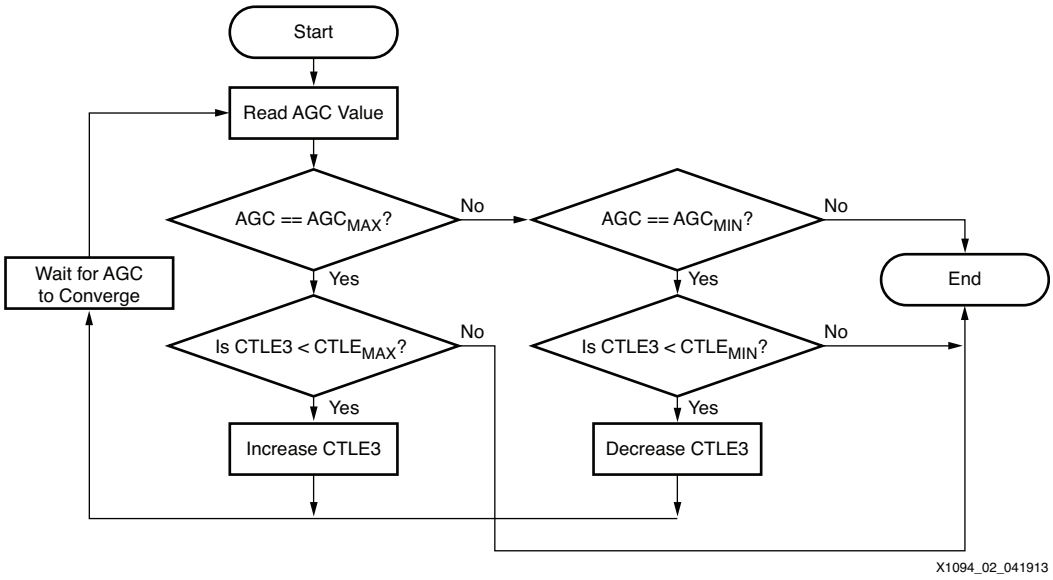

Figure 2: **Flowchart for CTLE3 Adaptation Logic**

Reference Design

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=344046

The module design is currently incorporated in the Wizard example design. Table 1 shows the reference design checklist. The FPGA resources used depend on the options selected in the Wizard menu.

Table 1: **Reference Design Checklist**

Parameter	Description
General	
Developer name	Xilinx
Target devices	7 series devices with GTX transceivers
Source code provided	Yes
Source code format	Verilog
Design uses code or IP from existing Xilinx application note or reference designs, CORE Generator™ software, or third party	No
Simulation	
Functional simulation performed	Yes
Timing simulation performed	Yes
Testbench used for functional and timing simulations	No
Testbench format	NA

Table 1: **Reference Design Checklist *(Cont'd)***

Parameter	Description
Simulator software/ version used	Synopsys VCS 2009.06
SPICE/IBIS simulations	No
Implementation	
Synthesis software tools/version used	XST 14.1 Vivado® tools 2013.2
Implementation software tools/versions used	ISE® Design Suite 14.1 Vivado tools 2013.2
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	KC724 board

Conclusion

The CTLE adaptation logic presented in the application note automatically adjusts the CTLE3 wide-band stage by monitoring the AGC value. This feature allows dynamic adjustment of the equalizer gain without requiring channel-loss analysis.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
11/18/2013	1.0	Initial Xilinx release.

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