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SMPTE 2022-5/6/7 High Bit Rate Media Transport over IP Networks with Forward Error Correction and Seamless Protection Switching on Kintex UltraScale FPGAs

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Summary

This application note covers the design considerations of a Video over IP network system using the performance features of the LogiCORE™ IP SMPTE 2022-5/6 Video over IP transmitter and receiver cores. The design focuses on high bit rate native media transport over 10 Gb/s Ethernet with a built-in forward error correction engine and SMPTE 2022-7 seamless protection switching. The design is able to support up to three SD/HD/3G-SDI streams.

The reference design has two platforms: the transmitter platform and the receiver platform. The transmitter platform design uses three LogiCORE SMPTE UHD-SDI cores to receive the incoming SDI video streams. The received SDI streams are multiplexed and encapsulated into fixed-size datagrams by the SMPTE 2022-5/6 video over IP transmitter core and sent out through two LogiCORE IP 10-Gigabit Ethernet MAC. The 10-Gigabit link is supported by two LogiCORE IP 10-Gigabit Ethernet PCS/PMA using an optical cable connected to the receiver end. On the receiver platform, the Ethernet datagrams are collected at the 10-Gigabit Ethernet MAC. The SMPTE 2022-5/6 video over IP receiver core filters the datagrams, de-encapsulates and de-multiplexes the datagrams into individual streams which are output through the SMPTE SDI cores. The Ethernet datagrams are buffered in DDR4 SDRAM memory for both the transmitter and receiver. The DDR traffic passes through the AXI interconnect to the AXI UltraScale™ memory controller. A MicroBlaze™ processor is included in the design to initialize the cores and read the status.

The reference design targets the Xilinx Kintex®UltraScale FPGA KCU105 evaluation kit, which uses the Kintex UltraScale XCKU040-2FFVA1156 FPGA, and an inrevium TB-FMCH-3GSDI2A FMC board. See the Kintex UltraScale FPGA KCU105 Evaluation Kit [Ref 1], inrevium TB-FMCH-3GSDI2A board [Ref 2] for details.

Reference Design

Included Systems

The reference design was created and built using the Vivado® Design Suite, System Edition 2015.1. The design also includes software built using the Xilinx Software Development Kit (SDK) 2015.1. The software runs on the MicroBlaze processor subsystem and implements control and status functions. Complete project files for Vivado Design Suite and the SDK are provided with this application note to allow examination and rebuilding of the design or to use it as a template for starting a new design.

Hardware

Introduction

The reference design is built around the SMPTE 2022-5/6 video over IP transmitter and receiver cores and leverages existing Xilinx IP cores to form the complete system. The input and output of the system are SDI video streams. The system consists of two platforms. The transmitter and receiver cores each reside in separate platforms. An optical cable connects the two platforms simulating an IP network. See Figure 1.

The SMPTE UHD-SDI cores have been configured to allow the video over IP cores to receive and transmit SD/HD/3G-SDI streams while the 10-Gigabit Ethernet MAC and 10-Gigabit Ethernet PCS/PMA enable the video over IP cores to transfer SDI data in the Ethernet medium. Although the UHD-SDI core supports up to 12G-SDI, the current SMPTE 2022-5/6 only specifies and supports up to 3G-SDI. See Figure 2 and Figure 3.

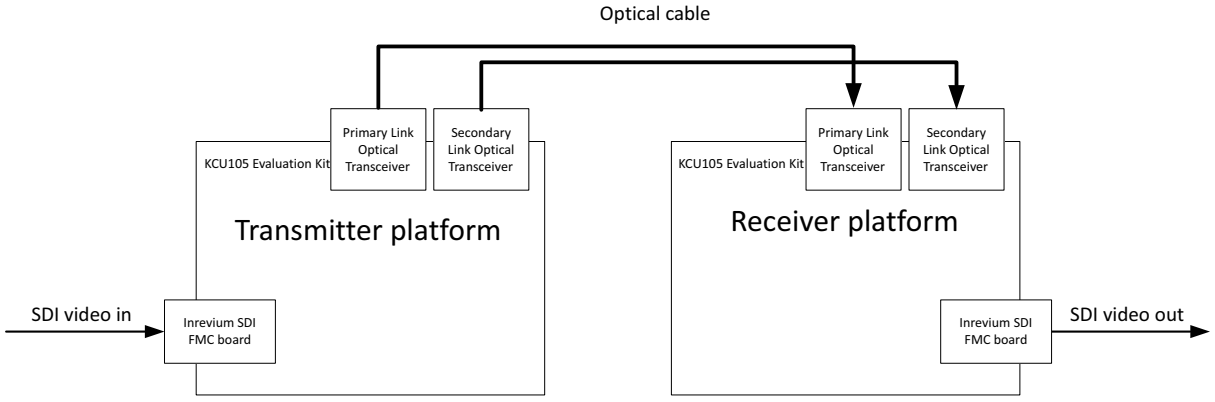

Figure 1: **Block Diagram of the Video over IP FPGA**

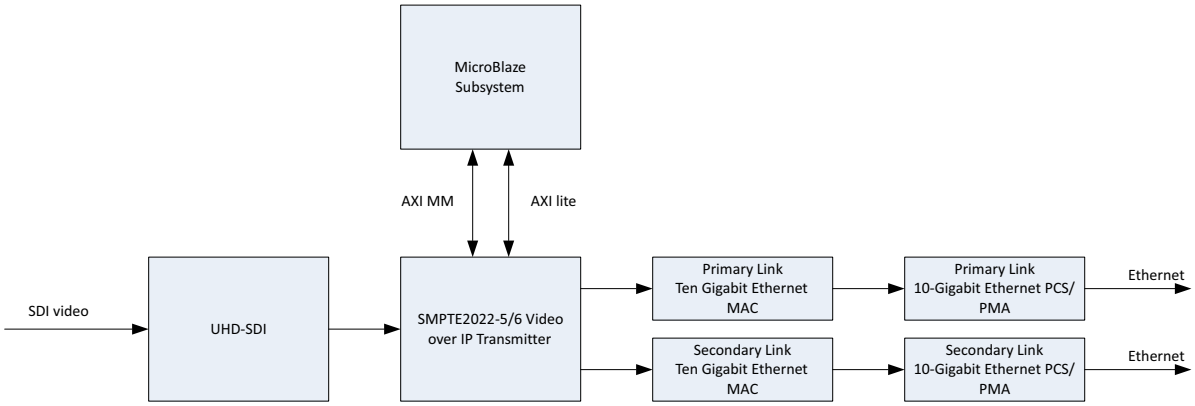

Figure 2: **Block Diagram of the Video over IP Transmitter FPGA**

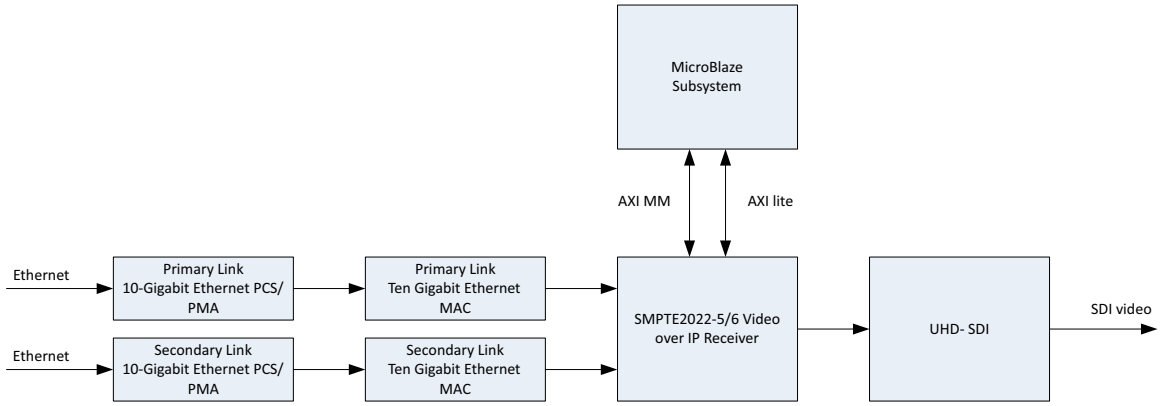

Figure 3: **Block Diagram of the Video over IP Receiver FPGA**

Other than managing the SDI streams, encapsulation and de-encapsulation, the transmitter and receiver cores include forward error correction (FEC) and seamless protection switching features. FEC protects the video stream during the transport of high-quality video over IP networks. With FEC, the transmitter adds systematically generated redundant data to its video. This redundancy allows the receiver to detect and correct a limited number of packet errors occurring anywhere in the video without the need to ask the transmitter for additional video data. These errors, in the form of lost video packets, result from a variety of causes ranging from thermal noise to storage system defects and transmission noise introduced by the environment. FEC gives the receiver the ability to correct these errors without needing a reverse channel to request retransmission of data. Seamless protection switching allows transmission and reception of two identical streams over potentially diverse path to add more reliability to the system. The receiver handles the seamless switching datagram by datagram without impacting the content or the stream. These features can be enabled using the core registers.

High-level control of the system is provided by a simplified MicroBlaze embedded processor subsystem containing I/O peripherals and processor support IP. A clock generator block and a processor system reset block supply clock and reset signals for the system, respectively. An AXI4 interconnect and an AXI4 memory interface generator (MIG) is instantiated in the subsystem allowing the video over IP cores access to the on-board DDR4 SDRAM. See Figure 4 and Table 1 for a block diagram of the MicroBlaze processor subsystem and its address map.

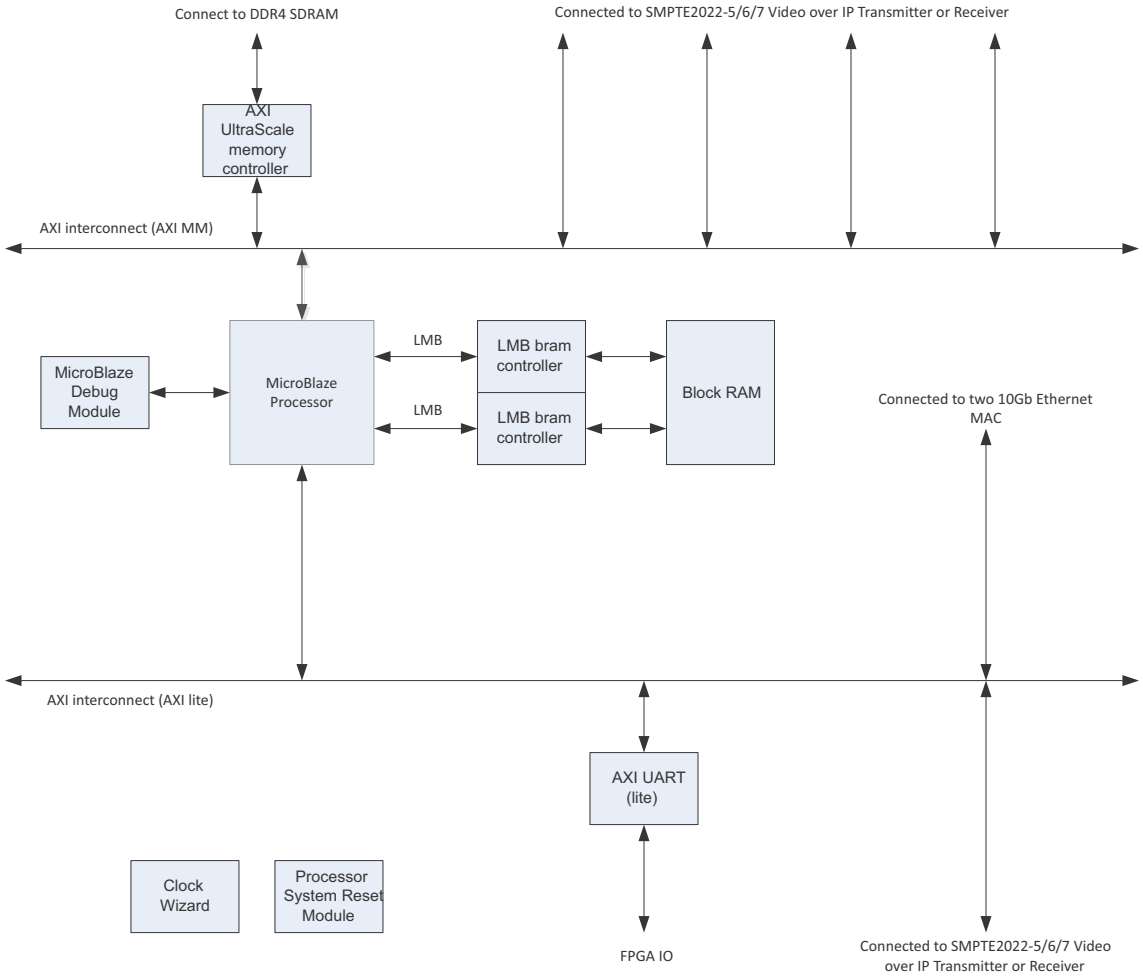

Figure 4: **Block Diagram of the MicroBlaze Subsystem in the Reference Design**

Table 1: **MicroBlaze Subsystem Address Map**

Peripheral	Instance	Base Address	High Address
lmb_bram_if_cntlr	ilmb_bram_if_cntlr	0x00000000	0x0001FFFF
lmb_bram_if_cntlr	dlmb_bram_if_cntlr	0x00000000	0x0001FFFF
mig_ultrascale	mig_1	0xC0000000	0xFFFFFFFF
axi_uartlite	axi_uartlite_1	0x40600000	0x4060FFFF
external axilite_interface	smpte2022_axilite	0x70E00000	0x70E0FFFF
external axilite_interface	ten_gig_eth_mac1_axilite	0x7C400000	0x7C400FFF
external axilite_interface	ten_gig_eth_mac2_axilite	0x7C500000	0x7C500FFF

Reference Design Specifics

In addition to the SMPTE 2022-5/6 Video over IP Transmitter and Receiver cores, the reference design includes the following cores:

- AXI interconnect
- MicroBlaze
- MicroBlaze Debug Module
- Local Memory Bus
- LMB BRAM Controller
- Block Memory Generator
- Clocking Wizard
- Processor System Reset
- AXI UARTLite
- Memory Interface Generator
- SMPTE UHD-SDI
- Ten Gigabit Ethernet MAC
- Ten Gigabit Ethernet PCS/PMA

Hardware System Specifics

This section describes the high-level features of the reference design, including how the main IP blocks are configured.

Video over IP System

The reference design implements the SMPTE 2022-5/6 video over IP cores as modules for broadcast applications that require bridging between broadcast connectivity standards (SD/HD/3G-SDI) and a 10-Gigabit Ethernet network. The cores are intended for developing Internet protocol-based systems to reduce the overall cost in broadcast facilities for distribution and routing of audio and video data. The SDI data to be transported are mapped into media datagram payloads as per SMPTE 2022-6. The systematically-generated redundant forward error correction datagrams are formatted according to SMPTE 2022-5. IP/UDP/RTP protocols provide standard headers when transporting the media and FEC datagrams over the IP network. The SMPTE 2022-5/6 datagrams are transmitted twice through two 10-Gigabit Ethernet MACs for seamless protection switch according SMPTE 2022-7.

To support the system functions correctly, the bandwidth available in the network must meet or exceed what is required to support the stream generated by the system. The overhead required for media datagram generation is approximately 5% due to the IP/UDP/RTP and SMPTE 2022-6 headers.

SMPTE 2022-5/6 Video over IP Transmitter

The SMPTE 2022-5/6 video over IP transmitter in the reference design is configured to accept three channels of SDI input from the SMPTE UHD-SDI receiver. The transmitter connects to two 10-Gigabit Ethernet MAC via two AXI4-Stream data interface. The transmitter also connects to MicroBlaze subsystem via an AXI4-Lite control interface. The transmitter core uses two AXI4 external master connectors to access the DDR4 SDRAM via the AXI4 interconnect. The memory map address range is fixed at 0xC0000000 - 0xFFFFFFFF.

The transmitter source MAC addresses for primary and secondary links are set to 0x000000000000AA and 0x000000000000CC respectively. The transmitter source IP address for primary and secondary links are set to 192.168.0.50 and 192.168.1.50 respectively and the destination IP address for primary and secondary links are set to 192.168.1.100 and 192.168.1.100 respectively. The UDP ports are configured as shown in Table 2. The FEC matrix sizes set for the channels are in Table 3. These parameters are configurable through the registers.

Table 2: **UDP Ports Values for the 3 SDI Channels**

BNC connector	Channel	Source UDP port	Destination UDP port
RX1	0	0x10	0x10
RX2	1	0x20	0x20
RX3	2	0x30	0x30

Table 3: **FEC Matrix Size Values for the 3 SDI Channels**

BNC connector	Channel	L	D
RX1	0	77	77
RX2	1	77	77
RX3	2	77	77

The SMPTE 2022-5/6 video over IP transmitter contains an AXI4-Lite interface which allows dynamic control of the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter v4.0 Product Guide* [Ref 4].

The registers are categorized into 2 sections, the general space and channel space. The parameters in the general space apply to all the channels. The channel space register is further divided into two sections where the parameters are set based on either the respective links and channel or the respective channel only. In this reference design, three channels are supported and all of the parameters are differentiated by the UDP destination port and the primary and secondary links are differentiated by the IP Address. See Software Application, page 10 for details.

For the general registers, normal address read and writes access is applied. For the Channels registers, observe the following steps to update the registers.

1. Set the channel to be configured at register address, base_addr+0x00C.
2. Configure the channel specific register.

3. Pulse REG_UPDATE bit of the CONTROL register to commit the channel registers change.
4. Repeat steps 1-3 for another channel or registers. See Figure 5.

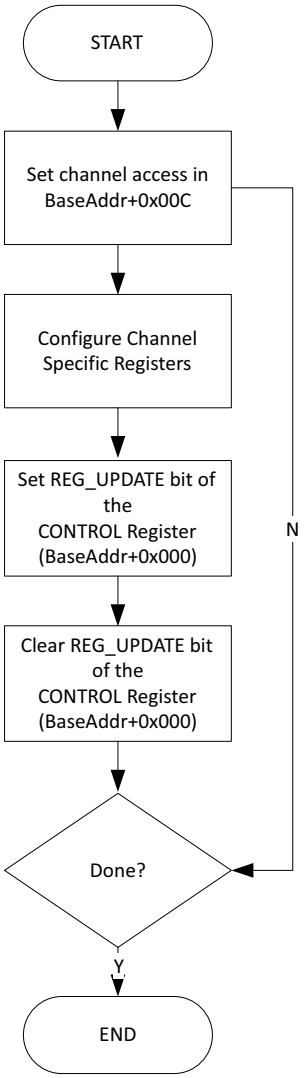

Figure 5: **Channel Register Configuration Flow Chart**

SMPTE 2022-5/6 Video over IP Receiver

The SMPTE 2022-5/6 video over IP receiver in the reference design is configured to stream three channels of SDI output to the SMPTE UHD-SDI transmitters. The receiver connects to two 10-Gigabit Ethernet MAC through two AXI4-Stream data interface. The receiver also connects to the MicroBlaze processor subsystem via an AXI4-Lite control interface. The receiver core uses two AXI4 external master connectors to access the DDR4 SDRAM via an AXI4 interconnect. The memory map address range is fixed at 0xC0000000-0xFFFFFFFF.

The incoming media packets are filtered based on the UDP destination ports, as shown in Table 4.

Table 4: **UDP Ports Values for the 3 SDI Channels**

BNC connector	Channel	Destination UDP port
TX1	0	0x10
TX2	1	0x20
TX3	2	0x30

The SMPTE 2022-5/6 video over IP receiver contains an AXI4-Lite interface which allows users to dynamically control the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver v5.0 Product Guide* [Ref 5].

The registers are categorized into two sections, the general space and the channel space. The parameters in the general space apply to all of the channels. The parameters in the channel space apply to an individual channel.

For the general registers, normal address read and writes access is applied. For the Channels registers, observe the following steps to update the registers.

1. Set the channel to be configured at register address, base_addr+0x00C.
2. Configure all the channel registers of interest for the particular channel.
3. Pulse bit 1 of register address, base_addr+0x000, to commit the channel registers change.
4. Repeat steps 1-3 for another channel. See Figure 5.

SMPTE UHD-SDI

The SMPTE UHD-SDI core has been configured to provide transmitter and receiver interfaces for SMPTE SD-SDI, HD-SDI, and 3G-SDI standards. The core is connected to UltraScale FPGA GTH transceivers for serialization and deserialization of the SDI video streams. Although the UHD-SDI core supports up to 12G-SDI, the current SMPTE 2022-5/6 only specifies and supports up to 3G-SDI. The SMPTE SDI receiver uses a 148.5 MHz GTX transceiver reference clock frequency to receive its supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTX transceiver appropriately for that SDI mode. The SMPTE SDI transmitter requires two different GTH transceiver reference clock frequencies for its supported SDI bit rates. 148.5 MHz and 148.35 MHz are used in the design. The clock multiplexer built into the GTH transceiver switches between these two reference clocks. A port dynamically controls the operating SDI mode for the transmitter. The transmitter, in turn, controls the GTH transmitter through the DRP to provide the appropriate configuration for each SDI mode. See the *LogiCORE IP SMPTE UHD-SDI v1.0 Product Guide* [Ref 6] and *Implementing SMPTE SDI Interfaces with UltraScale GTH Transceivers* [Ref 11] for more information.

Ten Gigabit Ethernet MAC

The 10-Gigabit Ethernet MAC instances on the transmitter side has the AXI4-Stream transmit interfaces connected to the output of the SMPTE 2022-5/6 video over IP transmitter. The 10-Gigabit Ethernet MAC instances on the receiver side has the AXI4-Stream receive interfaces

connected to the input of the SMPTE 2022-5/6 video over IP receiver. A 64-bit SDR PHY port is configured in the 10-Gigabit Ethernet MAC to interface to the 10-Gigabit Ethernet PCS/PMA cores. No flow control is used. See the *LogiCORE IP 10-Gigabit Ethernet MAC v14.0 Product Guide* [Ref 7] for more information.

Ten Gigabit Ethernet PCS/PMA

The Ten Gigabit Ethernet PCS/PMA cores create 10GBASE-R optical link between the video over IP transmitter and receiver. Each PCS/PMA uses one transceiver to achieve a 10 Gb/s data rate. An optical cable is connected between the SFP+ optical transceivers on both sides. The PCS/PMA 10GBASE-R/KR standard is fully specified in clauses 45, 49, 72, 73, and 74 of the 10-Gigabit Ethernet IEEE 802.3-2008 specification. See the *LogiCORE IP 10-Gigabit. Ethernet PCS/PMA v5.0 Product Guide* [Ref 8] for more information.

AXI Interconnect (AXI_MM)

This AXI4 interconnect instance (AXI_MM) provides the high FMAX and throughput for the design with a 256-bit core data width and a 200 MHz clock frequency for its slave interfaces. The AXI4 interconnect core master interface data width and clock frequency match the capabilities of the attached AXI4 MIG to optimize the dataflow. Setting the AXI4 interconnect core data width and clock frequency below the native width and clock frequency of the memory controller creates a bandwidth bottleneck within the system. To help meet the timing requirements of a 256-bit AXI4 interface at 200 MHz, a rank of register slices are enabled both at the master and slave interfaces of the interconnect. Together, the AXI4 interconnect and AXI4 MIG form a 4-port AXI4 MPMC connected to four AXI4 external master connectors. The configuration of this AXI4 interconnect is consistent with the system performance optimization recommendations for an AXI4 MPMC-based system as described in the *AXI Reference Guide* [Ref 9].

Memory Interface Generator

The Memory Interface Generator (MIG) forms the single slave connected to the AXI4 Interconnect. The MIG AXI4 interface is 512 bits wide, runs at 250 MHz, and disabled narrow burst support for optimal throughput and timing. This configuration matches the native AXI4 interface clock and width corresponding to a 64-bit DDR4 DIMM with 1000 MHz memory clock. Register slices are enabled to ensure that the interface meets timing at 250 MHz. These settings help ensure that a high degree of transaction pipelining is active to improve system throughput. See the *LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions v5.0* (PG150) [Ref 10]for more information about the memory controller.

AXI Interconnect (AXI4-Lite)

The MicroBlaze processor data peripheral (DP) interface master writes and reads to all AXI4-Lite slave registers in the design for control and status information. These interconnects are 32 bits and do not require high FMAX and throughput. Therefore, they are connected to a slower FMAX portion of the design by a separate AXI Interconnect. The AXI4-Lite Interconnect block is configured for shared-access mode because high throughput is not required in this portion of the design. Therefore, area can be optimized over performance on this interconnect block. Also,

this interconnect is clocked at 100 MHz to ensure that synchronous integer ratio clock converters in the AXI Interconnect can be used, which offer lower latency and less area than asynchronous clock converters. The slaves on the AXI4-Lite Interconnect are AXI UART (lite) and customized axilite_bridge IP to the Ten Gigabit Ethernet MAC and SMPTE 2022-5/6 Video over IP Transmitter or Receiver cores.

Software Application

The software application initializes the video over IP TX and RX systems respectively. After the software initialization, commands can be selected from the menu at the UART display.

Application-level software and the drivers for controlling the system are written in C. Alternatively, drivers and application software can be written directly to the IP control registers.

The software configures the register values as shown in Table 5 and Table 6. The base address of the register set is the AXI4-Lite bridge base address (0x70E00000). Registers not shown in the tables are not initialized and remain at their respective default values.

Table 5: **Initialized VoIP TX Register Values**

Offset	Register Name	Value		
General Space				
0x010	Primary Mac Address (Low)	0x000000AA		
0x014	Primary Mac Address (High)	0x00000000		
0x018	Secondary Mac Address (Low)	0x000000CC		
0x01C	Secondary Mac Address (High)	0x00000000		
0x028	Memory Base Address 3-MSb	0x00000006		
0x030	hitless_config	0x00000000		
Primary Channel Space		Ch1	Ch2	Ch3
0x080	ip_header	0x00006480		
0x084	vlan_tag_info	0x0000AB00	0x0000AB10	0x0000AB20
0x088	dest_mac_low_addr	0x000000FF		
0x08C	dest_mac_high_addr	0x00000000		
0x090	dest_ip_host_low_addr	0xC0A80064		
0x0A0	src_ip_host_low_addr	0xC0A80032		
0x0B0	udp_src_port	0x10	0x20	0x30
0x0B4	udp_dest_port	0x10	0x20	0x30
0x0D0	transmit_en	0x1		
0x0D8	ip_header_fec	0x00006480		
0x100	chan_en	0x1		
0x110	video_para_config	0x1		
0x118	ssrc	0x12345600	0x12345610	0x12345620
0x11C	FEC_config	0x6		

Table 5: **Initialized VoIP TX Register Values *(Cont'd)***

Offset	Register Name	Value		
0x124	FEC_L	0x4D		
0x128	FEC_D	0x4D		
Secondary Channel Space		Ch1	Ch2	Ch3
0x084	vlan_tag_info	0x0000AB00	0x0000AB10	0x0000AB20
0x088	dest_mac_low_addr	0x000000EE		
0x08C	dest_mac_high_addr	0x00000000		
0x090	dest_ip_host_low_addr	0xC0A80164		
0x0A0	src_ip_host_low_addr	0xC0A80132		
0x0B0	udp_src_port	0x10	0x20	0x30
0x0B4	udp_dest_port	0x10	0x20	0x30
0x0D0	transmit_en	0x1		
0x0D8	ip_header_fec	0x00006480		

Table 6: **Initialized VoIP RX Register Values**

Offset	Register Name	Value		
General Space				
0x028	network_path_differential	0x00149970		
0x034	fec_buf_base_addr	0xD8000000		
0x038	fec_buf_pool_size	0x0457b000		
Primary Channel Space		Ch1	Ch2	Ch3
0x088	match_vlan	0x0000AB00	0x0000AB10	0x0000AB20
0x08C	match_dest_ip_addr	0xC0A80064		
0x09C	match_src_ip_addr	0xC0A80032		
0x0AC	match_src_port	0x10	0x20	0x30
0x0B0	match_dest_port	0x10	0x20	0x30
0x0B4	match_sel	0x10		
0x100	chan_en	0x1		
0x110	match_ssrc	0x12345600	0x12345610	0x12345620
0x11C	playout_delay	0x002932E0		
0x12C	media_buf_base_addr	0xC0000000	0xC8000000	0xD0000000
0x130	media_pkt_buf_size	0x0000FFFF		
Secondary Channel Space		Ch1	Ch2	Ch3
0x088	match_vlan	0x0000AB00	0x0000AB10	0x0000AB20
0x08C	match_dest_ip_addr	0xC0A80164		
0x09C	match_src_ip_addr	0xC0A80132		
0x0AC	match_src_port	0x10	0x20	0x30

Table 6: **Initialized VoIP RX Register Values *(Cont'd)***

Offset	Register Name	Value		
0x0B0	match_dest_port	0x10	0x20	0x30
0x0B4	match_sel	0x10		

Software Process Flow

Reference Design for SMPTE 2022-5/6 TX and RX uses software flow as shown in Figure 6.

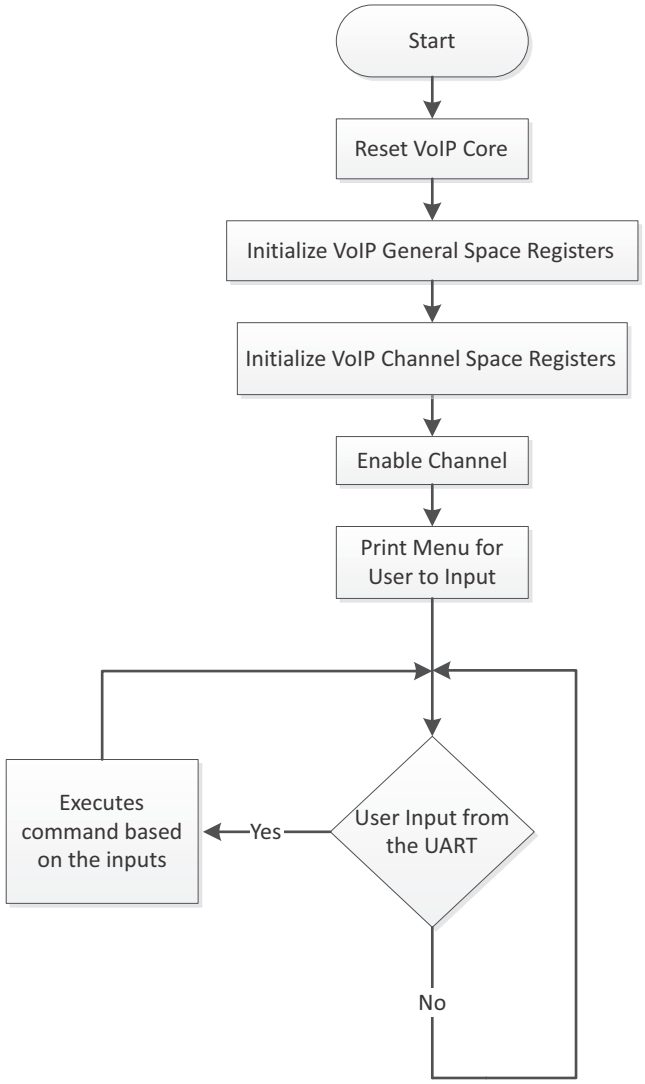

Figure 6: **Video over IP Transmitter and Receiver Overall Software Process**

Note: Channel enable is asserted last to ensure proper core operation after reset.

To perform software reset while the core has been configured and running, follow steps as shown in Figure 7.

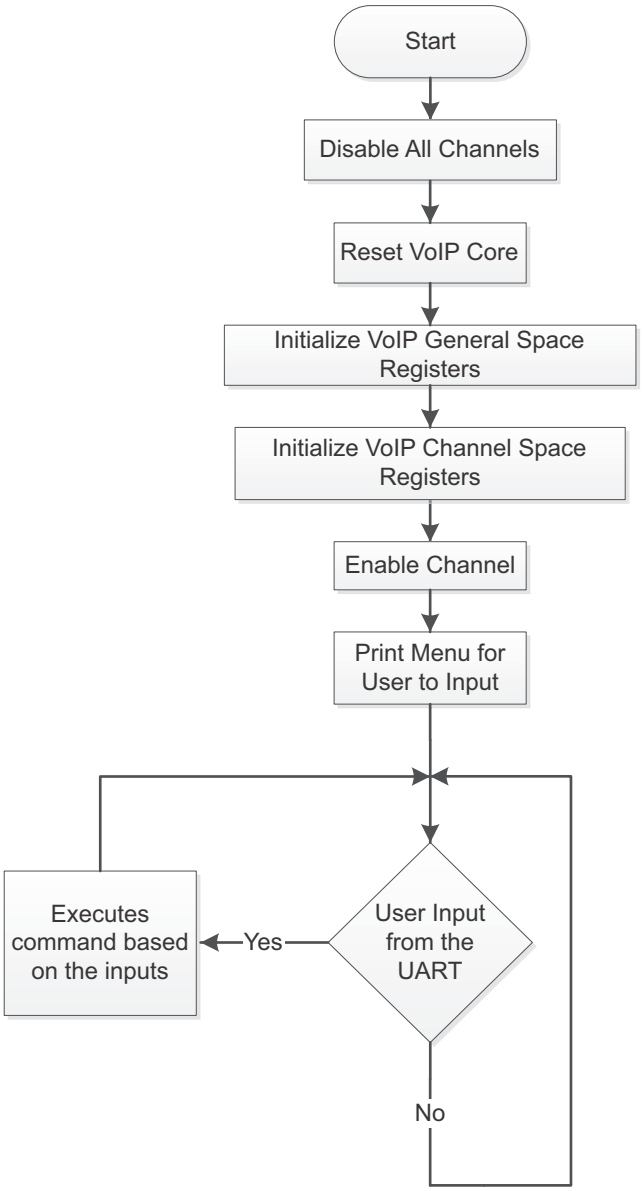

Figure 7: **Video over IP Transmitter and Receiver Software Reset Process**

Note: Channel Reset can be performed by setting bit-0 to low at chan_en register (register offset 0x100).

Note: The core is able to support changes of video stream (without performing channel reset) if the Video Format meets the register setting configured as stated in the *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver v4.0 Product Guide* [Ref 5], Memory Requirement and Register Configuration section.

Tool Flow and Verification

The following checklist indicates the tool flow and verification procedures used for the provided reference design.

Table 7: **Reference Design Checklist**

Parameter	Description
General	
Developer Name	Gilbert Magnaye, Ilias Ibrahim
Target Devices	Kintex UltraScale FPGA
Source code provided?	Yes
Source code format (if provided)	VHDL and Verilog
Design uses code or IP from existing reference design, application note, 3rd party or Vivado software? If yes, list.	Cores generated from Vivado IP Catalog
Simulation	
Functional simulation performed	N/A
Timing simulation performed?	N/A
Test bench provided for functional and timing simulation?	N/A
Test bench format	N/A
Simulator software and version	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/versions used	Vivado 2015.1
Implementation software tool(s) and version	Vivado 2015.1
Static timing analysis performed?	Yes
Hardware Verification	
Hardware verified?	Yes
Platform used for verification	Xilinx Kintex UltraScale FPGA KCU105 Evaluation

Requirements

Hardware

The hardware requirements for this reference system are:

- Two Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kits
- Two Inrevium 3G-SDI Boards (TB-FMCH-3GSDI2A)
- Two SFP+ Optical Transceiver
- Optical Cable

Software

This section includes any software requirements. Could include:

- Vivado Design Suite 2015.1
- Software Development Kit (SDK) 2015.1
- Software Terminals (for example, Tera Term, HyperTerminal or PuTTY)

Reference Design Files

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=391782, registration required.

Figure 8 shows the reference design directory structure.

IMPORTANT: *The reference design should be unzipped close to root. See Building Hardware.*

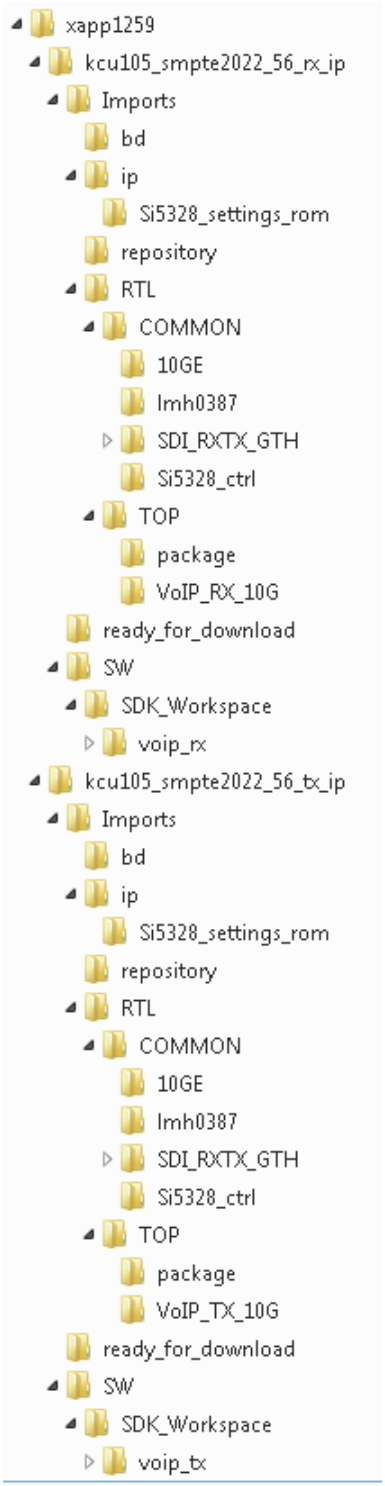

Figure 8: **Reference Design Directory Structure**

The two main directories in xapp1259.zip are kcu105_smpte2022_56_tx_ip and kcu105_smpte2022_56_rx_ip. Both have the same directory structure which is described in Figure 9.

```
    | add_hdl.TCL: TCL for importing package RTL into the project
    | all.TCL: TCL for building and compiling reference design package
    | hw_bldr_utils.TCL: Contains utility functions for building the project
    | ip.TCL: TCL for generating Xilinx IPs which are instantiated in the project
    | ipi_utils.TCL: Contains IPI specific utility functions for building the project
    | proj.TCL: Creates Vivado project and adds "repository" folder into project local
   repository
   | rsb.TCL: TCl for constructing IPI subsystem by calling system_basic.TCL in Imports\bd
   folder
   |
   \Imports
   |
   |-------\bd: Contains files for IPI subsystem construction
   |-------\ip: Contains configuration files for Xilinx IP
   |-------\repository: Contains non-Xilinx standard IPs (empty for this reference design)
   |-------\RTL:
   |-------------\COMMON: Contains 10G MAC, UHD-SDI, LMH0387 controller and Si5328
   Controller source file
   |-------------\TOP: Contains project package, top level and xdc files.
   |
   \ready_for_download: Contains "bit" file of the system.
   |
   |
   \SW
   |

|-------\SDK_Workspace: Contains source code of VoIP transmitter application.
```

Figure 9: **kcu105_smpte2022_56_tx_ip and kcu105_smpte2022_56_rx_ip**

Licensing

Ensure that the licenses for the SMPTE 2022-5/6 Video over IP Transmitter and Receiver cores, 10-Gigabit Ethernet PCS/PMA and Ten Gigabit Ethernet MAC are installed.

Reference Design Steps

Setup

This reference design runs on the KCU105 and TB-FMCH-3GSDI2A boards shown in Figure 10 and Figure 11.

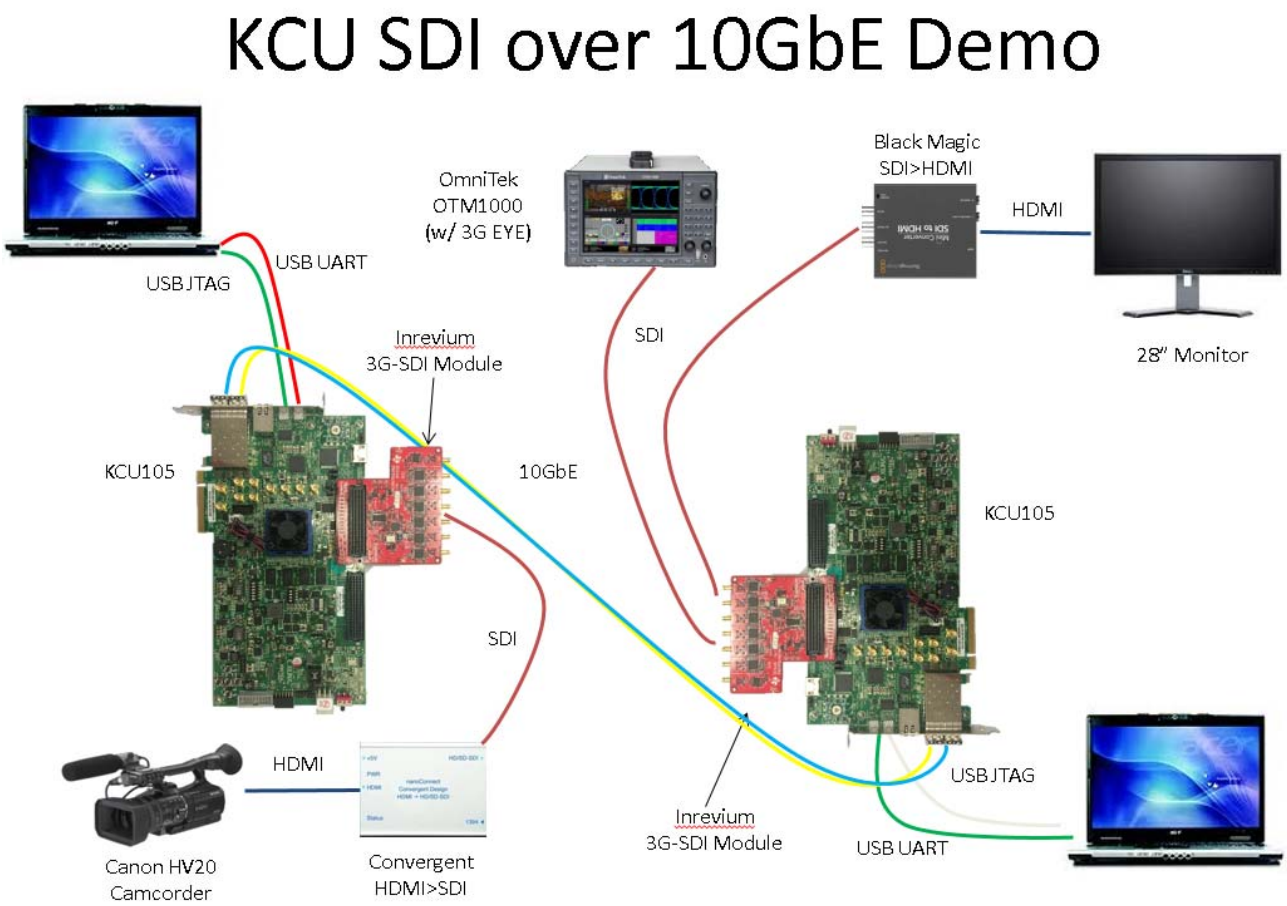

Figure 10: **SMPTE 2022-5/6/7 Demo System Setup**

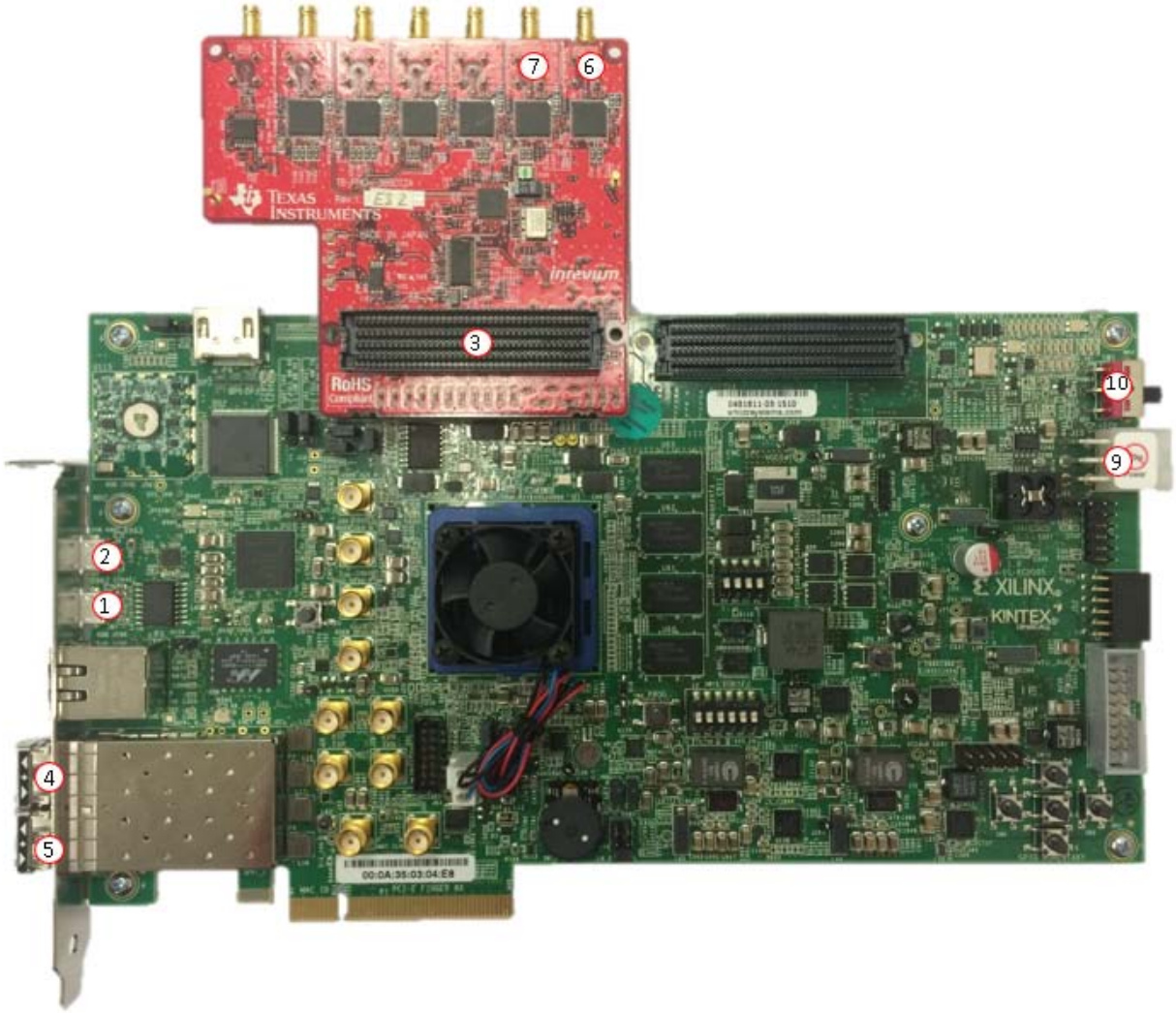

Figure 11: **KCU105, and TB-FMCH-3GSDI2A Boards**

In these instructions, numbers in parentheses correspond to callout numbers in Figure 11.

1. Connect a USB cable from the host PC to the USB JTAG port (1). Ensure the appropriate device drivers are installed.
2. Connect a second USB cable from the host PC to the USB UART port (2). Ensure that USB UART drivers described in the section Hardware Requirements have been installed.
3. Connect TB-FMCH-3GSDI2A board to the HPC-FMC of KCU105 (3).
4. Connect an SFP+ Optical Transceiver to the SFP slot (4) and (5), Primary and Secondary Links respectively.
5. Connect one end of the optical cable (4) to the SFP+ of VoIP transmitter board, the other end to the SFP+ of VoIP receiver board.
6. Connect one end of the optical cable (5) to the SFP+ of VoIP transmitter board, the other end to the SFP+ of VoIP receiver board.
7. Connect the CH0-TX, CH1-TX & CH2 ports of TB-FMCH-3GSDI2A (6) to the SDI video monitor if the KCU105 board is the VoIP receiver.

8. Connect the CH0-RX, CH1-RX & CH2 ports of TB-FMCH-3GSDI2A (7) to the SDI video generator if the KCU105 board is the VoIP transmitter.
9. Connect the KCU105 board to a power supply slot J49 (9).
10. Turn on the KCU105 board.
11. Start a terminal program (e.g. HyperTerminal) on the host PC with these settings:

    Note: Look for Silicon Labs Dual CP210x USB to UART Bridge: Standard COM Port when setting up the serial connection.

    - Baud Rate: 115200
    - Data Bits: 8
    - Parity: None
    - Stop Bits:1
    - Flow Control: None

Running the Reference Design

This section details the steps necessary to execute the system using the files in the ready_for_download directory

1. Launch the Xilinx Microprocessor Debugger by selecting Start > All Programs > Xilinx Design Tools > Vivado 2015.1.
2. In the Xilinx command shell window, change to the ready_for_download directory:

```
VoIP_TX: > cd <unzip_dir>\kcu105_smpte2022_56_tx_ip/ready_for_download
VoIP_RX: > cd <unzip_dir>\kcu105_smpte2022_56_rx_ip/ready_for_download
```

3. Download the bitstream to the FPGA:

```
XMD% fpga -f download.bit
```

4. Exit the XMD command prompt:

```
XMD% exit
```

Note: The software application will start immediately after the completion of FPGA configuration. The executable file (.elf) is embedded in the configuration file (download.bit). See Results section for sample of UART printouts.

Building Hardware

This section covers rebuilding the hardware design. Before rebuilding the project, ensure that the licenses for the SMPTE 2022-5/6 Video over IP Transmitter and Receiver cores, 10-Gigabit Ethernet PCS/PMA, and Ten Gigabit Ethernet MAC are installed.

Note: To ensure that no compilation errors occur due to long file paths, unzip the project files as close to the root directory as possible. For example, with a typical Windows installation, unzip the files at C:\.

Generating Programming File in Vivado Design Suite 2015.1

1. Open Vivado Design Suite
2. At the Tcl Console, change to the workspace directory by typing:

   VoIP_TX:

   ```
   > cd <unzip_dir>\kcu105_smpte2022_56_tx_ip
   ```

   VoIP_RX:

   ```
   > cd <unzip_dir>\kcu105_smpte2022_56_rx_ip
   ```

3. Run the all.tcl script to create, compile and generate the project bitstream

   ```
   > source all.tcl
   ```

Compiling Software in SDK

The SDK environment needs to be prepared after the completion of "all.tcl" script, this is done by exporting the project's hardware information and importing the SDK source codes.

1. **Export hardware**: In Vivado 2015.1 select, **File > Export > Export Hardware**.
   a. In the **Export Hardware** pop-up window, Check **Include bitstream** option.
   b. Set the **Export to**: field correspondingly:

   ```
   VoIP_TX: <unzip_dir>\kcu105_smpte2022_56_tx_ip\SW\SDK_Workspace
   VoIP_RX: <unzip_dir>\kcu105_smpte2022_56_rx_ip\SW\SDK_Workspace
   ```

2. **Launch Xilinx SDK 2015.1** from **Start > All Programs > Xilinx Design Tools > SDK 2015.1**.
   a. Once in SDK, create a new Board Support Package; **File > New > Board Support Package**.
   b. Click on **Specify** in the **No Hardware Platforms in the Workspace** pop-up window.
   c. Key-in **hw** in the **Project Name**: Field.
   d. Click on **Browse** and click **OPEN** after selecting the .HDF file in the corresponding folder:

   ```
   VoIP_TX: <unzip_dir>\kcu105_smpte2022_56_tx_ip\SW\SDK_Workspace
   VoIP_RX: <unzip_dir>\kcu105_smpte2022_56_rx_ip\SW\SDK_Workspace
   ```

   e. Click **Finish.**
   f. Key-in **voip_bsp** in the **Project name**: field of In the **New Board Support Package Project** pop-up window.
   g. Click **Finish**, then click **OK**
3. **Import SDK Sources**: In SDK 2015.1 select, **File > Import**
   a. In the Import pop-up window, select **General > Existing Projects into Workspace**
   b. Click **Next**.

c. Click on **Browse** button, and make sure that it points to the corresponding folders

```
VoIP_TX: <unzip_dir>\kcu105_smpte2022_56_tx_ip\SW\SDK_Workspace
VoIP_RX: <unzip_dir>\kcu105_smpte2022_56_rx_ip\SW\SDK_Workspace
```

d. Click **OK**.

e. Make sure **voip_bsp** and **voip_tx/rx** are checked.

f. Click **Finish**.

The BSP and software applications compile at this step. The process takes 2 to 5 minutes. The existing software applications can now be modified and new software applications can be created in the SDK.

Running the Hardware and Software through SDK

1. Select **Xilinx Tools > Program FPGA**. See Figure 11.

   Ensure the Hardware Platform is the same as written in Project Field, e.g: **hw**.

   Ensure the connection is set to **Local**.

   Ensure bootloop is used for **system_basic_i/microblaze_1**.

2. Click **Program**.

3. In the Project Explorer window, right click and select:

```
VoIP_TX:  voip_tx > Run As > Launch on Hardware (GDB)
VoIP_RX:  voip_rx > Run As > Launch on Hardware (GDB)
```

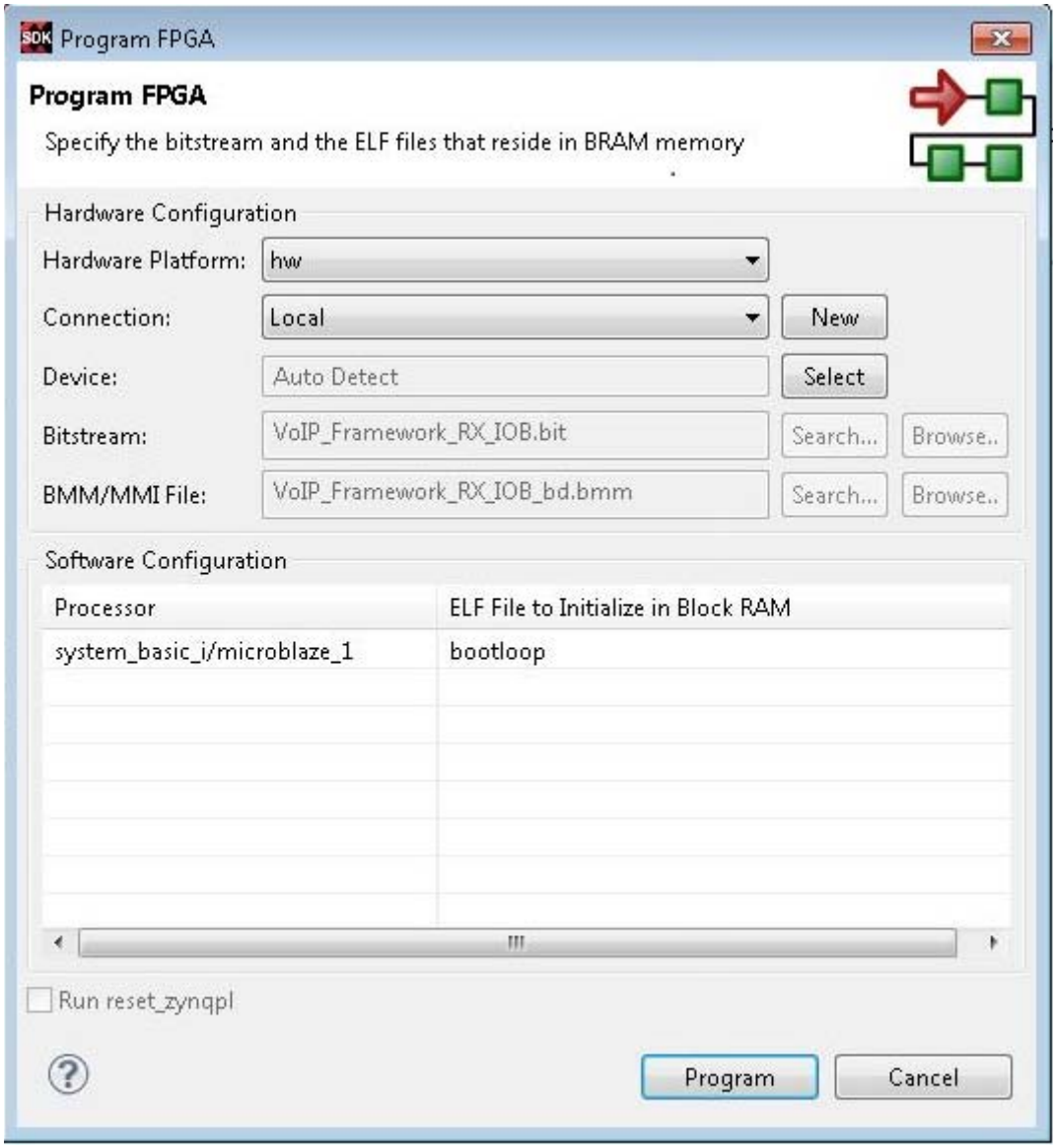

Figure 12: **Program FPGA Configuration Settings**

Results

HyperTerminal screen of VoIP TX and RX displays the output shown in Figure 13 and Figure 16 respectively.

VoIP_TX UART Display

```
_____  _____
 /   /\/   /
/___/  \  /   Xilinx Inc.
\   \   \/    V_SMPTE2022_567_TX 10G
 \   \        Vivado Reference Design
 /   /        Created: April 28, 2015
/___/   /\    Copyright (c) 2014 Xilinx, Inc.
\   \  /  \   All rights reserved.
 \___\/\___\

VoIP TX Reset

VoIP TX Initializing...

EMAC Fault Inhibit    : Enabled
Primary MAC Address   : 00-00-00-00-00-AA
Secondary MAC Address : 00-00-00-00-00-CC
Hitless Protection    : Enabled
VoIP TX Initialization done


Initializing for Primary Channel 1
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0010
Dest Port:        0x0010
VLAN:             Disabled
VLAN Tag:         0xAB00
SSRC:             0x12345600
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Primary Channel 1 Initialization Done

Initializing For Secondary Channel 1
IP Version:       IPv4
MEDIA TTL:        0
MEDIA TOS:        0
FEC TTL:          0
FEC TOS:          0
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:   192.168.1.50
Dest IP Addr:     192.168.1.100
Source Port:      0x0010
Dest Port:        0x0010
VLAN:             Disabled
VLAN Tag:         0xAB00
SSRC:             0x12345600
Time Stamp        Enabled
FEC Size:         77x77
```

```
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Secondary Channel 1 Initialization Done
VoIP TX Channel 1 Enabled
VoIP TX Configuration for Channel 1 Initialization Done


Initializing for Primary Channel 2
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0020
Dest Port:        0x0020
VLAN:             Disabled
VLAN Tag:         0xAB10
SSRC:             0x12345610
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Primary Channel 2 Initialization Done

Initializing For Secondary Channel 2
IP Version:       IPv4
MEDIA TTL:        0
MEDIA TOS:        0
FEC TTL:          0
FEC TOS:          0
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:   192.168.1.50
Dest IP Addr:     192.168.1.100
Source Port:      0x0020
Dest Port:        0x0020
VLAN:             Disabled
VLAN Tag:         0xAB10
SSRC:             0x12345610
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Secondary Channel 2 Initialization Done
VoIP TX Channel 2 Enabled
VoIP TX Configuration for Channel 2 Initialization Done


Initializing for Primary Channel 3
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
```

```
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0030
Dest Port:        0x0030
VLAN:             Disabled
VLAN Tag:         0xAB20
SSRC:             0x12345620
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Primary Channel 3 Initialization Done

Initializing For Secondary Channel 3
IP Version:       IPv4
MEDIA TTL:        0
MEDIA TOS:        0
FEC TTL:          0
FEC TOS:          0
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:   192.168.1.50
Dest IP Addr:     192.168.1.100
Source Port:      0x0030
Dest Port:        0x0030
VLAN:             Disabled
VLAN Tag:         0xAB20
SSRC:             0x12345620
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Secondary Channel 3 Initialization Done
VoIP TX Channel 3 Enabled
VoIP TX Configuration for Channel 3 Initialization Done


-----------------------
-- VoIP TX Main Menu --
-----------------------

 Select option
 1 = Reset Core
 2 = Initialize Core
 3 = Change Primary MAC Address
 4 = Change Secondary MAC Address
 5 = Hitless Protection On/Off
 6 = 10G MAC Fault Inhibit On/Off
 s = Configure Channel
 p = Probe Current Settings
 ? = help
------------------
>
```

Figure 13: **VoIP_TX UART Display**

You are allowed to choose one of nine options that displayed in the VoIP TX main menu (refer to Figure 13).

Note: Enable single (downstream) optical link from TX to RX by turning off the Hitless Protection (Option 5)

Select channel screen display:

```
-----------------------
--  Select Channel   --
-----------------------
 Primary Channels
 1 = Channel 1
 2 = Channel 2
 3 = Channel 3
 Secondary Channels
 a = Channel 1
 b = Channel 2
 c = Channel 3
------------------
>
```

Figure 14: **VoIP_TX Select Channel HyperTerminal Output**

You are allowed to choose one of three channels for each link (Primary/Secondary) or go back to main menu (refer to Figure 14). After selecting any of these available channels, the **Select Option** submenu is displayed and you are allowed to choose one of these options from the menu list (refer to Figure 15.)

```
-----------------------
--   Select Option   --
-----------------------
 1 = Channel Init
 2 = Channel Enable/Disable
 3 = Change Host IP Address
 4 = VLAN En/Disable
 5 = Change VLAN Tag
 6 = Set Dest MAC Addr
 7 = Set Dest IP Addr
 8 = Set Source UDP Port
 9 = Set Dest UDP Port
 0 = Set SSRC
 a = FEC On/Off
 b = Toggle FEC Level
 c = Set Column FEC
 d = Set Row FEC
 e = Toggle Block Alignment
 f = Time Stamp Include En/Disable
 t = Transmit Enable/Disable
 r = Transmit Packet Count Stat Reset
 p = Probe Status
 m = Main Menu
 s = Channel Select
------------------
>
```

Figure 15: **VoIP_TX Select Option HyperTerminal Output**

VoIP_RX UART Display

```
  _____  _____
 /    /\/    /
/___/  \   /    Xilinx Inc.
\   \   \/     V_SMPTE2022_567_RX 10G
 \   \         Vivado Reference Design
 /   /         Created: April 28, 2015
/___/   /\     Copyright (c) 2014 Xilinx, Inc.
\   \  /  \    All rights reserved.
 \___\/\___\


VoIP RX Reset

VoIP RX Initializing...

EMAC Fault Inhibit: Enabled

Network Diff. Path:      1350000
FEC Base Address:        0xD8000000
FEC Pool Size:           72855552
VoIP RX General Space Initialization done


Initializing Channel 1
Primary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB00
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0010
Match Source Port:       0x0010
Match SSRC:              0x12345600




Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB00
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0010
Match Source Port:       0x0010
Match SSRC:              0x00000000

Match Select:
   SSRC:                  Off
```

```
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
Playout Delay:            2700000
Channel Buffer Address:   0xC0000000
Channel Buffer Size:      65535
Timestamp Bypass:         Disable
Channel 1 Enabled
Channel 1 Initialization Done

Initializing Channel 2
Primary Stream Configure
IP Version:               IPv4
Match VLAN:               Disable
Match VLAN Tag:           0xAB10
Match Dest IP Addr:       192.168.0.100
Match Host IP Addr:       192.168.0.50
Match Dest Port:          0x0020
Match Source Port:        0x0020
Match SSRC:               0x12345610

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:               IPv4
Match VLAN:               Disable
Match VLAN Tag:           0xAB10
Match Dest IP Addr:       192.168.0.100
Match Host IP Addr:       192.168.0.50
Match Dest Port:          0x0020
Match Source Port:        0x0020
Match SSRC:               0x00000000

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
Playout Delay:            2700000
Channel Buffer Address:   0xC8000000
Channel Buffer Size:      65535
Timestamp Bypass:         Disable
Channel 2 Enabled
Channel 2 Initialization Done
```

```
Initializing Channel 3
Primary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB20
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0030
Match Source Port:       0x0030
Match SSRC:              0x12345620

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB20
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0030
Match Source Port:       0x0030
Match SSRC:              0x00000000

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
Playout Delay:           2700000
Channel Buffer Address:  0xD0000000
Channel Buffer Size:     65535
Timestamp Bypass:        Disable
Channel 3 Enabled
Channel 3 Initialization Done

-----------------------
-- VoIP RX Main Menu --
-----------------------

 Select option
 1 = Reset Core
 2 = Initialize Core
 3 = 10G MAC Fault Inhibit On/Off
 r = Reset General Space Stat Counters
 s = Configure Channel
 p = Probe Current Settings
 ? = help
------------------
>
```

Figure 16: **VoIP_RX HyperTerminal Output**

You are allowed to choose one of seven options displayed in the VoIP RX main menu (refer to Figure 16.)

```
Select channel screen display:
----------------------
--  Select Channel   --
----------------------
 Primary Channels
 1 = Channel 1
 2 = Channel 2
 3 = Channel 3
 Secondary Channels
 a = Channel 1
 b = Channel 2
 c = Channel 3
------------------
>
```

Figure 17: **VoIP_RX Select Channel HyperTerminal Output**

VoIP_RX Select Channel HyperTerminal Output

You are allowed to choose one of three channels for each links (Primary/Secondary) or go back to main menu (refer to Figure 17). After selecting any of these available channels, the "Select Option" submenu will be displayed and user is allowed to choose one of these options from the menu list (refer to Figure 18).

```
----------------------
--   Select Option   --
----------------------
 1 = Channel Init
 2 = Channel Enable/Disable
 3 = Match VLAN On/Off
 4 = Timestamp Bypass On/Off
 5 = Channel Filter Change
 p = Probe Status
 q = Probe Statistic
 r = Channel Statistics Reset
 m = Main Menu
 s = Channel Select
------------------
>
```

Figure 18: **VoIP_RX Select Option HyperTerminal Output**

Debugging

On-board GPIO LEDs can be used for quick troubleshooting. During normal operation all LEDs should asynchronously turn on within 5 seconds after bitstream configuration. The LED representations are shown in Table 8.

Table 8: **KCU105 GPIO LED Designations for Transmitter and Receiver**

GPIO_LED	Designation
0	10G PCS/PMA Primary Link Up
1	10G PCS/PMA Secondary Link Up
2	QPLL0 Lock
3	QPLL1 Lock
4	Si5328 Loss-of-Lock (Inverted)
5	GTRESETDONE
6	MMCM Lock
7	DDR Memory Initialization Done

GPIO_LED 0 and 1: When this LED is off, it can be an indication that either primary or secondary links are not properly connected to the opposite board.

GPIO_LED 2 and 3: When this LED is low, it can be an indication that 1.8V VADJ is not properly set. See Setting VADJ to 1.8V instructions below.

GPIO_LED 4: When this LED is low, it means that the 156.25 MHz Ethernet clock is not up. This takes about 15 seconds to turn on after bitstream configuration.

GPIO_LED 6 & 7: When this LED is low, it means that the memory subsystem didn't successfully initialize. Ensure that you are using a production version of KCU105.

Setting VADJ to 1.8V

Make sure that the VADJ power to FMCH port is at 1.8V. VADJ power good is indicated by DS19 LED located near the power switch of the KCU105 board. If the LED is off, the VADJ power can be set through KCU105's system controller's UART interface.

Open a Terminal window (115200, 8, N, 1) and set the COM port to the one communicating with the KCU105 System Controller. (Note, the single microUSB connector provides access to both the Zynq-7000 system controller's UART and to the UltraScale FPGA's UART.) In the Windows Device Manager, the Enhanced COM port associated with the CP210x, is the one connected to the System Controller.

After the system is brought up, IP (SMPTE 2022-56 TX and RX) debug need to be performed, this can be found under Core Debug Section in *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter v4.0 Product Guide* [Ref 4] and *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter v4.0 Product Guide* [Ref 5].

Known Issues

1. IPI subsystem may have timing violations within the MIG IP
2. The rx_ce_out UHD-SDI output port connected to rxN_dout_rdy_3G VoIP_TX input must be delayed by one rxN_clk cycle to ensure proper 3G-SDI Level B operation. This has been incorporated into the reference design with signal name, sdi_rx_ce_ff.

References

This application note uses the following references:

1. Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit, http://www.xilinx.com/products/boards-and-kits/kcu105.html
2. inrevium TB-FMCH-3GSDI2A http://solutions.inrevium.com/products/fmc/hpc/index.html
3. AMBA AXI4 specifications, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.set.amba/index.html
4. *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032)
5. *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033)
6. *LogiCORE IP SMPTE UHD-SDI Product Guide LogiCORE IP* (PG205)
7. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
8. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068)
9. *AXI Reference Guide* (UG761)
10. *LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions v7.0* (PG150)
11. *Implementing SMPTE SDI Interfaces with UltraScale GTH Transceivers* (XAPP1248)

Revision History

The following table shows the revision history for this document.

Date	Version	Changes
06/24/2015	1.0	Initial Xilinx release.

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