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Bus LVDS with Virtex-E Devices

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Summary

This application note describes how to use Virtex™-E Bus Low Voltage Differential Signaling (BLVDS) technology in high-performance multipoint applications. BLVDS extends the benefits of standard LVDS into multipoint configuration supporting bidirectional backplanes. Spice simulation results show that the multipoint configuration described in this application note can operate up to 200 MHz.

Introduction

Multipoint LVDS allows many transceivers to connect to a backplane. BLVDS provides higher current drive than LVDS with a comparable voltage swing when terminated with two parallel resistors (one at each end of the backplane). In multipoint configuration, the driver is located at any location on the bidirectional backplane; thus it requires terminations at both ends. The true differential LVDS input and output capability of the Virtex-E family enables this multipoint application. A Virtex-E multipoint driver with the capability to enable a high-impedance state can drive lines with different fan-outs, making Virtex-E devices suitable for high-performance multipoint backplane applications.

Multipoint LVDS

Figure 1 shows a typical multipoint LVDS configuration. This configuration is implemented with many transmitter-receiver pairs called transceivers. It allows bidirectional data transfer across the backplane. Due to bidirectional transfer capability, a line termination resistor is needed at both ends. The two 50 ohm, single-ended transmission lines are typically implemented as microstrips. Microstrip is a PCB (printed-circuit board) trace on the top or bottom layer of the PCB over a ground or power plane as illustrated in Figure 2. The characteristic impedance of the microstrip is determined by the trace width, trace height above the power/ground plane, trace thickness, and the relative dielectric constant of the PCB.

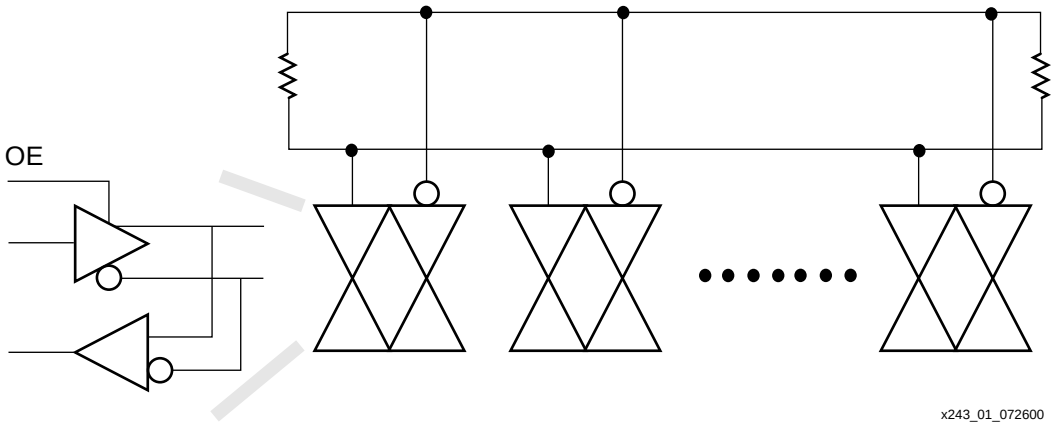


Figure 1: **Typical Multipoint LVDS Configuration**

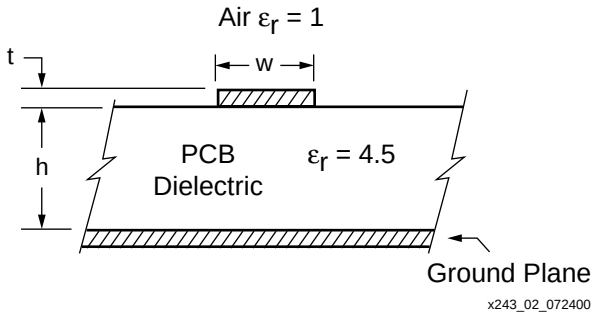


Figure 2: **Microstrip Transmission Line Cross-Section**

When the microstrip line is loaded with the devices and stubs, the distributed capacitance of the receivers and stubs affects both the propagation delay and the characteristic impedance of the line. The net result is that the effective (loaded line) impedance will be lower than the characteristic impedance of the line, and the effective line propagation delay will be slower. The effective impedance and line propagation delay are calculated using Equations 1 and 2.

$$Z_0(\text{effective}) = \sqrt{\frac{L}{C + \frac{NC_{LOAD}}{H}}} \quad (1)$$

$$T_{PD}(\text{effective}) = \sqrt{L\left(C + \frac{NC_{LOAD}}{H}\right)} \quad (2)$$

where C_{LOAD} = capacitance of each load in pF
N = number of loads
H = total length of transmission line
L = inductance per unit length
C = capacitance per unit length

The value of the termination resistor at each end of the line depends on the effective impedance of the line. As loading alters the characteristic impedance of the line, it is very important to determine the correct load impedance of the line to prevent signal-integrity issues such as reflections and ringing due to mismatched impedance.

Due to its bidirectional transfer capability the transmitter in a multipoint system can drive the line from any position. The end termination resistors should be chosen to reduce reflections but not overload the driver.

Multipoint LVDS Using Virtex-E Devices

In this section, two different multipoint-LVDS configurations using Virtex-E devices are simulated using SPICE models. The first multipoint-LVDS configuration consists of 10 Virtex-E transceivers. The second consists of 20 Virtex-E transceivers. Each single transmission line in both cases is modeled as a 50-ohm microstrip line with a line propagation delay (T_{PD}) of 135 ps/inch at a relative permitivity ε_r = 4.7 without loading, or a differential impedance of 100-ohms between two lines. The capacitance per unit length (C) is equal to 3.67 pF/inch, where the inductance per unit length (L) is 9.2 nH/inch.

Figure 3 shows a complete schematic for a 10-load multipoint LVDS using Virtex-E devices. The Virtex-E transceivers are connected in a bidirectional backplane. The driver can be located at any location on the backplane; thus termination is required at both ends of the backplane. Each Virtex-E BLVDS transceiver taps off the main multipoint lines every two inches. The main lines are 20-inches long. Each BLVDS transceiver tap line has a 1.5-inch maximum stub length. The transceivers in Figure 3 have an effective load capacitance of roughly 8 pF, including receiver capacitance, trace and stub capacitance. In a fully loaded system, all 10 transceivers are populated, and the effective differential impedance of the fully loaded backplane is about 70 ohms, as calculated using Equation 1. A 54-ohm termination resistor is placed across two lines at each end of the backplane to reduce reflections. Virtex-E BLVDS drivers provide the higher current drive needed to achieve a voltage swing of 400 mV with a lower effective impedance and double termination scheme. A 50-ohm series resistor on each signal line, next to the Virtex-E transceivers, reduces the magnitude of the reflections, which can be caused by the long stubs, and also attenuates the signals coming out of the Virtex-E drivers.

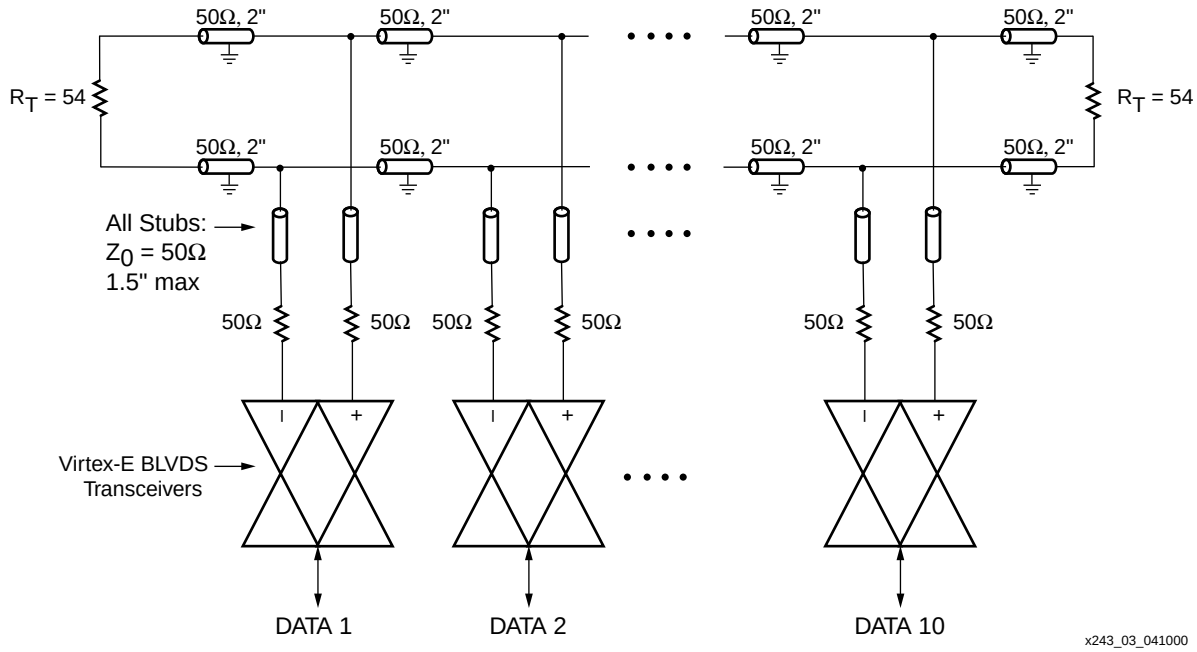
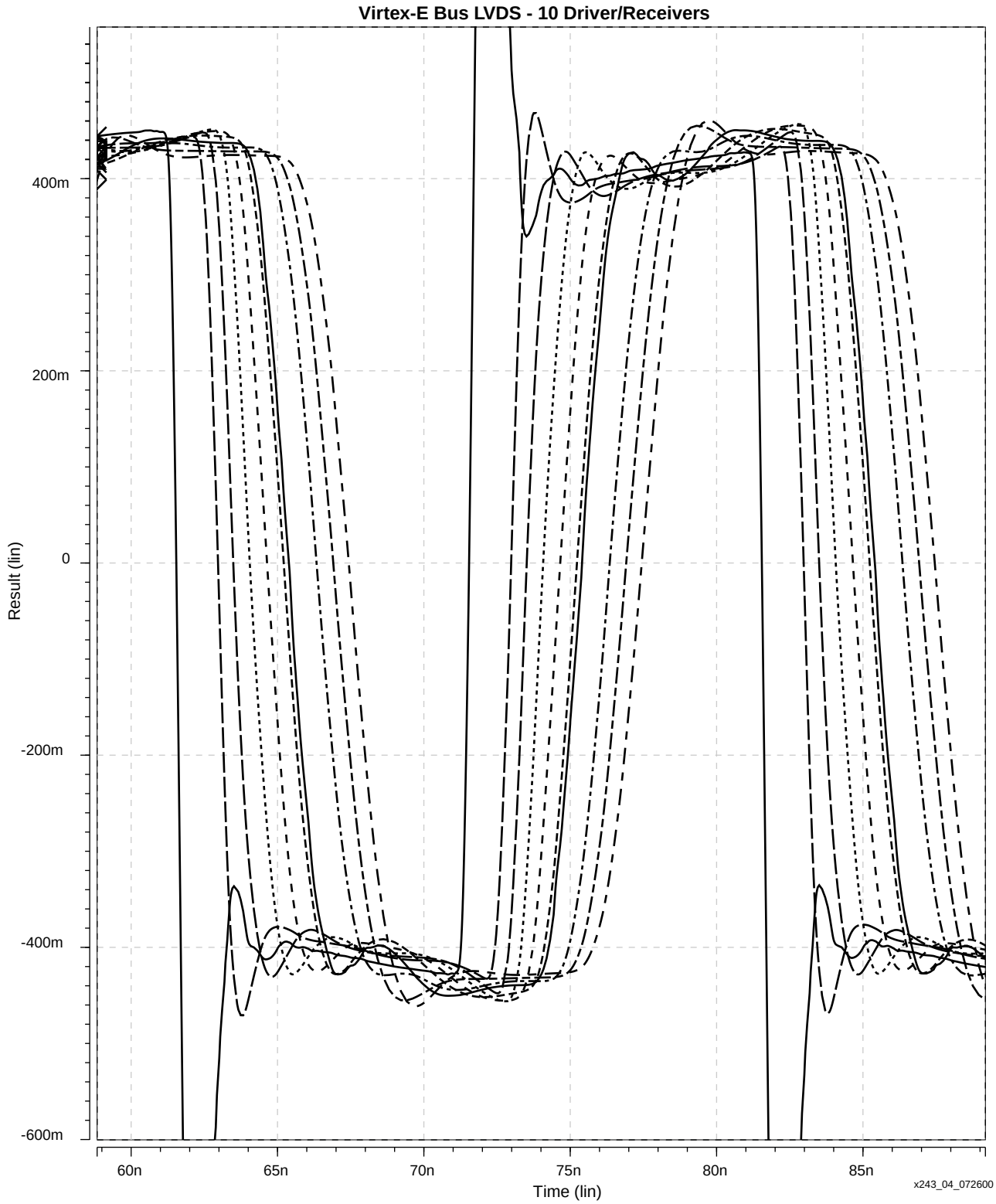


Figure 3: **10-Load Multipoint LVDS Using Virtex-E Devices**

Figure 4 shows the simulation waveforms for a 10-load multipoint LVDS using Virtex-E devices. The data is clocked over the backplane at a clock frequency of 200 MHz. Differential waveforms are shown for the output driver and input receivers. The longest rise time of 1.5 ns is measured with the driver located at one end of the backplane and the receiver located at the other end of the backplane. All the waveforms at the receiver end show similar characteristics with little undershoot or overshoot and negligible load reflections. Figure 4 also shows the receiver-input waveforms have substantial noise margins with respect to the receiver thresholds of ±100 mV. Table 1 shows the noise margin results for different cases depending on where the driver is located. There is some overshoot at the driver terminals but the receiver signals are not affected.



Notes:

1. A signal from the driver produces the overshoot and undershoot waveform.

Figure 4: **Simulation Waveforms for 10-Load Virtex-E Multipoint LVDS**

Table 1: **Noise Margin for 10-Load Configuration**

Noise Margin		
Falling Edge	**Rising Edge**	**Units**
280	280	mV

Figure 5 shows a 20-load multipoint LVDS schematic using Virtex-E devices. Each Virtex-E BLVDS transceiver is uniformly spaced two inches apart on a 40-inch multipoint length line. Each BLVDS transceiver tap line has 1.5-inch maximum stub length. The transceivers in Figure 5 have an effective load capacitance of roughly 8 pF, including receiver capacitance, trace and stub capacitance. When all 20 Virtex-E BLVDS transceivers are fully populated, the effective impedance of the fully loaded backplane is calculated using Equation 1 as 70 ohms. The effectvie impedance is the same as in the case of the 10-load scenario because the spacing between the stubs and the stub-lengths have not increased. An 80-ohm termination resistor is placed across the two lines at each end of the backplane to approximately match the effective impedance of the fully loaded line and to provide a differential voltage swing of approximately 250 mV at the receivers. A 50-ohm series resistor on each signal line, next to the Virtex-E transceivers, reduces the magnitude of the reflections (which can be caused by the long stubs) and attenuates the signals coming out of the Virtex-E devices.

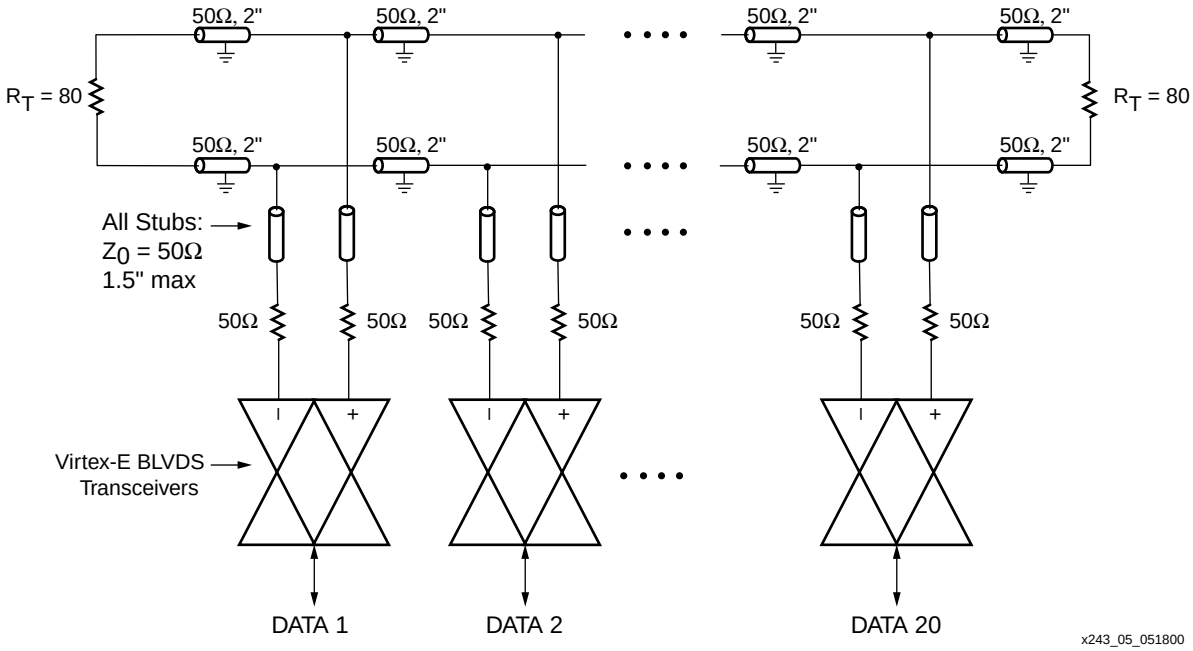


Figure 5: **20-Load Multipoint LVDS Using Virtex-E Devices**

Figure 6 shows the simulation waveforms for 20-load multipoint LVDS using Virtex-E devices. The data is clocked over the backplane at clock frequency of 200 MHz. Differential waveforms are shown for the output driver and input receivers. The longest rise time of 2.0 ns is measured with the driver located a one end of the backplane and the receiver is located at the other end of the backplane. All the waveforms at the receivers show similar characteristics with small undershoot or overshoot and negligible load reflections. The noise margin at the receiver inputs is substantial with respect to the receiver thresholds of ±100 mV. Table 2 shows noise margin results for different cases on where the driver is located. There is some overshoot at the driver terminals but the receiver signals are not affected.

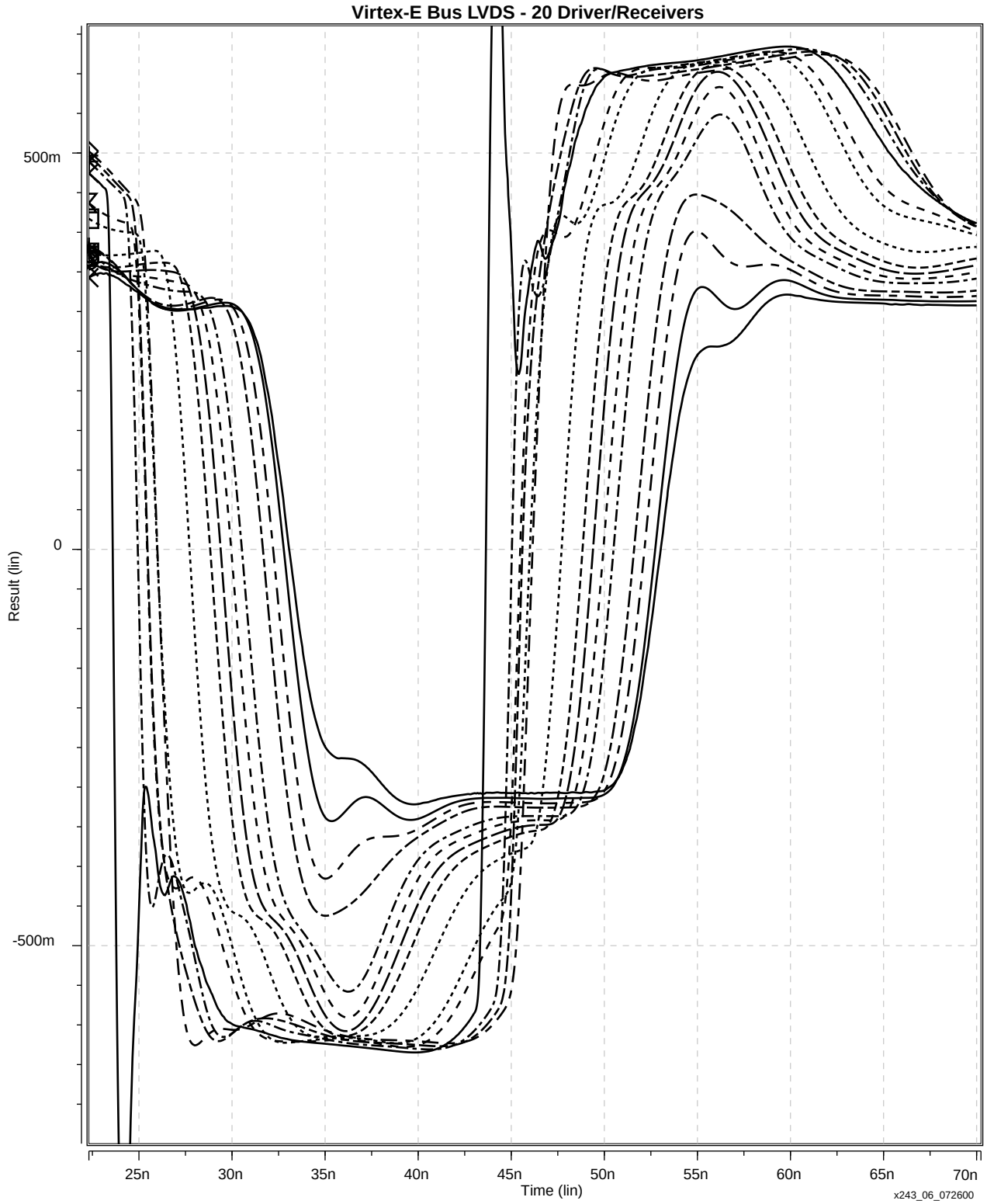


Figure 6: **Simulation Waveforms for 20-Load Virtex-E Multipoint LVDS**

Table 2: **Noise Margin for 20-Load Configuration**

Noise Margin		
Falling Edge	**Rising Edge**	**Units**
220	220	mV

Multipoint LVDS using Virtex-E devices and National BLVDS:

Conclusion

Virtex-E BLVDS technology enables system designers to customize their high-performance multipoint backplane applications while maximizing overall bandwidth. Spice simulation shows that a clock rate of 200 MHz is achievable in different loading configurations. Virtex-E FPGAs utilizing BLVDS eliminate costly TTL-BLVDS and BLVDS-TTL translators, reduce board area, EMI, power consumption, and signal delay skew while reliably transferring high-speed signals over multipoint backplanes.

Appendix A: Design Pointers for Bus LVDS

1. Minimize stub lengths to reduce transmission line effects. Keep the stub length between 0.5 and 1.5 inches.
2. The effective (loaded line) impedance is lower than the characteristic (unloaded) impedance of the line due to distributed capacitance loading. The more loads are added to the backplane, the lower the effective impedance of the line.
3. The end termination (parallel termination) resistor value at each end of the backplane should be close to the effective impedance of backplane.
4. Stub termination (series termination) should be used to reduce transmission line effects.
5. Match the length of the two lines that make up the differential pair to minimize common-mode noise.
6. Place the two lines close to each other to ensure noise picked up will appear as common-mode and rejected by the receivers.
7. Check the transmission line effects of the receiver next to the driver because the signals edge rate is highest there.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
7/26/00	1.0	Initial Xilinx Release