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Assigning CoolRunner-II VREF Pins

Summary

The flexibility of the CoolRunner™-II CPLD allows users to configure any I/O pin to act as a voltage reference (VREF) pin. This document describes the different methods and underlying rules for determining the number and placement of these VREF pins.

Introduction

The CoolRunner-II family supports the following high-speed I/O standards in the 128-macrocell and larger devices: SSTL2-1, SSTL3-1 and HSTL-1. These I/O standards all require VREF pins for proper operation. In most devices, VREF pins are specifically declared on the datasheet, leaving no placement options for the user. The CoolRunner-II CPLD allows any I/O pin to act as a VREF pin, granting extra freedom to the board-layout engineer when laying out the pins. However, if VREF pin placement is not done properly, additional VREF pins may be required, resulting in a loss of potential I/O pins or board re-work.

VREF Placement Methods

There are two methods of determining VREF locations: Software Placement and Manual Placement. Software Placement allows the Xilinx CPLD software to place the VREF pins based on the locations and the I/O Standard of the pins in the design. Manual Placement requires the user to look at his I/O Standards and their locations, then check VREF placement rules in order to determine where VREF pins must be assigned. The Xilinx CPLD software then double-checks these assignments and may add pins as needed. The VREF placement rules are not trivial, and therefore the Software Placement method is recommended for most users.

Software Placement (Automatic)

If you do not configure any pins as VREF, the Xilinx software will automatically assign them using the guidelines mentioned later in the Manual Placement section. The following flow is recommended for the Software Placement method:

1. Place I/O Standard attributes on all I/Os
2. (Optional) Pin lock I/Os
3. Implement design
4. Pin lock I/Os (if not already pin assigned in earlier step)
5. Copy VREFs from the .GYD file into UCF
6. Re-implement design and verify VREFs

Step 1. Place I/O Standard attributes on all I/O

This can be done by utilizing the Constraints Editor GUI or by editing the Users Constraint File (UCF) in any text editor.

The syntax for assigning an I/O standard to a net in the UCF is:

NET <*signal name*> IOSTANDARD = <*I/O standard attribute name*>;

Example:

NET data_in IOSTANDARD=HSTL_I;

Alternatively, these attributes may be entered in the source HDL files. For more details, please see **Xilinx XAPP378:Using CoolRunner-II Advanced Features**.

If the design is not yet complete, a user may find that the inputs that connect to unfinished sub-modules are removed from the design during Xilinx fitter optimization. This behavior is generally desired because the software is removing pins and logic that serve no purpose in the design, and therefore take up logic resources which could be used elsewhere. However, with respect to VREF pin assignments, this behavior is not beneficial because these inputs will have an impact on the placement of other I/O and VREF pins.

This problem can be resolved by creating 'dummy logic' as a placeholder. Create an output pin, and then tie all of the unused inputs together into a single logic function so the inputs cannot be trimmed.

For example:

A design contains a data bus that is currently unused (data<1:0>) as well as an enable signal (en). In order to ensure that these inputs are not trimmed out of the design, create a dummy output that uses these signals as inputs.

dummylogic <= data(1) and data(0) and en;

This simple fix will ensure that the inputs are not trimmed out of the design, and therefore included when analyzing the IOs for VREF pins. When the design is complete, the dummy logic may be removed.

Step 2. Pin Lock I/Os

This step is optional. It is generally recommended that you allow the Xilinx CPLD software to place the I/Os for you, as the software grants maximum flexibility to the fitter when it places logic in the device. Location constraints may be created by using the Constraints Editor or by editing the UCF in any ASCII text editor (eg. Wordpad, vi, Notepad).

The syntax for assigning pin locations in the UCF is:

NET <signal name> LOC = <location>;

Example for pinned packages (VQ,PQ,TQ):

NET data_in LOC = P12;

Example for ball-grid packages (CP, FT, FG):

NET data_in LOC=M10;

Step 3. Implement Design

In this phase, the Xilinx CPLD software takes the constraints given (I/O standards, pin locations, device and package), fits the design, and creates VREF pins for the necessary I/O standards. At this point, Design Rule Checking (DRC) also verifies that there are not more I/O standards than I/O banks, and that multiple I/O standards do not exist within the same I/O bank. If no conflicts are found, the pinout and VREF information is written into the Device Pin Out section of the report file (designname.rpt).

Step 4. Pin Lock I/Os

If the I/Os were not pin-assigned earlier, they must be now. If this is not done, the Xilinx CPLD software may move pins around in order to best meet timing and to best share logic after multiple iterations of the design. This could result in the location of VREF pins changing.

Pin assignments may be done by double-clicking on the "Lock Pins" process within the ISE Project Navigator. This is located under "Implement Design" section of the Processes tree. This process will take the pin locations for all I/Os and VREFs placed by the fitter and write them into the UCF.

Step 5. Copy VREFs from the .GYD file into the UCF

After a successful fit, a [designname].GYD file will be present in the project directory. Locate this file and open it in any text editor. At the bottom of the .GYD file are the pins selected by the fitter to use as VREF pins.

They will appear similar to the following:

CONFIG VREF = P13;

CONFIG VREF = P23;

Copy these VREF statements into the User Constraints File (UCF).

Step 6. Re-implement design and Verify VREFs

Re-implement the design with the new VREF constraints and check the pin-out diagram at the bottom of the fitter report to ensure that the VREFs you have assigned are in the proper locations. Also count the number of VREFs in the pin-out diagram to make sure that they equal the number that you have in the constraints file.

Manual Placement

VREF Placement Rules

Note: This section may be skipped if the user utilizes the Software Placement method.

I/O Banking

Only the 128-macrocell and larger CoolRunner-II CPLDs support the SSTL2-1, SSTL3-1, and HSTL-1 I/O Standards. These I/O Standards each require their own reference voltages. The CoolRunner-II CPLD I/Os are separated into banks. Each bank shares the same reference voltage level; therefore, one may not place more than one I/O standard type within the same bank. The XC2C128 and XC2C256 have two I/O banks and the XC2C384 and XC2C512 have four banks.

Pad Distance Limit

An I/O pin utilizing a VREF may only be 6 ***pads*** away from its VREF pin. Pad distances are ***not*** pin distances. In order to determine pad distance with respect to pins, consult **Appendix A: Pad Distance Tables**, page 5. These tables list all device and package I/O pins and contain a "distance" column, which is used to determine pad distance. To determine distance, simply find the difference between distance values for the VREF pin and the I/O pin.

Example :

Given a XC2C128 TQ144 with an I/O in Pin 17 and a VREF on Pin 12.
Appendix A, Table 1 contains the table for a XC2C128 and Column 1 contains the I/O pin numbers for the TQ144 package. Matching Pin 17 (row) with the distance column returns a distance of 126. Matching Pin 12 (row) with the distance column returns a distance of 121. The (absolute) difference between 126 and 121 is 5; therefore this combination does not violate the pad distance limit.

VREF I/O Limit

Each VREF pin may support at most six single-ended I/O pins. The software will not allow a programming file to be generated unless this requirement is met.

Example:

Consider a design that has eight SSTL2-1 inputs for a XC2C256 PQ208. Since each VREF can only support six I/O this design will require two VREF pins. Table 2 of Appendix A contains the distance table for the XC2C256. Column 2 lists the I/O pins for the PQ208. The table shows a cluster of I/O pins from 142 to 155 that are all I/O pins and are also all in bank 2. This set of pins was chosen arbitrarily.

Assigning VREFs to pins 145 and 151 provides good coverage because Pin 145 can support I/Os from 139 to 144 (excluding 141, which is a GND pin) and 146 to 150 and Pin

151 provides some overlap from pin 145 to 155 (156 and 157 are not I/O pins). These happen to be adjacent pin numbers, but the distance table shows that these are all adjacent pads as well.

Because each VREF can only sustain six I/O, the eight SSTL2-1 I/O pins should be spread evenly around each VREF pin.

Manual Placement Flow

1. Place I/O Standard attributes on all I/O
2. Pin lock I/Os and VREFs
3. Implement design
4. Verify VREF placement

Step 1. Place I/O Standard Attributes

This can be done by utilizing the Constraints Editor GUI or by editing the UCF in any text editor.

The syntax for assigning an I/O standard to a net in the UCF is:

NET <*signal name*> IOSTANDARD = <*I/O standard attribute name*>;

Example:

NET data_in IOSTANDARD=HSTL_I;

This can also be done in the source files. For more details, please see Xilinx **XAPP378:Using CoolRunner-II Advanced Features**.

If the design is not yet complete,a user may find that the unused inputs or outputs are removed from the design. This can be easily resolved by creating some "dummy" logic that routes to an output. This will prevent the pins from being trimmed and allow the fitter to account for them when assigning VREF pins. An example of "dummy" logic can be found on page 2 of this document.

Step 2. Pin Lock I/Os and VREFs

Location constraints may be created by using the Constraints Editor or by editing the UCF in any text editor. At the time of this writing, VREF constraints may **not** be entered using the Constraints Editor.

The syntax for assigning pin locations in the UCF is:

NET <signal name> LOC = Pxx;

For pinned packages (VQ, PQ, TQ), xx is the pin number. For ball-grid packages (CP, FT, FG) remove the P and replace xx with the pin number.

Example:

Pinned package: NET data_in LOC = P12;

Ball-grid package: NET data_in LOC=M10;

Assign VREF pins in the UCF using the following syntax.

CONFIG VREF = Pxx;

For pinned packages (VQ, PQ, TQ), xx is the pin number. For ball-grid packages (CP, FT, FG) remove the P and replace xx with the pin number.

Example:

Pinned package: CONFIG VREF=P9;

Ball-grid package: CONFIG VREF=B2;

Step 3. Implement Design

In this phase, the Xilinx CPLD software will take the constraints given (I/O standards, pin locations, device and package) and fit the design. Design Rule Checking (DRC) is done at this point to verify the following:

- There are not more I/O standards than there are I/O banks available in the device
- There are not multiple I/O standards within the same I/O bank
- That there are sufficient VREF pins per I/O bank

If there are no DRC errors, the pinout and VREF information is then written into the report file [designname].RPT.

Step 4. Verify VREF Placement

After the CPLD software has fit the design, it is recommended to check the VREF placement as well as to verify that no **new** VREF pins were added. The CPLD software will add VREF pins if the VREF pins provided by the user are insufficient.

Conclusion

CoolRunner-II CPLDs allow maximum flexibility with user-assignable VREF pins. However, this flexibility is not without cost, as manual placement requires that users spend some time to understand placement rules. Failure to understand and comply with these rules will result in unnecessary VREF pins or the inability to generate a programming file. Software placement needs minimal user interaction and is the recommended flow for most designers.

Appendix A: Pad Distance Tables

Table 1: **CoolRunner-II 128-Macrocell CPLD Pad Distance Table**

TQ144	CP132	VQ100	Pin Type	Distance	Bank
1	A2	.	VCC	110	2
2	A1	1	I/O/GTS2	111	2
3	B2	2	I/O/GTS3	112	2
4	B1	.	I/O	113	2
5	C3	3	I/O/GTS0	114	2
6	C2	4	I/O/GTS1	115	2
7	C1	.	I/O	116	2
8	D3	5	VAUX	117	2
9	D2	6	I/O	118	2
10	D1	7	I/O	119	2
11	E3	8	I/O	120	2
12	E2	9	I/O	121	2
13	E1	10	I/O	122	2
14	F3	11	I/O	123	2
15	F2	12	I/O	124	2
16	F1	.	I/O	125	2
17	G1	13	I/O	126	2
19	G2	.	I/O	1	2

Table 1: **CoolRunner-II 128-Macrocell CPLD Pad Distance Table *(Continued)***

TQ144	CP132	VQ100	Pin Type	Distance	Bank
21	G3	14	I/O	2	2
22	H1	15	I/O	3	2
23	H2	16	I/O	4	2
24	H3	17	I/O	5	2
25	J1	18	I/O	6	1
26	J2	19	I/O	7	1
27	J3	20	VCCIO	8	1
28	K1	.	I/O	9	1
29	K2	21	GND	10	1
30	K3	22	I/O/GCK0	11	1
32	L2	23	I/O/GCK1	12	1
35	M2	24	I/O/CDR	13	1
36	N1	25	GND	14	1
37	P1	26	VCC	15	1
38	N2	27	I/O/GCK2	16	1
39	P2	28	I/O/DGE	17	1
40	M3	.	I/O	18	1
41	N3	.	I/O	19	1
43	P3	29	I/O	20	1
45	M4	30	I/O	21	1
47	P4	31	GND	22	1
49	M5	32	I/O	23	1
50	N5	33	I/O	24	1
51	P5	34	I/O	25	1
52	M6	35	I/O	26	1
53	N6	36	I/O	27	1
54	P6	37	I/O	28	1
55	P7	38	VCCIO	29	1
56	N7	39	I/O	30	1
57	M7	40	I/O	31	1
58	P8	41	I/O	32	1
59	N8	42	I/O	33	1
60	M8	43	I/O	34	1
61	P9	44	I/O	35	1
62	N9	.	GND	36	1
63	M9	45	TDI	37	1

Table 1: **CoolRunner-II 128-Macrocell CPLD Pad Distance Table *(Continued)***

TQ144	CP132	VQ100	Pin Type	Distance	Bank
64	P10	46	I/O	38	1
65	N10	47	TMS	39	1
67	M10	48	TCK	40	1
68	P11	.	I/O	41	1
69	N11	49	I/O	42	1
70	M11	.	I/O	43	1
71	P12	50	I/O	44	1
72	N12	.	GND	45	1
73	P13	51	VCCIO	46	1
74	P14	52	I/O	47	1
76	N13	53	I/O	48	1
77	N14	.	I/O	49	1
78	M12	54	I/O	50	1
79	M13	.	I/O	51	1
80	M14	55	I/O	52	1
81	L12	.	I/O	53	1
82	L13	56	I/O	54	1
83	L14	.	I/O	55	1
84	K12	57	VCC	56	2
85	K13	58	I/O	57	2
86	K14	59	I/O	58	2
87	J12	60	I/O	59	2
88	J13	61	I/O	60	2
89	J14	.	GND	61	2
90	H14	62	GND	62	2
91	H13	63	I/O	63	2
92	H12	64	I/O	64	2
93	G14	.	VCCIO	65	2
94	G13	65	I/O	66	2
95	G12	66	I/O	67	2
96	F14	67	I/O	68	2
97	F13	.	I/O	69	2
98	F12	68	I/O	70	2
99	E14	69	GND	71	2
100	E13	.	I/O	72	2
101	E12	70	I/O	73	2

Table 1: **CoolRunner-II 128-Macrocell CPLD Pad Distance Table *(Continued)***

TQ144	CP132	VQ100	Pin Type	Distance	Bank
102	D14	71	I/O	74	2
103	D13	72	I/O	75	2
104	D12	73	I/O	76	2
105	C14	74	I/O	77	2
108	B14	75	GND	78	2
109	A14	.	VCCIO	79	2
110	B13	76	I/O	80	2
111	A13	.	I/O	81	2
112	C12	77	I/O	82	2
113	B12	78	I/O	83	2
115	A12	.	I/O	84	2
116	C11	79	I/O	85	2
117	B11	80	I/O	86	2
118	A11	81	I/O	87	2
119	C10	.	I/O	88	2
120	A10	82	I/O	89	2
121	C9	.	I/O	90	2
122	B9	83	TDO	91	2
123	A9	84	GND	92	2
124	A8	85	I/O	93	2
125	B8	86	I/O	94	2
126	C8	87	I/O	95	2
127	A7	88	VCCIO	96	2
128	B7	89	I/O	97	2
129	C7	90	I/O	98	2
130	A6	91	I/O	99	2
131	B6	92	I/O	100	2
132	C6	93	I/O	101	2
133	A5	.	I/O	102	2
134	B5	94	I/O	103	2
136	C5	95	I/O	104	2
138	A4	96	I/O	105	2
140	B4	97	I/O	106	2
141	C4	98	VCCIO	107	2
143	A3	99	I/O/GSR	108	2
144	B3	100	GND	109	2

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table**

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
D3	3	2	A1	1	I/O/GTS2	200	2
C3	4	.	.	.	I/O	201	2
E3	5	3	B2	2	I/O/GTS3	202	2
B2	6	4	B1	.	I/O	203	2
D4	7	5	C3	3	I/O/GTS0	204	2
D2	8	.	.	.	I/O	205	2
E5	9	6	C2	4	I/O/GTS1	206	2
B1	10	7	C1	.	I/O	207	2
F4	11	8	D3	5	VAUX	208	2
E4	12	9	D2	6	I/O	209	2
F11	13	.	.	.	GND	210	2
C1	14	10	.	7	I/O	211	2
E2	.	.	D1	.	I/O	212	2
F7	.	.	.	.	VCCIO	213	2
F2	15	11	E3	8	I/O	214	2
F3	16	12	.	9	I/O	215	2
G4	17	13	E2	10	I/O	216	2
G3	18	14	E1	.	I/O	217	2
F5	19	15	F3	11	I/O	218	2
G5	20	16	F2	12	I/O	219	2
H2	21	17	F1	.	I/O	220	2
H4	22	.	G1	13	I/O	221	2
H3	23	18	.	.	I/O	222	2
H1	.	.	.	.	I/O	223	2
F6	24	.	.	.	GND	224	2
H5	25	.	.	.	I/O	225	2
F8	26	.	.	.	VCCIO	226	2
J1	.	19	.	.	I/O	1	1
J5	.	20	G2	.	I/O	2	1
J2	27	21	G3	14	I/O	3	1
J3	28	22	H1	15	I/O	4	1
K1	29	23	H2	16	I/O	5	1
J4	30	24	H3	17	I/O	6	1
K2	31	25	J1	18	I/O	7	1
K5	32	26	J2	19	I/O	8	1

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
J6	33	27	J3	20	VCCIO	9	1
L1	34	.	.	.	I/O	10	1
K3	35	.	.	.	I/O	11	1
G10	.	.	.	.	GND	12	1
L2	36	.	.	.	I/O	13	1
K4	37	.	.	.	I/O	14	1
L5	38	.	K1	.	I/O	15	1
M1	39	.	.	.	I/O	16	1
L4	40	28	.	.	I/O	17	1
N1	41	.	.	.	I/O	18	1
G7	42	29	K2	21	GND	19	1
L3	43	.	.	.	I/O	20	1
M2	44	30	K3	22	I/O/GCK0	21	1
P1	45	31	L1	.	I/O	22	1
M3	46	32	L2	23	I/O/GCK1	23	1
N2	47	.	.	.	I/O	24	1
N4	48	33	.	.	I/O	25	1
R1	49	.	L3	.	I/O	26	1
N3	50	34	M1	.	I/O	27	1
P2	51	35	M2	24	I/O/CDR	28	1
G8	52	36	N1	25	GND	29	1
P3	53	37	P1	26	VCC	30	1
P4	54	.	.	.	I/O	31	1
P5	55	38	N2	27	I/O/GCK2	32	1
R2	56	.	.	.	I/O	33	1
T1	57	.	.	.	I/O	34	1
T2	58	39	P2	28	I/O/DGE	35	1
K6	59	.	.	.	VCCIO	36	1
N5	60	40	M3	.	I/O	37	1
R4	61	41	N3	29	I/O	38	1
M5	62	42	P3	.	I/O	39	1
R5	63	43	M4	30	I/O	40	1
R6	64	44	N4	.	I/O	41	1
N6	65	45	.	.	I/O	42	1
R3	66	46	.	.	I/O	43	1
M6	67	.	.	.	I/O	44	1

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
G9	68	47	P4	31	GND	45	1
T3	69	48	.	.	I/O	46	1
P6	70	49	.	32	I/O	47	1
T4	71	50	M5	33	I/O	48	1
P7	72	51	N5	34	I/O	49	1
T5	73	52	P5	35	I/O	50	1
N7	74	.	M6	36	I/O	51	1
R7	75	.	N6	37	I/O	52	1
M7	76	.	.	.	I/O	53	1
T6	77	53	P6	.	I/O	54	1
N8	78	54	.	.	I/O	55	1
L7	79	55	P7	38	VCCIO	56	1
T7	80	.	.	.	I/O	57	1
H10	81	.	.	.	GND	58	1
R8	82	56	N7	39	I/O	59	1
P8	83	57	M7	40	I/O	60	1
T8	84	58	P8	41	I/O	61	1
M8	85	59	.	42	I/O	62	1
N9	86	60	N8	43	I/O	63	1
R9	87	.	.	.	I/O	64	1
T10	88	.	M8	.	I/O	65	1
R10	89	.	.	.	I/O	66	1
P10	90	.	.	.	I/O	67	1
N10	91	61	P9	.	I/O	68	1
L8	92	.	.	.	VCCIO	69	1
M11	.	.	.	44	I/O	70	1
H7	93	62	N9	.	GND	71	1
R11	94	63	M9	45	TDI	72	1
N11	95	64	P10	46	I/O	73	1
N12	96	65	N10	47	TMS	74	1
R12	97	66	.	.	I/O	75	1
P12	98	67	M10	48	TCK	76	1
T15	99	.	.	.	I/O	77	1
R14	.	68	P11	.	I/O	78	1
N13	100	.	N11	49	I/O	79	1
R13	101	69	M11	.	I/O	80	1

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
P13	102	70	P12	50	I/O	81	1
P14	103	71	.	.	I/O	82	1
H8	104	72	N12	.	GND	83	1
J11	105	73	P13	51	VCCIO	84	1
P15	106	74	P14	52	I/O	85	1
R15	107	75	N13	.	I/O	86	1
T16	108	76	N14	53	I/O	87	1
N14	109	77	M12	.	I/O	88	1
R16	110	.	.	54	I/O	89	1
N15	111	78	M13	.	I/O	90	1
M15	112	79	.	55	I/O	91	1
M13	113	80	M14	.	I/O	92	1
P16	114	81	.	56	I/O	93	1
N16	115	82	L12	.	I/O	94	1
L14	116	.	.	.	I/O	95	1
M14	117	.	L13	.	I/O	96	1
L15	118	.	.	.	I/O	97	1
L13	119	83	L14	.	I/O	98	1
M12	120	.	.	.	I/O	99	1
M16	121	.	.	.	I/O	100	1
K14	122	.	.	.	I/O	101	1
L16	123	.	.	.	I/O	102	1
K13	124	84	K12	57	VCC	103	1
K15	125	85	K13	58	I/O	104	1
L12	126	86	K14	59	I/O	105	1
K16	127	87	J12	60	I/O	106	1
J14	128	88	J13	61	I/O	107	1
H9	129	89	J14	.	GND	108	1
J10	130	90	H14	62	GND	109	1
J15	.	91	H13	63	I/O	110	1
J13	131	92	H12	64	I/O	111	1
K11	132	93	G14	.	VCCIO	112	1
G6	133	.	.	.	VCCIO	113	2
J12	.	.	.	.	I/O	114	2
H15	134	94	.	65	I/O	115	2
H14	135	95	.	66	I/O	116	2

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
G16	136	96	G13	67	I/O	117	2
H13	137	97	G12	.	I/O	118	2
G15	138	98	F14	68	I/O	119	2
H16	139	.	F13	.	I/O	120	2
F16	140	.	F12	.	I/O	121	2
J7	141	99	E14	69	GND	122	2
H12	142	.	.	.	I/O	123	2
E16	143	.	.	.	I/O	124	2
G14	144	100	.	.	I/O	125	2
F15	145	.	.	.	I/O	126	2
G13	146	101	E13	.	I/O	127	2
E15	147	.	.	.	I/O	128	2
F13	148	102	E12	.	I/O	129	2
F14	149	.	.	.	I/O	130	2
C16	150	103	D14	70	I/O	131	2
E14	151	.	.	.	I/O	132	2
D15	152	104	D13	71	I/O	133	2
B16	153	105	D12	72	I/O	134	2
G11	154	106	C14	73	I/O	135	2
C14	155	107	C13	74	I/O	136	2
J8	156	108	B14	75	GND	137	2
H6	157	109	A14	.	VCCIO	138	2
B15	158	110	B13	76	I/O	139	2
A16	159	111	A13	77	I/O	140	2
B13	160	112	C12	78	I/O	141	2
B14	161	113	B12	79	I/O	142	2
C13	162	.	.	.	I/O	143	2
A15	163	114	A12	80	I/O	144	2
C12	164	.	.	.	I/O	145	2
B12	165	115	C11	81	I/O	146	2
D13	166	.	.	.	I/O	147	2
A14	167	116	B11	82	I/O	148	2
E13	168	117	.	.	I/O	149	2
A13	169	118	A11	.	I/O	150	2
C11	170	119	.	.	I/O	151	2
A12	171	.	C10	.	I/O	152	2

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
F10	172	.	.	.	VCCIO	153	2
J9	.	.	.	.	GND	154	2
B11	.	.	B10	.	I/O	155	2
D11	173	.	.	.	I/O	156	2
A11	174	.	A10	.	I/O	157	2
D10	175	.	.	.	I/O	158	2
B10	.	120	C9	.	I/O	159	2
E12	.	121	.	.	I/O	160	2
A10	176	122	B9	83	TDO	161	2
K10	177	123	A9	84	GND	162	2
F12	178	124	A8	85	I/O	163	2
B9	179	125	B8	86	I/O	164	2
C9	180	126	C8	87	I/O	165	2
F9	181	127	A7	88	VCCIO	166	2
C10	182	128	.	89	I/O	167	2
A9	183	129	.	.	I/O	168	2
D9	184	130	.	.	I/O	169	2
E10	185	131	B7	90	I/O	170	2
E11	186	.	C7	.	I/O	171	2
A8	187	132	A6	91	I/O	172	2
C8	188	.	B6	.	I/O	173	2
B8	189	.	.	92	I/O	174	2
K7	190	.	.	.	GND	175	2
D8	191	.	C6	.	I/O	176	2
A7	192	133	.	93	I/O	177	2
E9	193	.	A5	.	I/O	178	2
B7	194	134	.	.	I/O	179	2
D7	195	135	B5	.	I/O	180	2
A6	196	136	.	.	I/O	181	2
C7	197	.	C5	.	I/O	182	2
B6	198	.	.	.	I/O	183	2
E8	199	137	A4	94	I/O	184	2
A5	200	138	.	95	I/O	185	2
B5	201	139	.	96	I/O	186	2
A4	202	140	B4	97	I/O	187	2
A3	203	.	.	.	I/O	188	2

Table 2: **CoolRunner-II 256-Macrocell CPLD Pad Distance Table *(Continued)***

FT256	PQ208	TQ144	CP132	VQ100	Pin Type	Distance	Bank
H11	204	141	C4	98	VCCIO	189	2
A2	205	142	.	.	I/O	190	2
C4	206	143	A3	99	I/O/GSR	191	2
K8	207	144	B3	100	GND	192	2
B4	208	.	.	.	I/O	193	2
D5	1	1	A2	.	VCC	194	2
B3	2	.	.	.	I/O	195	2
K9	.	.	.	.	GND	196	2
L11	.	.	.	.	GND	197	2
L6	.	.	.	.	GND	198	2
D12	.	.	.	.	VCC	199	2

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table**

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
D5	F11	207	144	GND	250	2
A1	B4	208	.	I/O	251	2
D4	D5	1	1	VCC	252	2
C3	B3	2	.	I/O	253	2
D3	D3	3	2	I/O/GTS2	254	2
B2	C3	4	.	I/O	255	2
B1	E3	5	3	I/O/GTS3	256	2
C2	B2	6	4	I/O	257	2
C1	D4	7	5	I/O/GTS0	258	2
D2	A1	.	.	I/O	259	2
F4	D2	8	.	I/O	260	2
E2	C2	.	.	I/O	261	2
E1	E5	9	6	I/O/GTS1	262	2
F2	B1	10	7	I/O	263	2
F1	F4	11	8	VAUX	264	2
G4	E4	12	9	I/O	265	2
G3	C1	.	10	I/O	266	2
D18	F6	13	.	GND	267	2
G2	E2	14	11	I/O	268	2
G1	F2	15	12	I/O	269	2

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
K9	G6	.	.	VCCIO	270	2
H4	E6	16	.	I/O	271	2
H3	F3	17	.	I/O	272	2
H2	D1	18	.	I/O	273	2
H1	G4	19	.	I/O	274	2
J3	E1	20	.	I/O	275	2
J2	G3	21	.	I/O	276	2
J1	G2	22	.	I/O	277	2
K3	F5	.	13	I/O	278	2
K2	F1	23	14	I/O	279	2
K1	G5	.	15	I/O	280	2
L1	H2	.	.	I/O	281	2
L3	H4	.	.	I/O	282	2
L2	G1	.	16	I/O	283	2
M1	H3	.	17	I/O	284	2
M2	H1	.	.	I/O	285	2
E4	G10	24	.	GND	286	2
M3	H5	25	18	I/O	287	2
L9	H6	26	.	VCCIO	288	2
N1	.	.	.	I/O	1	1
N2	.	.	.	I/O	2	1
N3	J1	.	.	I/O	3	1
P1	J5	.	.	I/O	4	1
P2	J2	27	19	I/O	5	1
P3	J3	28	20	I/O	6	1
P4	K1	29	21	I/O	7	1
R1	J4	30	22	I/O	8	1
R2	K2	.	23	I/O	9	1
R3	K5	31	24	I/O	10	1
R4	.	.	25	I/O	11	1
T1	.	32	26	I/O	12	1
M9	J6	33	27	VCCIO	13	1
E19	G7	.	.	GND	14	1
T2	L1	34	.	I/O	15	1
T3	K3	35	.	I/O	16	1
T4	L2	36	.	I/O	17	1

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
U1	K4	37	.	I/O	18	1
U2	L5	38	.	I/O	19	1
U3	M1	39	.	I/O	20	1
V1	L4	40	28	I/O	21	1
V2	N1	41	.	I/O	22	1
J9	G8	42	29	GND	23	.
U4	L3	43	.	I/O	24	1
V3	M2	44	30	I/O/GCK0	25	1
W1	M4	45	31	I/O	26	1
W2	P1	.	.	I/O	27	1
Y1	M3	46	32	I/O/GCK1	28	1
N9	K6	.	.	VCCIO	29	1
Y2	N2	47	33	I/O	30	1
W4	N4	48	34	I/O	31	1
AA1	R1	49	.	I/O	32	1
AA2	N3	50	.	I/O	33	1
AB2	P2	51	35	I/O/CDR	34	1
J14	G9	52	36	GND	35	1
AA3	P3	53	37	VCC	36	1
Y4	P4	54	.	I/O	37	1
AB3	P5	55	38	I/O/GCK2	38	1
AA4	R2	56	.	I/O	39	1
Y5	T1	57	.	I/O	40	1
AA5	T2	58	39	I/O/DGE	41	1
P10	L7	59	.	VCCIO	42	1
AB4	.	.	.	I/O	43	1
W6	N5	60	40	I/O	44	1
AB5	.	.	41	I/O	45	1
Y6	R4	61	42	I/O	46	1
AA6	M5	.	43	I/O	47	1
AB6	.	62	44	I/O	48	1
W7	R5	63	45	I/O	49	1
Y7	.	.	.	I/O	50	1
AA7	R6	64	46	I/O	51	1
AB7	N6	65	.	I/O	52	1
W8	R3	66	.	I/O	53	1

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
Y8	M6	67	.	I/O	54	1
K10	H10	68	47	GND	55	1
AA8	.	69	48	I/O	56	1
AB8	T3	70	49	I/O	57	1
Y9	P6	71	50	I/O	58	1
AA9	T4	72	51	I/O	59	1
AB9	P7	73	52	I/O	60	1
W10	T5	74	53	I/O	61	1
Y10	N7	75	.	I/O	62	1
AA10	R7	76	54	I/O	63	1
AB10	M7	77	.	I/O	64	1
AB11	.	.	.	I/O	65	1
W11	.	.	.	I/O	66	1
AA11	.	.	.	I/O	67	1
Y11	T6	78	.	I/O	68	1
P11	L8	79	55	VCCIO	69	1
AB12	N8	.	.	I/O	70	3
AA12	T7	.	.	I/O	71	3
Y12	R8	80	56	I/O	72	3
W12	P8	.	.	I/O	73	3
AB13	T8	.	57	I/O	74	3
K11	H7	81	.	GND	75	3
AA13	M8	82	.	I/O	76	3
Y13	.	83	.	I/O	77	3
AB14	.	.	.	I/O	78	3
AA14	T9	84	58	I/O	79	3
Y14	N9	.	.	I/O	80	3
W14	P9	.	.	I/O	81	3
AB15	R9	85	.	I/O	82	3
AA15	M9	86	59	I/O	83	3
Y15	T10	87	.	I/O	84	3
W15	M10	88	60	I/O	85	3
AB16	R10	.	.	I/O	86	3
AA16	T11	89	.	I/O	87	3
Y16	P10	90	.	I/O	88	3
AB17	T12	91	61	I/O	89	3

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
K12	H8	.	.	GND	90	3
P12	L9	92	.	VCCIO	91	3
AA17	N10	.	.	I/O	92	3
AB18	T13	.	.	I/O	93	3
K13	H9	93	62	GND	94	3
AA18	M11	.	.	I/O	95	3
Y17	P11	.	.	I/O	96	3
AB19	R11	94	63	TDI	97	3
AA19	N11	95	64	I/O	98	3
Y18	T14	.	.	I/O	99	3
AB20	N12	96	65	TMS	100	3
AA20	R12	97	66	I/O	101	3
Y19	P12	98	67	TCK	102	3
W19	T15	99	68	I/O	103	3
AB21	R14	100	69	I/O	104	3
AA21	N13	101	70	I/O	105	3
AB22	R13	102	71	I/O	106	3
AA22	P13	103	.	I/O	107	3
Y20	P14	.	.	I/O	108	3
L10	J10	104	72	GND	109	3
P13	L10	105	73	VCCIO	110	3
Y21	P15	106	74	I/O	111	3
W20	R15	107	75	I/O	112	3
W21	T16	108	76	I/O	113	3
Y22	N14	109	77	I/O	114	3
W22	R16	110	78	I/O	115	3
V20	N15	111	79	I/O	116	3
V21	M15	112	.	I/O	117	3
U19	M13	113	.	I/O	118	3
V22	P16	114	80	I/O	119	3
U20	N16	115	.	I/O	120	3
U21	L14	116	81	I/O	121	3
U22	M14	117	.	I/O	122	3
T19	L15	118	.	I/O	123	3
T20	L13	119	82	I/O	124	3
T21	M12	120	.	I/O	125	3

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
L11	J7	.	.	GND	126	3
T22	M16	121	.	I/O	127	3
R21	K14	122	83	I/O	128	3
R22	.	123	.	I/O	129	3
P20	L16	.	.	I/O	130	3
N20	K13	124	84	VCC	131	3
P21	K15	125	.	I/O	132	3
N14	K11	.	.	VCCIO	133	3
N19	L12	126	85	I/O	134	3
N21	.	127	86	I/O	135	3
N22	K16	.	87	I/O	136	3
M22	J14	128	88	I/O	137	3
L12	J8	129	89	GND	138	3
L13	J8	130	90	GND	139	3
M19	J15	.	91	I/O	140	3
M20	J13	131	92	I/O	141	3
M21	.	.	.	I/O	142	3
L22	.	.	.	I/O	143	3
M14	J11	132	93	VCCIO	144	3
L14	H11	133	.	VCCIO	145	4
L21	J16	.	.	I/O	146	4
L20	K12	134	.	I/O	147	4
L19	J12	135	.	I/O	148	4
K22	H15	136	94	I/O	149	4
K21	H14	137	95	I/O	150	4
K20	G16	138	96	I/O	151	4
K19	H13	139	97	I/O	152	4
J22	.	140	98	I/O	153	4
M10	J9	141	99	GND	154	4
J21	.	142	.	I/O	155	4
J20	G15	.	.	I/O	156	4
J19	.	143	100	I/O	157	4
H22	.	.	.	I/O	158	4
H21	.	144	101	I/O	159	4
H19	H16	.	.	I/O	160	4
G22	F16	145	.	I/O	161	4

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
G21	H12	.	.	I/O	162	4
G20	E16	146	.	I/O	163	4
G19	G14	147	102	I/O	164	4
F22	F15	148	.	I/O	165	4
F21	G13	149	103	I/O	166	4
F20	E15	150	.	I/O	167	4
E22	F13	.	.	I/O	168	4
M11	K10	.	.	GND	169	4
K14	H11	.	.	VCCIO	170	4
E21	D16	151	.	I/O	171	4
F19	F14	152	104	I/O	172	4
E20	C16	.	.	I/O	173	4
D22	E14	153	105	I/O	174	4
D21	D15	154	106	I/O	175	4
C22	G12	155	107	I/O	176	4
M12	K7	156	108	GND	177	4
K14	F10	157	109	VCCIO	178	4
D20	C15	158	110	I/O	179	4
D19	D14	159	111	I/O	180	4
C21	B16	.	.	I/O	181	4
C20	G11	.	.	I/O	182	4
B22	C14	160	112	I/O	183	4
B21	B15	161	113	I/O	184	4
A22	A16	.	.	I/O	185	4
A21	B13	162	114	I/O	186	4
J13	F10	.	.	VCCIO	187	4
M13	K8	.	.	GND	188	4
A20	D12	.	.	VCC	189	4
B20	B14	163	115	I/O	190	4
C19	C13	.	.	I/O	191	4
B19	A15	.	.	I/O	192	4
C18	C12	164	.	I/O	193	4
B18	B12	.	.	I/O	194	4
A19	D13	165	116	I/O	195	4
D17	A14	166	.	I/O	196	4
A18	E13	.	.	I/O	197	4

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
C17	A13	167	117	I/O	198	4
B17	C11	168	.	I/O	199	4
D16	A12	169	118	I/O	200	4
C16	B11	.	.	I/O	201	4
B16	D11	170	119	I/O	202	4
D15	A11	171	120	I/O	203	4
J13	F9	172	.	VCCIO	204	4
C15	D10	173	.	I/O	205	4
B15	B10	174	121	I/O	206	4
D14	E12	175	.	I/O	207	4
C14	A10	176	122	TDO	208	4
B14	.	.	.	I/O	209	4
C13	F12	.	.	I/O	210	4
N10	K9	177	123	GND	211	4
A13	B9	178	124	I/O	212	4
D12	C9	179	125	I/O	213	4
C12	C10	180	126	I/O	214	4
J12	F9	181	127	VCCIO	215	4
B11	A9	.	.	I/O	216	4
A10	D9	182	128	I/O	217	4
B10	E10	183	129	I/O	218	2
C10	E11	184	130	I/O	219	2
D10	A8	185	.	I/O	220	2
A9	C8	186	131	I/O	221	2
B9	B8	187	.	I/O	222	2
C9	D8	188	.	I/O	223	2
D9	A7	189	.	I/O	224	2
A8	E9	.	132	I/O	225	2
B8	B7	.	133	I/O	226	2
C8	D7	.	.	I/O	227	2
N11	L11	190	.	GND	228	2
D8	A6	.	134	I/O	229	2
A7	C7	191	.	I/O	230	2
B7	B6	.	.	I/O	231	2
C7	E8	192	.	I/O	232	2
D7	A5	193	135	I/O	233	2

Table 3: **CoolRunner-II 384-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	TQ144	PinType	Distance	Bank
J11	F8	.	.	VCCIO	234	2
N12	L6	.	.	GND	235	2
A6	D6	194	136	I/O	236	2
B6	B5	195	137	I/O	237	2
C6	C6	196	138	I/O	238	2
A5	.	197	.	I/O	239	2
D6	A4	198	.	I/O	240	2
A4	.	199	.	I/O	241	2
A3	E7	200	.	I/O	242	2
B5	.	201	.	I/O	243	2
C5	A3	202	139	I/O	244	2
B4	C5	203	140	I/O	245	2
C4	.	.	.	I/O	246	2
J10	F7	204	141	VCCIO	247	2
B3	A2	205	142	I/O	248	2
A2	C4	206	143	I/O/GSR	249	2

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table**

FG324	FT256	PQ208	Pin Type	Distance	Bank
D3	D3	3	I/O/GTS2	285	2
B2	C3	4	I/O	286	2
B1	E3	5	I/O/GTS3	287	2
C2	B2	6	I/O	288	2
C1	D4	7	I/O/GTS0	289	2
E3	.	.	VCC	290	.
D2	A1	.	I/O	291	2
D1	.	8	I/O	292	2
F4	D2	.	I/O	293	2
F3	.	.	I/O	294	2
E2	C2	.	I/O	295	2
E1	E5	9	I/O/GTS1	296	2
F2	B1	10	I/O	297	2
F1	F4	11	VAUX	298	.
G4	E4	12	I/O	299	2
D5	F11	13	GND	300	.
G3	C1	.	I/O	301	2

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
G2	E2	14	I/O	302	2
G1	F2	.	I/O	303	2
J10	F7	.	VCCIO	304	2
H4	E6	15	I/O	305	2
H3	F3	.	I/O	306	2
H2	D1	16	I/O	307	2
H1	G4	17	I/O	308	2
J4	E1	18	I/O	309	2
J3	G3	19	I/O	310	2
J2	G2	20	I/O	311	2
J1	.	21	I/O	312	2
K4	F5	.	I/O	313	2
K3	.	.	I/O	314	2
K2	F1	.	I/O	315	2
K1	.	.	I/O	316	2
L1	G5	.	I/O	317	2
L4	H2	.	I/O	318	2
L3	.	22	I/O	319	2
L2	H4	23	I/O	320	2
M1	.	.	I/O	321	2
D18	F6	24	GND	322	.
M2	G1	.	I/O	323	2
M3	H3	25	I/O	324	2
M4	H1	.	I/O	325	2
J11	F8	26	VCCIO	326	2
N1	H5	.	I/O	327	2
N2	.	.	I/O	1	1
N3	.	.	I/O	2	1
N4	J1	27	I/O	3	1
P1	J5	28	I/O	4	1
P2	J2	29	I/O	5	1
P3	J3	30	I/O	6	1
P4	K1	.	I/O	7	1
E4	G10	.	GND	8	.
R1	J4	31	I/O	9	1
R2	K2	.	I/O	10	1

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
R3	K5	32	I/O	11	1
M9	J6	33	VCCIO	12	1
R4	L1	34	I/O	13	1
T1	K3	.	I/O	14	1
T2	.	35	I/O	15	1
T3	L2	36	I/O	16	1
T4	K4	.	I/O	17	1
U1	.	37	I/O	18	1
U2	L5	38	I/O	19	1
U3	M1	39	I/O	20	1
E19	G7	.	GND	21	.
V1	L4	40	I/O	22	1
V2	N1	41	I/O	23	1
J9	G8	42	GND	24	.
U4	L3	43	I/O	25	1
V3	M2	44	I/O/GCK0	26	1
W1	M4	.	I/O	27	1
W2	P1	45	I/O	28	1
Y1	M3	46	I/O/GCK1	29	1
W3	N2	.	I/O	30	1
Y2	N4	47	I/O	31	1
Y3	R1	.	I/O	32	1
N9	K6	.	VCCIO	33	1
W4	.	48	I/O	34	1
AA1	.	49	I/O	35	1
AB1	N3	50	I/O	36	1
AA2	.	.	I/O	37	1
AB2	P2	51	I/O/CDR	38	1
J14	G9	52	GND	39	.
AA3	P3	53	VCC	40	.
Y4	P4	54	I/O	41	1
AB3	P5	55	I/O/GCK2	42	1
AA4	R2	56	I/O	43	1
Y5	T1	57	I/O	44	1
AA5	T2	58	I/O/DGE	45	1
AB4	.	.	I/O	46	1

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
W6	N5	.	I/O	47	1
P10	L7	59	VCCIO	48	1
K10	H10	.	GND	49	.
AB5	R4	60	I/O	50	1
Y6	M5	61	I/O	51	1
AA6	R5	62	I/O	52	1
AB6	R6	63	I/O	53	1
W7	.	64	I/O	54	1
Y7	N6	65	I/O	55	1
AA7	.	66	I/O	56	1
AB7	R3	67	I/O	57	1
W8	.	.	I/O	58	1
Y8	M6	.	I/O	59	1
K11	H7	68	GND	60	.
AA8	.	.	I/O	61	1
AB8	T3	69	I/O	62	1
W9	P6	70	I/O	63	1
Y9	T4	71	I/O	64	1
AA9	P7	72	I/O	65	1
AB9	.	.	I/O	66	1
W10	T5	73	I/O	67	1
Y10	.	.	I/O	68	1
AA10	N7	74	I/O	69	1
AB10	.	.	I/O	70	1
AB11	R7	75	I/O	71	1
W11	M7	76	I/O	72	1
AA11	T6	77	I/O	73	1
Y11	.	.	I/O	74	1
AB12	.	78	I/O	75	1
AA12	.	.	I/O	76	1
P11	L8	79	VCCIO	77	1
Y12	.	.	I/O	78	1
W12	N8	.	I/O	79	3
AB13	T7	.	I/O	80	3
AA13	R8	80	I/O	81	3
K12	H8	81	GND	82	.

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
Y13	P8	82	I/O	83	3
W13	T8	.	I/O	84	3
AB14	M8	83	I/O	85	3
AA14	T9	.	I/O	86	3
Y14	N9	84	I/O	87	3
W14	P9	85	I/O	88	3
AB15	R9	86	I/O	89	3
AA15	M9	.	I/O	90	3
Y15	T10	87	I/O	91	3
W15	M10	88	I/O	92	3
AB16	R10	.	I/O	93	3
AA16	T11	89	I/O	94	3
Y16	P10	90	I/O	95	3
W16	T12	91	I/O	96	3
K13	H9	.	GND	97	.
M14	J11	92	VCCIO	98	3
AB17	.	.	I/O	99	3
AA17	.	.	I/O	100	3
AB18	N10	.	I/O	101	3
AA18	T13	.	I/O	102	3
Y17	M11	.	I/O	103	3
L10	J10	93	GND	104	.
W17	P11	.	I/O	105	3
AB19	R11	94	TDI	106	.
AA19	N11	.	I/O	107	3
Y18	T14	95	I/O	108	3
AB20	N12	96	TMS	109	.
AA20	R12	97	I/O	110	3
Y19	P12	98	TCK	111	.
W19	T15	99	I/O	112	3
AB21	R14	100	I/O	113	3
AA21	N13	101	I/O	114	3
AB22	R13	102	I/O	115	3
AA22	P13	103	I/O	116	3
Y20	P14	.	I/O	117	3
L11	J7	104	GND	118	.

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
N14	K11	105	VCCIO	119	3
Y21	P15	106	I/O	120	3
W20	R15	107	I/O	121	3
W21	T16	108	I/O	122	3
Y22	N14	109	I/O	123	3
W22	R16	110	I/O	124	3
V20	N15	111	I/O	125	3
V21	M15	112	I/O	126	3
U19	M13	113	I/O	127	3
V22	P16	114	I/O	128	3
U20	N16	115	I/O	129	3
U21	L14	116	I/O	130	3
U22	M14	117	I/O	131	3
T19	L15	118	I/O	132	3
L12	J8	.	GND	133	.
T20	L13	.	I/O	134	3
T21	M12	119	I/O	135	3
T22	M16	120	I/O	136	3
R19	K14	.	I/O	137	3
R20	.	.	I/O	138	3
P12	L10	.	VCCIO	139	3
R21	.	121	I/O	140	3
R22	.	.	I/O	141	3
P19	L16	.	I/O	142	3
P20	.	.	I/O	143	3
P21	.	122	I/O	144	3
P22	.	123	I/O	145	3
N19	.	.	I/O	146	3
L13	J9	.	GND	147	.
N20	K13	124	VCC	148	.
N21	K15	125	I/O	149	3
N22	L12	.	I/O	150	3
P13	L9	.	VCCIO	151	3
M22	.	.	I/O	152	3
M19	K16	126	I/O	153	3
M20	.	.	I/O	154	3

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
M21	.	127	I/O	155	3
L22	J14	128	I/O	156	3
L21	.	.	I/O	157	3
M10	K10	129	GND	158	.
V4	.	130	GND	159	.
L20	J15	.	I/O	160	3
L19	.	.	I/O	161	3
K22	J13	131	I/O	162	3
.	.	132	VCCIO	163	3
J12	F10	133	VCCIO	164	4
K21	J16	.	I/O	165	4
K20	K12	134	I/O	166	4
K19	J12	135	I/O	167	4
J22	H15	136	I/O	168	4
J21	H14	137	I/O	169	4
J20	G16	138	I/O	170	4
J19	H13	139	I/O	171	4
H22	G15	140	I/O	172	4
M11	K7	141	GND	173	.
H21	.	142	I/O	174	4
H20	H16	143	I/O	175	4
H19	F16	144	I/O	176	4
G22	H12	145	I/O	177	4
G21	E16	146	I/O	178	4
J13	F9	.	VCCIO	179	4
G20	G14	147	I/O	180	4
G19	F15	148	I/O	181	4
F22	G13	149	I/O	182	4
F21	E15	150	I/O	183	4
F20	F13	151	I/O	184	4
E22	D16	152	I/O	185	4
E21	F14	153	I/O	186	4
F19	C16	154	I/O	187	4
E20	E14	155	I/O	188	4
M12	K8	156	GND	189	.
K14	H11	157	VCCIO	190	4

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
D22	D15	.	I/O	191	4
D21	G12	.	I/O	192	4
C22	C15	.	I/O	193	4
D20	.	158	I/O	194	4
D19	D14	.	I/O	195	4
C21	.	.	I/O	196	4
C20	B16	159	I/O	197	4
B22	G11	.	I/O	198	4
B21	C14	.	I/O	199	4
A22	B15	160	I/O	200	4
A21	A16	161	I/O	201	4
B20	B13	162	I/O	202	4
C19	.	163	I/O	203	4
B19	.	164	I/O	204	4
M13	K9	.	GND	205	.
A20	D12	.	VCC	206	.
C18	B14	165	I/O	207	4
B18	C13	166	I/O	208	4
A19	A15	167	I/O	209	4
D17	C12	168	I/O	210	4
A18	B12	169	I/O	211	4
C17	D13	170	I/O	212	4
B17	A14	171	I/O	213	4
L14	.	172	VCCIO	214	4
A17	E13	173	I/O	215	4
D16	A13	.	I/O	216	4
C16	C11	.	I/O	217	4
B16	A12	.	I/O	218	4
A16	B11	.	I/O	219	4
D15	D11	.	I/O	220	4
C15	A11	.	I/O	221	4
B15	D10	.	I/O	222	4
A15	B10	174	I/O	223	4
D14	E12	175	I/O	224	4
C14	A10	176	TDO	225	.
B14	F12	.	I/O	226	4

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
N10	L11	177	GND	227	.
A14	.	178	I/O	228	4
D13	.	.	I/O	229	4
C13	.	.	I/O	230	4
P14	.	.	GND	231	.
B13	.	.	I/O	232	4
A13	.	.	I/O	233	4
A12	B9	179	I/O	234	4
D12	.	180	I/O	235	4
B12	C9	.	I/O	236	4
.	.	181	VCCIO	237	4
C12	.	182	I/O	238	4
A11	C10	.	I/O	239	4
B11	.	.	I/O	240	4
C11	A9	.	I/O	241	4
D11	.	.	I/O	242	4
A10	D9	.	I/O	243	4
B10	E10	183	I/O	244	2
C10	E11	184	I/O	245	2
D10	A8	185	I/O	246	2
A9	C8	186	I/O	247	2
B9	B8	187	I/O	248	2
C9	D8	188	I/O	249	2
D9	A7	189	I/O	250	2
A8	E9	.	I/O	251	2
N11	L6	190	GND	252	.
B8	.	191	I/O	253	2
C8	B7	.	I/O	254	2
D8	D7	192	I/O	255	2
K9	G6	.	VCCIO	256	2
A7	A6	.	I/O	257	2
B7	.	193	I/O	258	2
C7	C7	194	I/O	259	2
D7	B6	195	I/O	260	2
A6	E8	196	I/O	261	2
B6	A5	197	I/O	262	2

Table 4: **CoolRunner-II 512-Macrocell CPLD Pad Distance Table *(Continued)***

FG324	FT256	PQ208	Pin Type	Distance	Bank
C6	D6	198	I/O	263	2
L9	H6	.	VCCIO	264	2
N12	.	.	GND	265	.
A5	B5	199	I/O	266	2
D6	C6	200	I/O	267	2
A4	A4	.	I/O	268	2
A3	E7	201	I/O	269	2
B5	A3	202	I/O	270	2
C5	C5	.	I/O	271	2
B4	.	203	I/O	272	2
C4	A2	.	I/O	273	2
.	.	204	VCCIO	274	2
B3	.	205	I/O	275	2
A2	C4	206	I/O/GSR	276	2
N13	.	207	GND	277	.
A1	B4	208	I/O	278	2
P9	.	.	GND	279	.
D4	D5	1	VCC	280	.
C3	B3	2	I/O	281	2
V19	.	.	GND	282	.
W5	.	.	GND	283	.
W18	.	.	GND	284	.

Further Reading

Application Notes

http://www.xilinx.com/xapp/xapp375.pdf (Timing Model)
http://www.xilinx.com/xapp/xapp376.pdf (Logic Engine)
http://www.xilinx.com/xapp/xapp377.pdf (Low Power Design)
http://www.xilinx.com/xapp/xapp378.pdf (Advanced Features)
http://www.xilinx.com/xapp/xapp379.pdf (High Speed Design)
http://www.xilinx.com/xapp/xapp380.pdf (Cross Point Switch)
http://www.xilinx.com/xapp/xapp381.pdf (Demo Board)
http://www.xilinx.com/xapp/xapp382.pdf (I/O Characteristics)
http://www.xilinx.com/xapp/xapp383.pdf (Single Error Correction Double Error Detection)
http://www.xilinx.com/xapp/xapp384.pdf (DDR SDRAM Interface)
http://www.xilinx.com/xapp/xapp387.pdf (PicoBlaze Microcontroller)
http://www.xilinx.com/xapp/xapp388.pdf (On the Fly Reconfiguration)
http://www.xilinx.com/xapp/xapp389.pdf (Powering CoolRunner-II CPLDs)

http://www.xilinx.com/xapp/xapp393.pdf (8051 Microcontroller Interface)
http://www.xilinx.com/xapp/xapp394.pdf (Interfacing with Mobile SDRAM)
http://www.xilinx.com/xapp/xapp395.pdf (Using DataGATE)

CoolRunner-II Data Sheets

http://direct.xilinx.com/bvdocs/publications/ds090.pdf (CoolRunner-II Family Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds091.pdf (XC2C32 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds092.pdf (XC2C64 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds093.pdf (XC2C128 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds094.pdf (XC2C256 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds095.pdf (XC2C384 Datasheet)
http://direct.xilinx.com/bvdocs/publications/ds096.pdf (XC2C512 Datasheet)

CoolRunner-II White Papers

http://www.xilinx.com/publications/products/cool2/wp_pdf/wp165.pdf (Chip Scale Packaging)
http://www.xilinx.com/publications/whitepapers/wp_pdf/wp170.pdf (Security)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/05/03	1.0	Initial Xilinx release.
07/25/03	1.1	Changed XAPP # to from 398 to 399