XAPP434 (v2.2) October 13, 2006

Web Server Reference Design Using a PowerPC-Based Embedded System

Author: Martin Muggli, Matthew Ouellette, Sathyanarayanan Thammanur, Robert Armstrong, Jr.

Summary

This application note details an embedded system example design of a Web server running on a PowerPC™ core within a Xilinx Virtex™-4 FX FPGA. The system is designed using the Embedded Development Kit (EDK). The application note also explains how to set up a system as a Web client and how to connect to the Web server running on the PowerPC processor.

Hardware Requirements

- Xilinx ML403 Virtex-4 FX development board. This platform contains a Virtex-4 FX12 FPGA.
- JTAG Parallel 4 Cable or Platform USB Cable.
- Crossover Ethernet Cable.
- Crossover or null-modem RS-232 cable.

Software Requirements

- Embedded Development Kit (EDK) 8.2i or later
- ISE 8.2i SP1 or later
- Internet Explorer, Firefox, or Mozilla Web browser
- Web server EDK project (downloaded from Xilinx Web site). The project can be opened in the Xilinx Platform Studio (XPS), through which the Web server design can be customized and downloaded to the Xilinx FPGA.

  The MicroBlaze Web server design can be downloaded from:

  www.xilinx.com/bvdocs/appnotes/xapp434.zip

Introduction

The embedded system design used in this application note contains these components (see Figure 1).

- A PowerPC processor connected to 16 KB of BRAM memory over the Processor Local Bus (PLB).
- A UARTLite, an external SRAM memory interface, an Ethernet 10/100 MAC, an external DDR SDRAM memory interface, and a General Purpose I/O (GPIO), all connected to either the PLB or the On-chip Peripheral Bus (OPB) through a PLB2OPB Bridge.

All of the IP cores used in the design are described in the *Processor IP Reference Guide* included with the EDK.

In the design, four GPIO output bits are connected to LEDs (DS4, 5, 6, and 15) on the development board and five input GPIO bits are connected to the directional push buttons. In the design example, the Ethernet MAC is running at 100 Mb/s. To run the example the peer network connection needs to be set to 100 Mb/s. If your connection auto-negotiates to 1000 Mb/s, you will need to change the configuration of your PC network adapter to run at 100 Mb/s only.

Note: The 10/100 Ethernet MAC PLB peripheral (PLB_ETHERNET) used with this design is not a free core. An evaluation license is required to use the core; the evaluation license is included with the EDK. The evaluation version of the core includes built-in timeout circuitry that disables the core after a period of time.

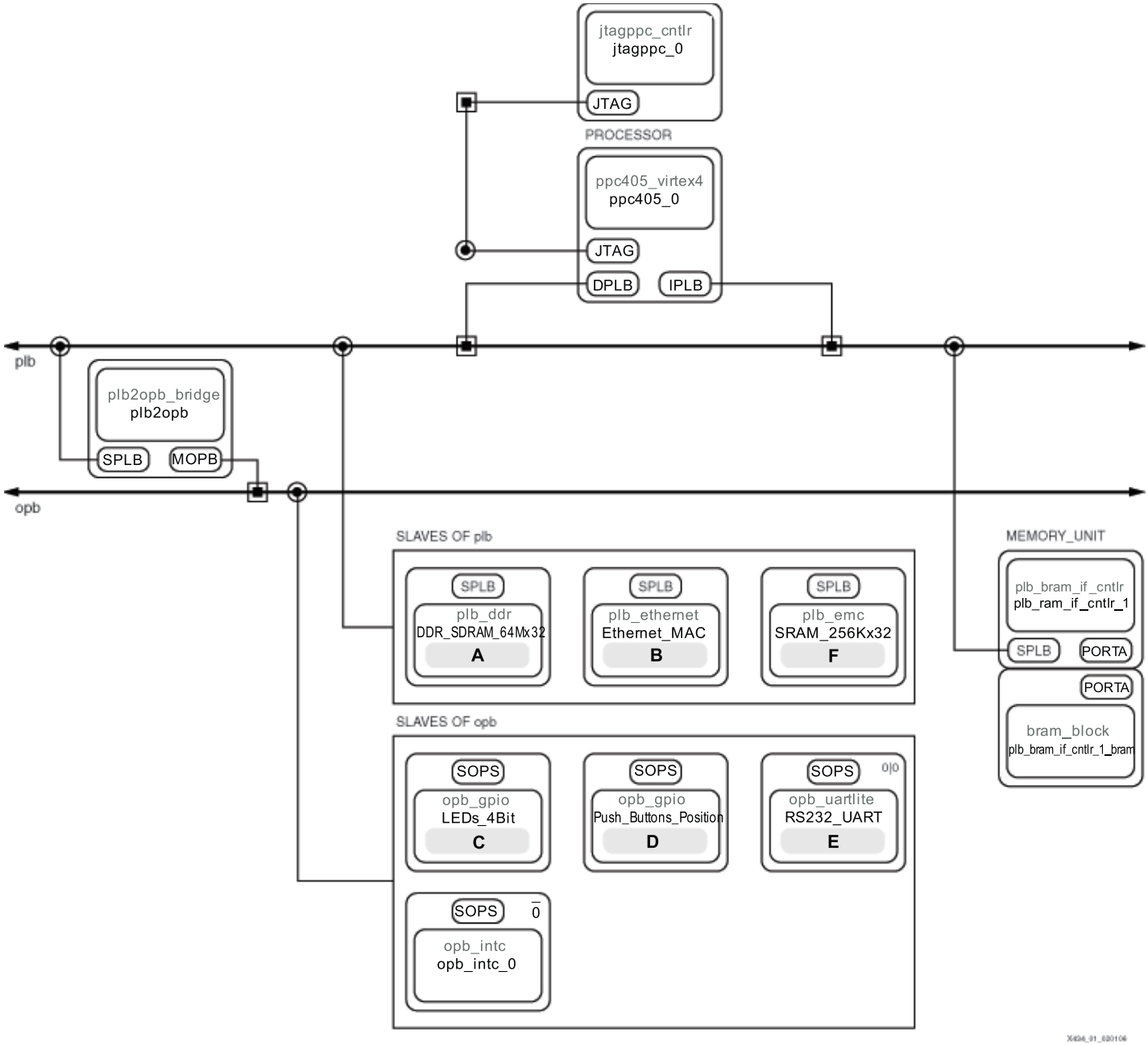

Figure 1: **PowerPC Web Server Design**

Table 1 shows the devices used in the Web server design and the memory map for the design.

Table 1: **Web Server Design Devices**

Device	Version	Address		Instances	Bus
		Low	High		
Virtex-4 PowerPC 405	1.01.a	N/A	N/A	ppc405_0	PLB
OPB UARTLite	1.00.b	0x40600000	0x4060ffff	RS232_Uart	OPB
OPB GPIO	3.01.b	0x40000000, 0x40020000	0x4000ffff, 0x4002ffff	LEDs_4Bit, Push_Buttons_ Position	Memory controller for block RAM
PLB DDR	1.11.a	0x00000000	0x03ffffff	DDR_SDRAM_ 64Mx32	PLB
PLB Ethernet	1.01.a	0x80400000	0x80400000	Ethernet_MAC	PLB
PLB EMC	2.00.a	0x06000000	0x060fffff	SRAM_256Kx32	PLB
PLB BRAM IF Controller	1.00.b	0xffffc000	0xffffffff	plb_bram_if_cntlr_ 1	PLB
JTAGPPC_CNTLR	2.00.a	N/A	N/A	jtagppc_0	N/A - Connects PowerPC processor to the JTAG chain
OPB INTC	1.00.c	0x41200000	0x4120ffff	opb_intc_0	OPB

The Web Server

The Web server source code is located in the project's /WebServer directory. The lwIP and XilMFS libraries accessed by the Web server design are included by LibGen, the Library Generator utility, and have been added to the project via the Software Platform Settings dialog.

On this system the Web server is running HTTP 1.1. A file system, built using the LibXil Memory File System library, stores the files for the Web page. The Web page source, including all HTML and images, is located in the project's /WebPage directory. The server listens for requests at port 80. Every request is processed, then replies are served up by the server to the client.

Operations Performed by the Web Server

The Web server in the design displays a Web page (see Figure 2) through which these operations can be performed:

- HEX-digit LED Display

  When a HEX digit is typed in the Web page, it is displayed as a four-digit binary number on the board's LEDs when submitted via the Submit button.

- Image Hosting

  The Web server is capable of serving images in .gif and .jpg formats stored in the memory file system.

- Push Buttons

  Press the board's directional push buttons and the binary value will be displayed on the Web page when the Web page is reloaded.

- Host Adobe Acrobat PDF Files

  The Web server can also serve PDF files stored within the memory file system.

- Custom Commands

  The Web server reference design implements several commands, accessible via the .xwscmd file extension. These commands allow you to view the push button status, change the LED values, etc.

Figure 2: **Web Page to Control Web Server Operations**

Opening the Web Server Design

To open the Web server project in EDK, follow these steps:

1. Unzip the included design files.

   The design files are the EDK project files describing the Web server.

2. Open Xilinx Platform Studio (XPS) (**Start** → **Programs** → **Xilinx Embedded Development Kit** → **Xilinx Platform Studio**).
3. In XPS, select **File** → **Open Project**. The Open Project dialog box appears.
4. Browse to the system.xmp file in the ML403/PowerPC directory, and then open the system.xmp file in XPS.

Generating the Netlist and Implementing the Design

To generate the system netlist and implement the hardware design:

1. Generate the netlist by selecting **Tools** → **Generate Netlist** in XPS.

   Observe the progress of the operation in the XPS transcript window.

   The evaluation license for the 10/100 Ethernet MAC core is used to generate the netlist for that core.

2. Implement the design by selecting **Tools** → **Generate Bitstream** in XPS.

   Observe the progress of the operation in the XPS transcript window.

   When XPS implements the system, it accesses a UCF constraints file for the ML403 board. The UCF file is located in the supplied /data directory. XPS also uses the OPT option file included in the /etc directory.

Viewing the Libraries Used in the Design

EDK contains software library support for networking and memory file systems. The Web server design running on the PowerPC processor uses the lwIP TCP/IP stack, the Xilinx MicroKernel (XMK) operating system, and the XilMFS memory file system library.

To view the library settings for the Web server design:

1. In the System tab of the XPS project view window, select **Software** → **Software Platform Settings**.
2. In the **Software Platform** tab of the Software Platform Settings dialog box, observe the **Libraries** table at the bottom left corner of the dialog box (see Figure 3).

   The table indicates that the lwIP and XilMFS libraries are used in the design. Also note that the Xilinx MicroKernel operating system is selected.

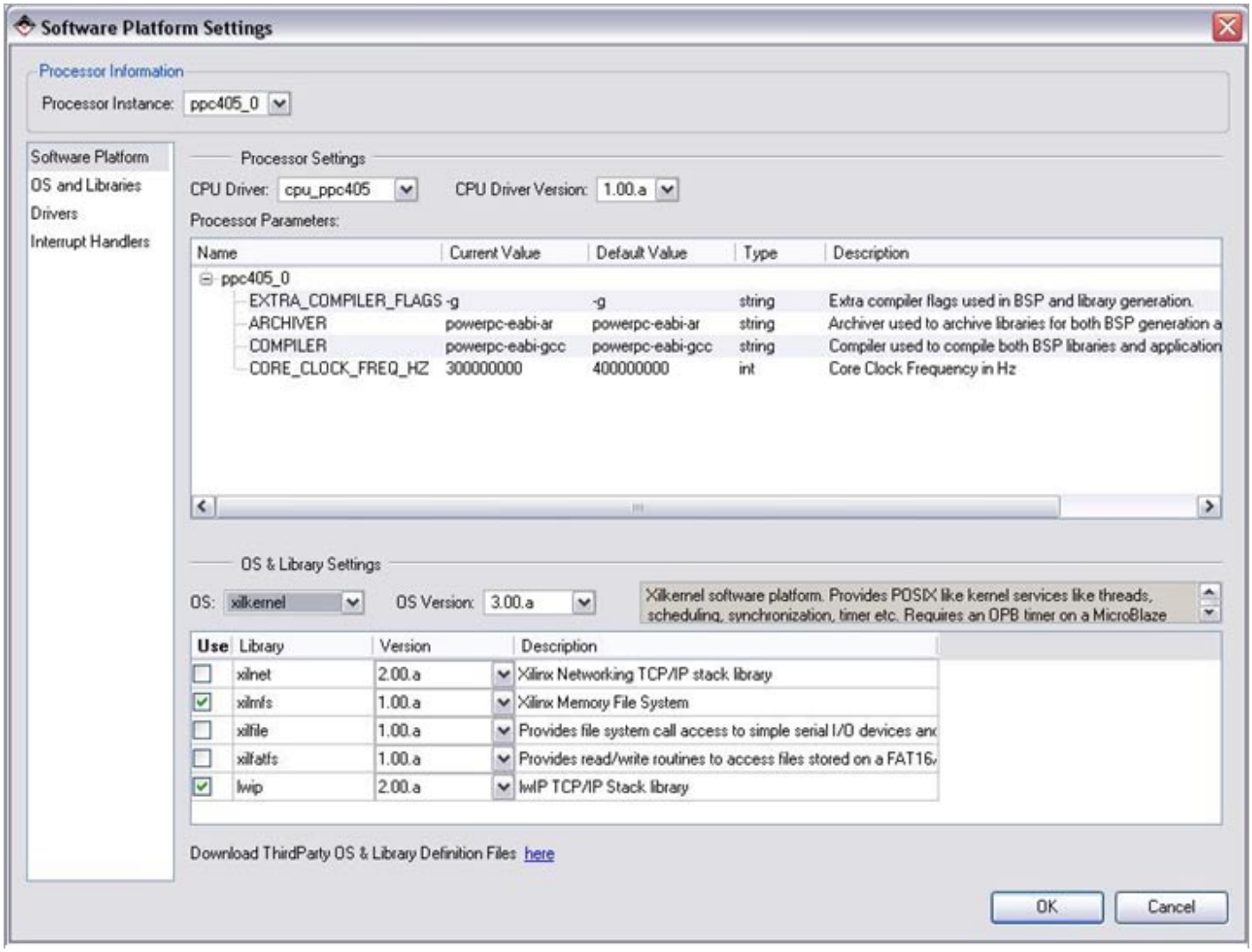

Figure 3: **Libraries Table in Software Platform Settings Dialog Box**

Configuring the Web Server and Compiling the Web Server Code

The Web Server reference design requires that a memory file system be initialized for download into the ML403 SRAM before the design can be executed. The MFS image must be generated before the Web Server is downloaded.

To generate the MFS image:

1. Open a Cygwin shell from **Start** → **Programs** → **Xilinx Platform Studio** → **Accessories** → **Launch EDK Shell**.
2. Change directory to the project's /WebPage directory with the cd command.
3. Remove any pre-existing MFS images in the project's /WebServer directory as follows:

   ```
   rm ../WebServer/*.mfs
   ```

4. Generate the MFS image as follows:

   ```
   mfsgen -cvbfs ../WebServer/image.mfs 700 404.html index.html logoV2005.gif xapp434.pdf
   ```

   The command line options and syntax for the "mfsgen" command are listed in the *OS and Libraries Document Collection* document, in the EDK documentation directory.

5. Exit the EDK shell with the Exit command.
6. In XPS, select **Software** → **Build All User Applications** to compile the Web server design.

Downloading the Web Server Code

Once the Web server code is compiled, the download program must be updated and downloaded to the FPGA.

To download the code to the FPGA, follow these steps:

1. In XPS, select **Device Configuration** → **Update Bitstream**.

   In the XPS transcript window, observe that the bitstream is updated by the iMPACT (ISE device configuration) tool.

   Note: The iMPACT GUI cannot be open when the **Update Bitstream** command runs.
2. Connect the JTAG Parallel 4 cable or Platform USB cable from the PC to the ML403.
3. In XPS, select **Device Configuration** → **Download Bitstream**.

   The bitstream is downloaded to the development board by the iMPACT tool. When the FPGA device is configured, the DONE light is illuminated on the ML403.

Configuring the Web Client and Running the Web Server Demo

1. Unplug any Ethernet cable connected to the host PC and connect the crossover Ethernet cable to the PC and to the ML403 Ethernet port.

   The JTAG Parallel 4 or Platform USB cable must also remain connected from the PC to the ML403.
2. Modify the host PC's IP address so it is in the same subnet as the Web server. To change the PC's IP address, follow these steps:
   a. Select **Start** → **Settings** → **Control Panel** on the Windows desktop.
   b. Double-Click **Network and Internet Connections**.
   c. Right-click the applicable LAN connection, then select **Properties**.
   d. Select **Internet Protocol** and click **Properties**.

   Note: When the PC's IP address is changed in the following steps, note the original property settings so the properties can be changed back after performing the demo.

   e. In the Internet Protocol Properties dialog box, select **Use the following IP Address**.
   f. In the **IP address** box, enter a unique IP address in the same subnet as the one you wish to use for the Web server. For example, if the IP address you want to use for the Web server is 1.2.3.4, the IP address of **`1.2.3.9`** can be entered in the **IP Address** box.
   g. Click **OK** on the Internet Protocol Properties dialog box.
   h. If a message indicates that a subnet mask is missing, Select **OK**. Select **OK** again and again.
3. In XPS, select **Debug** → **Launch XMD** to download the MFS image and the Web server application code to the MicroBlaze processor.

   Note: XMD (Xilinx Microprocessor Debugger) is the EDK debug engine for embedded systems. It includes a TCL environment that allows you to create fully customized debug tools. After launching XMD, it will source xmd.ini if the file is present in the EDK project directory. The xmd.ini file contains a list of TCL commands to run each time XMD runs.

4. From XMD, change directory to the project's /WebServer directory:

   ```
   cd WebServer
   ```

5. Download the MFS image:

   ```
   dow -data image.mfs 0x06000000
   ```

6. Download the Web server design's executable code:

   ```
   dow executable.elf
   ```

7. Run the application:

   ```
   con
   ```

8. Open an HTML browser and point to the URL http://x.x.x.x, where x.x.x.x is the IP address you specified for the Web server.

   Note: If the browser uses a proxy to access the Internet, disable the proxy setting and enable a direct connection to the Internet.

9. The Web server demo page should appear in the browser (see Figure 2). Follow the instructions to read the directional push button values and write to the LEDs on the development board.

Note: XMD (Xilinx Microprocessor Debugger) is the EDK debug engine for embedded systems. It includes a TCL environment which allows you to create fully customized debug tools. After launching XMD, it will source xmd.ini if the file is present in the EDK project directory. The xmd.ini file contains a list of TCL commands to run each time XMD runs.

Device Utilization and Performance

Table 2 provides device utilization and performance metrics.

Table 2: **Device Utilization and Performance Metrics**

Parameters	Specification/Details	
Maximum Frequency (by speed grade)	XC4VFX12-10	100 MHZ
	XC4VFX12-11	110 MHZ
	XC4VFX12-12	115 MHZ
Device Utilization	Slices	4383
	GLCK Buffers	5
	RAMB16 (Block RAM)	12

Note: Due to design considerations, although this reference design will meet timing requirements at higher frequencies, it must be operated at 100 MHz.

Reference Design

The PowerPC Web server design files can be downloaded from:

www.xilinx.com/bvdocs/appnotes/xapp434.zip

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/04	1.0	Initial Xilinx release in Application Note template.
11/3/04	1.1	Revised for EDK 6.3i release.
03/08/06	2.0	Reference design re-written; updated for EDK 8.1i release.
05/01/06	2.1	Added device utilization and performance metrics.
10/13/06	2.2	Updated software requirements to EDK 8.2i or later and ISE 8.2i Service Pack 1 (SP1) or later. Additional minor edits.