XAPP656 (v1.0) November 5, 2004

Using the Virtex-II Pro RocketIO MGT for Frequency Multiplication

Summary

The Virtex-II Pro™ RocketIO™ multi-gigabit transceiver (MGT) is extremely useful to the system designer in its usual role as a high-speed serial communications device. Many designs, however, will not use every available MGT in the package. An unused RocketIO MGT can be used as a frequency synthesizer, generating a low-jitter clock for use either in the FPGA or in the rest of the system.

50/50 Clock Implementation

The RocketIO transceiver is placed into a mode where it accepts 20-bit parallel data at a frequency of F_{IN} MHz. This data is then transmitted at a bit rate of (20 x F_{IN}) Mb/s. If the data pattern is `10101010101010101010`, for example, then the transmitted bitstream will actually look like—and, more importantly, can be used as—a clock of frequency (10 x F_{IN}) MHz with a duty cycle of 50/50. If the bitstream is set to `11111000001111100000`, then the resulting clock will be (2.5 x F_{IN}) MHz. The clock output from the RocketIO transceiver is Current Mode Logic (CML), but can be AC-coupled back into a Low Voltage Differential (LVDS) clock input, either on the Virtex-II Pro FPGA or a third-party device.

As the number of sequential ones and zeros alternately fed to the RocketIO transceiver increases, the frequency-multiplier term (20/2*n*) in the equation below drops toward 1.0, which value is reached when $n = 10$ (ten ones followed by ten zeros fed to the MGT). Continuing from this point ($n > 10$), the frequency multiplier value drops *below* 1.0. For example, a multiplier of 0.5 is achieved by feeding the RocketIO transceiver with twenty zeros, followed by twenty ones. This sequencing is easily achieved using either a constant or a very simple process to generate the data fed to the MGT's transmitter.

The output frequency is given by the formula

$$F_{OUT} = F_{IN} \times \frac{20}{2n}$$

where *n* is the number of consecutive ones and zeros fed to the RocketIO transmitter.

The input clock can be in the range of 40 MHz to 156 MHz. An example that shows a multiplication by 1.25 is shown in Figure 1.

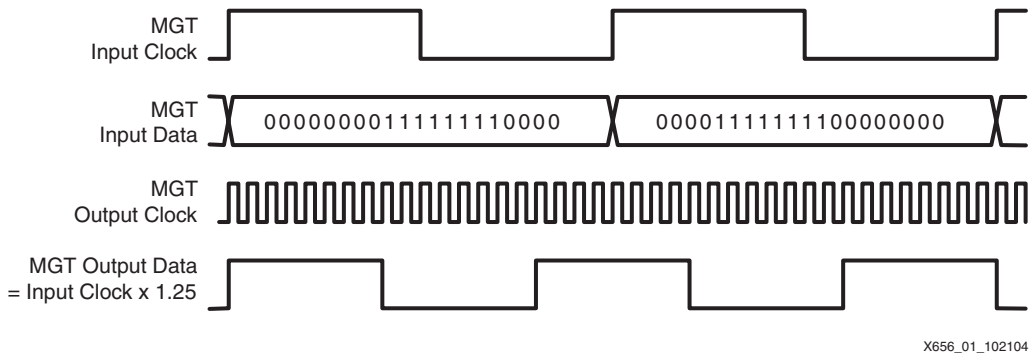

Figure 1: **Timing Diagram Example of Multiplication by 1.25**

A selection of useful values is shown in Table 1.

Table 1: **Non-exhaustive List of Possible Frequency Multiplications for 50/50 Output**

Number of Ones and Zeros Alternately Fed to the MGT	Frequency Multiplier
1	10
2	5
4	2.5
5	2
5	1.6666
8	1.25
10	1
15	0.6666
16	0.625
20	0.5

Non-50/50 Clock Implementation

If the design can tolerate a duty cycle that is not 50/50, then another slightly modified technique can be used. The run length of ones and zeros is given when the formula is solved for *n,* as

$$n = \frac{20}{2 \times FrequencyRatio}$$

where *FrequencyRatio* is the output clock frequency divided by the input clock frequency. Therefore, if a frequency ratio of 4:1 is required (output clock = 4 x the input clock), *n* would be 2.5. It is obviously impossible to transmit two and one-half zeros and two and one-half ones, but this can be emulated by sending either two ones and three zeros, or two zeros and three ones. This will result in the correct frequency, albeit with a duty cycle that is not 50%. Because the output from the RocketIO transceiver is AC-coupled to the LVDS input, the duty cycle will tend to be cleaned up somewhat, but this should not be relied upon.

The input clock can be in the range of 40 MHz to 156 MHz. A detailed timing example for multiplication by 4 is shown in Figure 2.

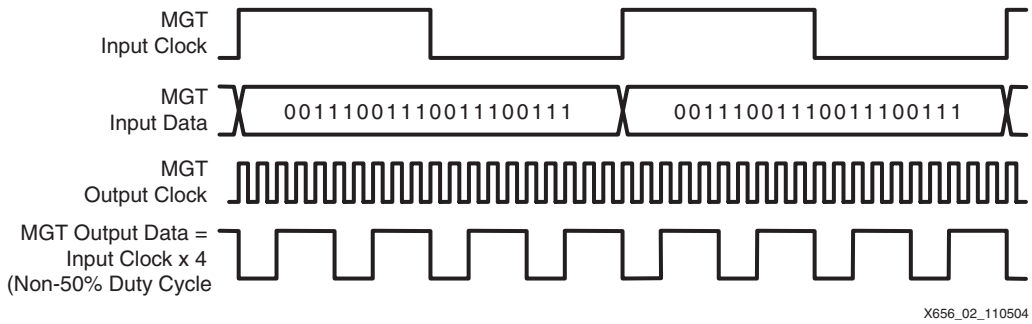

Figure 2: **Example Timing Diagram for Multiplication by 4**

A selection of useful values is shown in Table 2.

Table 2: **Non-exhaustive List of Possible Frequency Multiplications for Non-50/50 Clock**

Number of Ones and Zeros Alternately Fed to the MGT	Zeros	Ones	Frequency Multiplier
2.5	3	2	4
12.5	13	12	0.8

Design Files

Design files for the techniques described in this application note are available in both VHDL and Verilog from the Xilinx web site.

http://www.xilinx.com/bvdocs/appnotes/xapp656.zip

Conclusion

The unused RocketIO transceiver in a Virtex-II Pro device can be used as a general-purpose frequency multiplier.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/05/04	1.0	Initial Xilinx release.