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Synthesizable CIO DDR RLDRAM II Controller for Virtex-4 FPGAs

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Summary

This application note describes how to use a Virtex®-4 device to interface to Common I/O (CIO) Double Data Rate (DDR) Reduced Latency DRAM (RLDRAM II) devices. The reference design targets two CIO DDR RLDRAM II devices at a clock rate of 200/230/250 MHz with data transfers at 400/460/500 Mb/s per pin.

Introduction

This application note describes a CIO DDR RLDRAM II controller design implemented in a Virtex-4 device. The first section describes RLDRAM II functionality while the following sections describe implementation and timing analysis details.

RLDRAM II Devices

The second generation of RLDRAM is a high-performance memory, combining the performance-critical features that networking and cache applications need, such as high density (up to 288 Mb), high bandwidth (up to 28.8 Gb/s), and fast SRAM-like random access.

RLDRAM II is based on a new internal eight-bank architecture that minimizes data access time. This memory provides minimized latency and reduced row cycle times ideal for applications such as networking, graphics, and cache that require critical response times and very fast random access.

RLDRAM II operates at a clock frequency of up to 400 MHz and uses a DDR interface. The DDR interface transfers two 36-bit, 18-bit, or 9-bit wide data words per clock cycle. Output data is referenced to the free-running output data clock (QK). Commands, addresses, and control signals are registered at every positive edge of the differential input clock (CK), while input data is registered at both positive and negative edges of the input data clock (DK).

The RLDRAM II architecture offers separate I/O (SIO) and CIO options. SIO devices have separate read and write ports to eliminate bus turnaround cycles and contention. They are also optimized for near-term read and write balance and full bus utilization.

CIO devices have a shared read/write port that requires one additional cycle to turn the bus around. The RLDRAM II CIO architecture is optimized for data streaming, where the near-term bus operation is either 100% read or 100% write, independent of the long-term balance.

The CIO RLDRAM II device has a shared data read/write port, resulting in a bidirectional data bus. During read commands, the data is output from the device and is referenced to both edges of the QK clocks. During write commands, the data is input to the device and is sampled at both edges of the DK clocks.

Read and write access to RLDRAM II is burst-oriented. The burst length is programmable at 2, 4, or 8 through the Mode register. RLDRAM II I/Os use the 1.5V or 1.8V HSTL I/O standard.

Designers should choose an I/O version that provides an optimal compromise between performance and utilization, shown in [Ref 1].

Clocking

The RLDRAM II device requires a differential input, master-clock pair, CK and $\overline{CK}$. When CK and $\overline{CK}$ are 180° out of phase, they provide the best system margins. The RLDRAM II device feeds an internal DLL to create the differential output, data-clock pair, QK and $\overline{QK}$. Only the rising edge of CK is used for address and control latching.

A differential input, data-clock pair, DK and $\overline{DK}$, is another requirement. Both rising edges are used to latch data to the device. When DK and $\overline{DK}$ are 180° out of phase, they provide the best margin on write data. For the x36 configuration, two differential input, data-clock pairs are available, with DQ0 through DQ17 referenced to DK0 and $\overline{DK0}$, and DQ18 through DQ35 referenced to DK1 and $\overline{DK1}$. For the x18 and x9 configurations, all DQ are referenced to DK and $\overline{DK}$ as a single-differential input, data-clock pair.

The last set of clocks is the differential-output, data-clock pair, QK and $\overline{QK}$. During a read from the device, QK and $\overline{QK}$ are transmitted by the RLDRAM II and edge-aligned with the output data. In the x36 configuration, QK0 and $\overline{QK0}$ are aligned with the least significant data bits (DQ0 through DQ17) while QK1 and $\overline{QK1}$ are aligned with the most significant data bits (DQ18 through DQ35). In the x18 configuration, QK0 and $\overline{QK0}$ are aligned with the least significant data bits (DQ0 through DQ8) while QK1 and $\overline{QK1}$ are aligned with the most significant data bits (DQ9 through DQ17). The x9 configuration only uses QK0 and $\overline{QK0}$ aligned with the data bits (DQ0 through DQ8).

Mode Register

The Mode register stores data controlling the operating modes of the memory. It programs the RLDRAM II configuration, burst length, test mode, and I/O options. During a Mode register set command, the address inputs A[17:0] are sampled and stored in the Mode register shown in Table 1. The Mode register can be configured at any time during device operation.

Table 1: **Mode Register Fields**

Address Bits	Field Name	Description
A[17:10]	Reserved	Must be set to zero
A9	On-Die Termination	0 - Disabled 1 - Enabled
A8	Impedance Matching	0 - Internal 50Ω 1 - External
A7	DLL Reset	0 - DLL reset 1 - DLL enabled
A6	Unused	-
A5	Address Mux	0 - Non-multiplexed 1 - Multiplexed
A[4:3]	Burst Length (BL)	00 - 2 01 - 4 10 - 8 11 - Not valid
A[2:0]	Configuration	000 - 1 (BL of 8 not available) 001 - 1 (BL of 8 not available) 010 - 2 011 - 3 100 to 111 - Reserved

Configuration Table

Table 2 shows the different RLDRAM II configurations that can be programmed into the Mode register for different operating frequencies. The read and write latency (t_{RL} and t_{WL}) values and the row cycle times (t_{RC}) are shown in clock cycles as well as in nanoseconds (ns).

Table 2: **RLDRAM II Configurations**

Frequency	Symbol	Configuration			Unit
		1	2	3	
	t_{RC}	4	6	8	cycles
	t_{RL}	4	6	8	cycles
	t_{WL}	5	7	9	cycles
400 MHz	t_{RC}	-	-	20.0	ns
	t_{RL}	-	-	20.0	ns
	t_{WL}	-	-	22.5	ns
300 MHz	t_{RC}	-	20.0	26.7	ns
	t_{RL}	-	20.0	26.7	ns
	t_{WL}	-	23.3	30.0	ns
200 MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	20.0	30.0	40.0	ns
	t_{WL}	25.0	35.0	45.0	ns

RLDRAM II Burst Length (BL) and Configuration Matrix

Table 3 shows the RLDRAM II burst lengths and configuration matrix.

Table 3: **RLDRAM II Burst Length and Configuration Matrix**

Burst Length	Configuration		
	200 MHz (-5)	300 MHz (-3.3)	400 MHz (-2.5)
BL = 2	Config=1 Config=2 Config=3	$<t_{RC}$ Config=2 Config=3	$<t_{RC}$ $<t_{RC}$ Config=3
BL = 4	Config=1 Config=2 Config=3	$<t_{RC}$ Config=2 Config=3	$<t_{RC}$ $<t_{RC}$ Config=3
BL = 8	N/A Config=2 Config=3	N/A Config=2 Config=3	N/A $<t_{RC}$ Config=3

Notes:

1. N/A - Not available, BL=8 is not available for Config=1 (Micron)
2. $<t_{RC}$ - violates t_{RC}, configuration not allowed (Micron)
3. BL=8 is not supported by the controller
4. The controller focuses on BL=2 and BL=4 (all three configurations)

Address Bus

Table 4 shows the address bus usage for different burst lengths and configurations.

Table 4: **Address Bus Usage**

Burst Length	Configuration		
	x36	x18	x9
BL = 2	[18:0]	[19:0]	[20:0]
BL = 4	[17:0]	[18:0]	[19:0]
BL = 8	N/A	[17:0]	[18:0]

Commands

Table 5 describes RLDRAM II commands used with the RLDRAM II device.

Table 5: **RLDRAM II Commands**

Command	Description
DESEL/NOP	The NOP command performs a no operation to the RLDRAM II to deselect the device.
MRS	Sets the Mode register via the address inputs A[17:0]. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	Initiates a burst read access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank.
WRITE	Initiates a burst write access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank. The input data appearing on the DQ bus is written to the memory array subject to the data mask (DM) input logic level appearing with the data. If the DM signal is Low, the data is written to memory. If the DM signal is High, the data inputs are ignored. This part of the data word is not written.
AREF	Refreshes the memory content of a bank during normal operation of the RLDRAM II. The command must be issued each time a refresh is required. The value on the BA[2:0] inputs selects the bank. The refresh address is generated by an internal refresh controller and makes each address bit unused during the AREF command. The RLDRAM II requires 64K cycles at an average periodic interval of 0.49 µs (maximum). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM II at periodic intervals of 3.9 µs.

Bank Usage

The Mode register controls both the burst length and the RLDRAM II configuration. The selected t_{RC} defines how frequently any one bank can be accessed, while the burst length determines how often a new address is required.

Banks can be accessed in any order at any time as long as t_{RC} is met before revisiting a bank. One method to optimize the use of the eight-bank architecture offered by the RLDRAM II is to read data from or write data to the device using a *round-robin* approach.

Correspondence of RL and WL Times

RLDRAM II imposes WL=RL+1 every time a read-to-write cycle is performed, making the data pipelining both correct and efficient. For a write-to-read cycle, however, a *dead cycle* must be added to the write-to-read cycle or the write and read data appears at the same time. This causes contention or data loss, and the controller must handle the contention.

CIO DDR RLDRAM II Controller

Implementation Details

Figure 1 shows a top-level block diagram of the CIO DDR RLDRAM II controller.

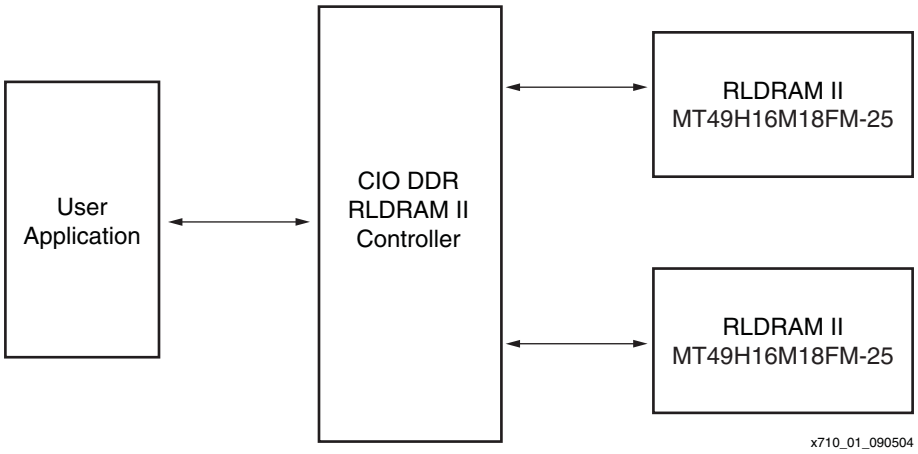

Figure 1: **CIO DDR RLDRAM II Controller (Top Level)**

Design Features

The key features of the CIO DDR RLDRAM II Controller design are:

- Micron compliant (to the specification shown in [Ref 1]).
- Data interface width of 36 bits using two MT49H16M18FM-25 devices from Micron, supporting two 16M x 18 bits devices.
- Common I/O mode for the bidirectional data bus.
- ChipSync™ technology is used by the Virtex-4 FPGA physical layer
- ChipSync technology detects the edges of QK to determine their phase relationship with the internal FPGA clock.
- Delayed read data center-aligned to the rising edge of the internal FPGA clock in the data window.
- Performance is 200 MHz (400 Mb/s) for XC4VLX25 -10 speed grade, 230 MHz (460 Mb/s) for XC4VLX25 -11 speed grade, and 250 MHz (500 Mb/s) for XC4VLX25 -12 speed grade.
- FIFO-based user interface.
- Burst lengths of 2 and 4.

  Note: The current design does not support contiguous 2-word bursts.
- Pre-set Mode register, where Config=2 and BL=4.
- Non-multiplexed address bus.
- Automatic and manual refresh.

Block Diagram Description

This section includes a detailed block diagram of the CIO DDR RLDRAM II controller (Figure 2, page 6) and descriptions of the major blocks.

User Interface

The backend interface of the controller is a FIFO-based implementation. Three FIFOs are used: an address FIFO, a write-data FIFO, and a read-data FIFO. The user interface also provides a configuration register and some other control signals.

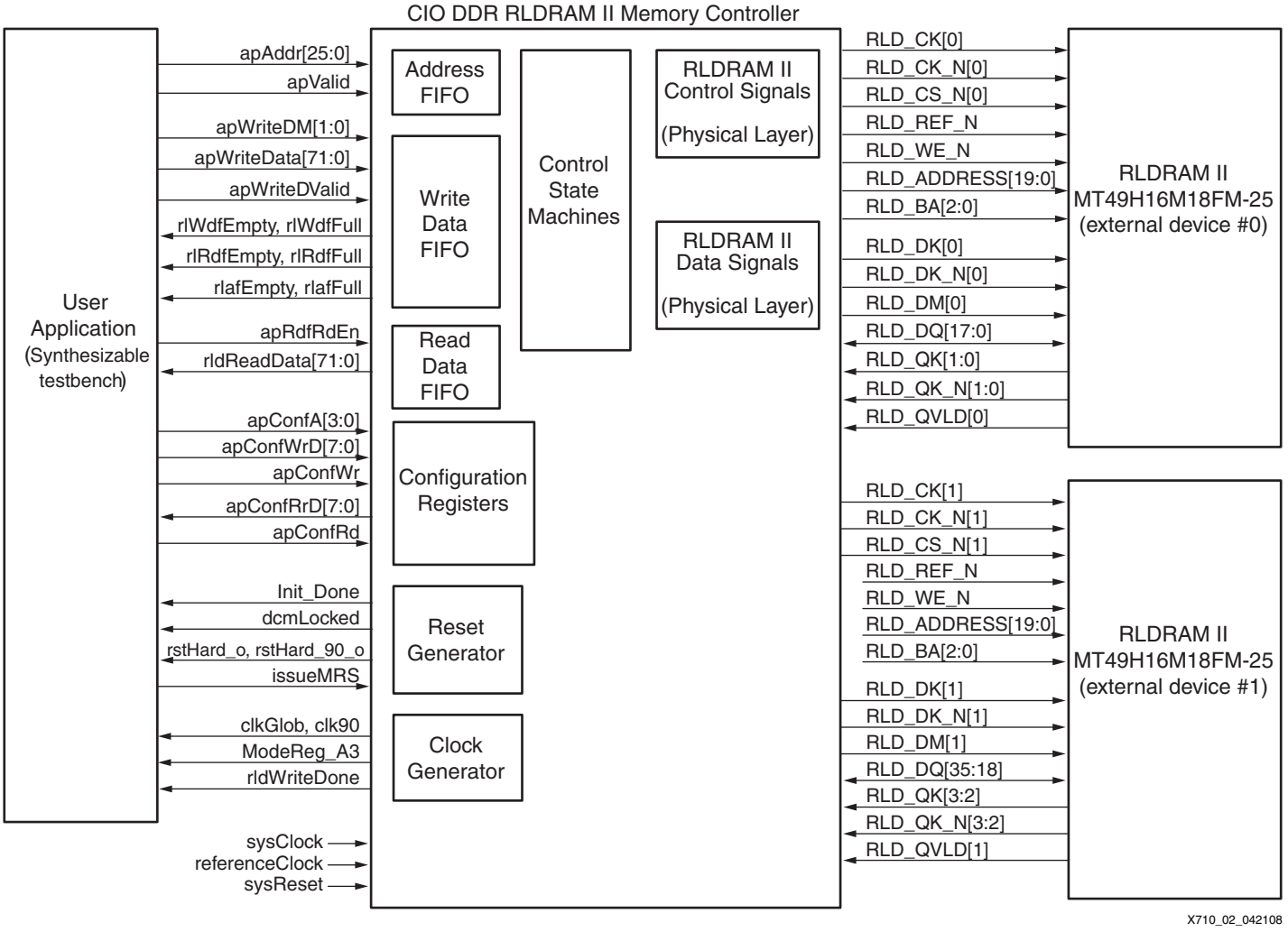

Figure 2: **CIO DDR RLDRAM II Controller (Detailed)**

Address FIFO

The address FIFO serves as the buffer for the backend interface to store addresses corresponding to the read and write data as well as the user-controlled refreshes. All reads, writes, and user refreshes are scheduled in this FIFO. This synchronous FIFO is 26 bits wide and 16 words deep. Table 6 defines the configuration of the 26 bits.

Table 6: **Address FIFO Bit Configuration**

Bit Configuration	Description
25	User Refresh
24	Read/$\overline{\text{Write}}$
23	Reserved
[22:3]	Memory Address bits A[19:0]
[2:0]	Memory Bank Address bits BA[2:0]

Write-Data FIFO

The write-data FIFO serves as a buffer for the backend interface to store data that needs to be written into the memory. This synchronous FIFO is 74 bits wide and 15 words deep. For a burst length of 2, each location in the write-data FIFO constitutes the required data. For a burst

length of 4, two locations in the write-data FIFO constitute the required data. Table 7 defines the configuration of the 74 bits.

Table 7: **Write-Data FIFO Bit Configuration**

Bit Configuration	Description
[73:72]	Write-Data Mask
[71:0]	Write Data

Read-Data FIFO

The read-data FIFO serves as a buffer to store data the controller has read from the memory. Then it is read by the controller to compare with the expected data. This synchronous FIFO is 4 x 18 bits wide and 16 words deep. For a burst length of 2, each location in the read-data FIFO constitutes the data read from the memory. For a burst length of 4, two locations in the read-data FIFO constitute the data read from the memory. Table 8 defines the configuration of the 72 bits.

Table 8: **Read-Data FIFO Bit Configuration**

Bit Configuration	Description
[71:0]	Read Data

Configuration Registers

The configuration registers block provides an interface for the application to read from and write to the configuration registers. For example, auto refresh is ON by default, making the controller send AREF commands to the memories at the required intervals. The user can turn auto refresh OFF through the confCycRef bit. This is an internal configuration bit. The user can also update/read through the configuration read/write access port. In this case, the user is responsible for issuing USER REFRESH commands.

The burst length can be changed at either compile time in the code, or it can be reprogrammed during run time through the configuration register confMReg[4:3]. These bits are defined in Table 1.

Clock Generator

This block generates all the required clocks for the controller by using a DCM; the output for the two clock phases is 0 and 90. The 200-MHz reference clock buffer is included in this module; this clock goes to all IDELAYCTRL primitives.

Reset Generator

This block generates different reset signals. It also performs the initialization and configuration (MRS) of the RLDRAM II.

Control State Machines

This block contains a state machine that controls NOP, READ, WRITE, AUTO REFRESH, and USER REFRESH operations to and from the memories.

RLDRAM II Control Signals Physical Layer

This block contains the pads that interface with the RLDRAM II control and address signals. It is a separate module from the data signals memory interface.

RLDRAM II Data Signals Physical Layer

This block contains the pads that interface with the RLDRAM II data signals. A calibration circuit samples the QK/$\overline{\text{QK}}$ signals using the Virtex-4 FPGA ChipSync feature. The FPGA clock

samples both the data clock, for calibration, and the data itself to capture it in the same clock domain. Refer to XAPP701 [Ref 2] for more details.

Pin Descriptions

Table 9 provides pin descriptions for the CIO DDR RLDRAM II controller.

Table 9: **CIO DDR RLDRAM II Controller Pin Descriptions**

Pin Name	Pin Direction	Description
Interface to User Application		
apAddr[25:0]	In	Address FIFO data input, synchronous with clkGlob (for example, the FPGA Clock)
apConfA[3:0]	In	Configuration registers address bus, synchronous with clkGlob
apConfRd	In	Configuration registers read enable, synchronous with clkGlob
apConfRdD[7:0]	Out	Configuration registers read data, synchronous with clkGlob
ApConfWr	In	Configuration registers write data valid, synchronous with clkGlob
apConfWrD[7:0]	In	Configuration registers write data, synchronous with clkGlob
apRdfRdEn	In	Read-Data FIFO read enable, synchronous with clk90
apValid	In	Address FIFO data valid input, synchronous with clkGlob
apWriteData[71:0]	In	Write-Data FIFO data input, synchronous with clkGlob
apWriteDM[1:0]	In	Write-Data FIFO DM input, synchronous with clkGlob
apWriteDValid	In	Write-Data FIFO data valid input, synchronous with clkGlob
clk90	Out	System-clock output from DCM
clkGlob	Out	System-clock output from DCM (main FPGA Clock)
dcmLocked	Out	Indicates DCM is locked and synchronous with clkGlob
Init_Done	Out	Indicates memory initialization is complete and synchronous with clkGlob
issueMRS	In	A pulse on this input causes the controller to program Mode register into the memory, synchronous with clkGlob (at power-up, MRS is done as part of the initialization).
ModeReg_A3	Out	Mode register A3 bit, can be used to differentiate between burst lengths of 2 and 4, synchronous with clkGlob
rlafEmpty	Out	Address FIFO empty flag, synchronous with clkGlob
rlafFull	Out	Address FIFO full flag, synchronous with clkGlob
rldReadData[71:0]	Out	Read-Data FIFO data output, synchronous
rldWriteDone	Out	Indicates that a write to memory is complete, synchronous with clkGlob
rlRdfEmpty	Out	Read-Data FIFO empty flag, synchronous
rlRdfFull	Out	Read-Data FIFO full flag, synchronous
rlWdfEmpty	Out	Write-Data FIFO empty flag, synchronous with clkGlob
rlWdfFull	Out	Write-Data FIFO full flag, synchronous with clkGlob
rstHard_90_o	Out	Active-High reset until DCM is locked, synchronous with clk90
rstHard_o	Out	Active-High reset until DCM is locked, synchronous with clkGlob
referenceCLK	In	200-MHz reference clock for IDELAYCTRL (taps)
sysClk	In	System clock
sysReset	In	Active-High system reset

Table 9: **CIO DDR RLDRAM II Controller Pin Descriptions *(Continued)***

Pin Name	Pin Direction	Description
Interface to Two CIO DDR RLDRAM II Devices		
RLD_DQ[35:0]	In/Out	Data input/outputs. During read commands, the data is sampled at both edges of QK. During write commands, the data is referenced to both edges of DK.
RLD_ADDRESS[19:0]	Out	Row and column addresses for read and write operations. During a MODE REGISTER SET, the address inputs define the register settings.
RLD_BA[2:0]	Out	Bank addresses select the internal bank to apply a command.
RLD_CK[1:0] RLD_CK_N[1:0]	Out	Master differential clocks for addresses and commands.
RLD_CS_N[1:0]	Out	Chip Select command
RLD_DK[1:0] RLD_DK_N[1:0]	Out	Differential write-data clocks
RLD_DM[1:0]	Out	DM signals for write data
RLD_REF_N	Out	Refresh command
RLD_WE_N	Out	Write Enable command
RLD_QK[3:0] RLD_QK_N[3:0]	In	Differential read-data clocks transmitted by the RLDRAM II devices and edge-aligned with read data.
RLD_QVLD[1:0]	In	Data valid signals transmitted by the RLDRAM II devices. Indicate valid read data.

Memory Initialization

The RLDRAM II device must be powered up and initialized in a predefined manner. The initialization sequence is handled by the controller:

1. After all power supply and reference voltages are stable and the master clock (RLD_CK and RLD_CK_N) is stable, the RLDRAM II requires a 200 µs (minimum) delay prior to applying an executable command.
2. After the 200 µs (minimum) delay has passed, three MRS commands are issued: two dummies plus one valid MRS.
3. Six clock cycles (t_{MRSC}) after the valid MRS, eight AUTO REFRESH commands are issued, one on each bank and separated by 2,048 cycles.
4. After six clock cycles (t_{RC}) for Configuration 2, initialization is complete. The device is ready for normal operation as indicated by the Init_Done outputs to the application.

Clocking Methodology and Read/Write Datapaths

The Virtex-4 FPGA clocking methodology and read/write datapath integrated is integrated in the IOB delay functionality (a ChipSync feature), for example, IDELAY/IDELAYCTRL. Read data is captured directly in the FPGA global clock domain. Write data and clock are transmitted using quadrature phase-shifted outputs of the DCM.

Implementation Details

The RLDRAM II reference design takes advantage of the newest features of the Virtex-4 family: improvements in I/O, clocking resources, and storage elements. All of these features contribute to the high performance and ease-of-use for this design. The following sections describe the design implementation in more detail.

User Interface

The user interface module uses three FIFOs to store the address and data values for Read/Write commands. One FIFO holds the commands (read, write, and/or user refresh) and

the Read/Write addresses. Another FIFO stores the Write data and data mask (used as byte write enable). The third FIFO stores the Read data.

The user sends commands through the user interface with concurrent rising and falling data. The commands and data are transferred by the system clock (single data-rate transfers). This reference design shows an external 36-bit data bus, thus a 72-bit internal data bus is submitted/received to/from the controller's FIFOs.

The user monitors the “rlafFull” FIFO full flag signal before sending new commands. For example, the Write data is built from “apWriteDM[1:0], apWriteData[71:0]” and is written to the controller with the write enable signals named apWriteDValid. This also applies to the read data. A 72-bit “rldReadData” (rising/falling edge read data) is extracted from the Read FIFO.

Reset/Init State Machine

The state diagram for the Reset/Init state machine is shown in Figure 3.

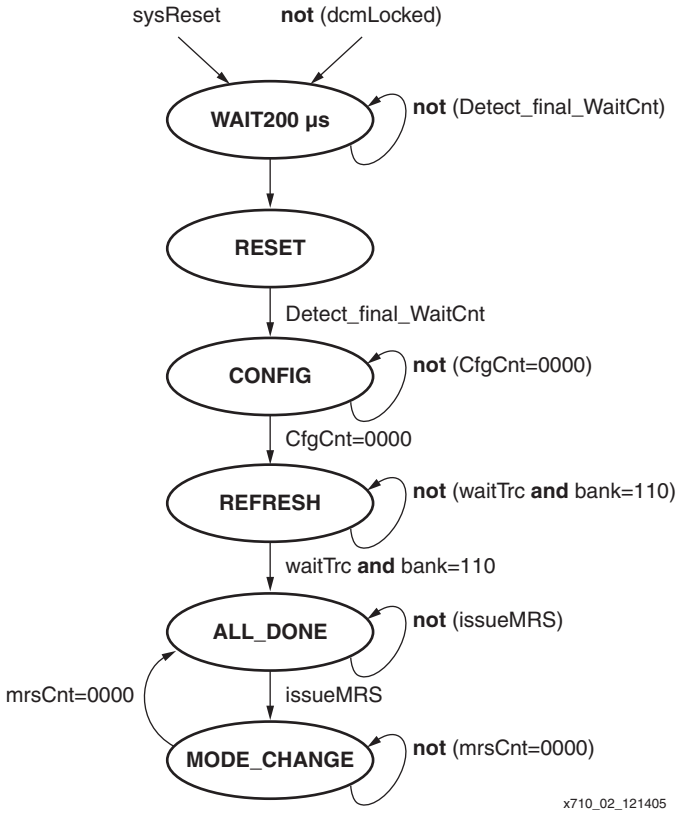

Figure 3: **State Diagram for the Reset/Init Machine**

This state machine is responsible for handling the reset condition, preparing the memory initialization, initiating the calibration process (data capture) and supporting memory mode changes.

Data Calibration State Machine

The state diagram for the data calibration state machine is shown in Figure 4.

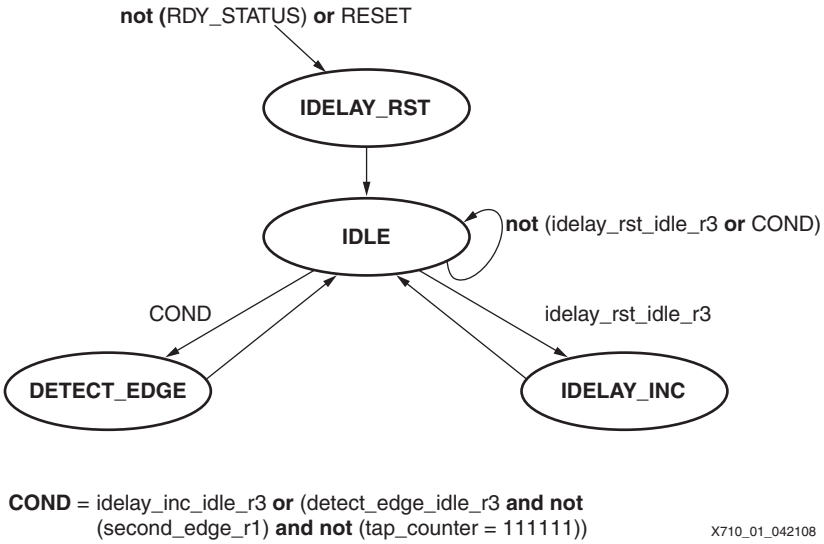

Figure 4: **State Diagram for the Data Calibration State Machine**

Two steps are required to achieve the data calibration.

1. Each read clocks QK/QK_N are captured independently, and the state machine finds the clock edges and measures the clock window to locate the mid-point.
2. The number of taps (counts) is applied to the data words IDELAY based on the mid-point. If the wrong read clock is evaluated and applied, the data is not captured correctly. After each reset, only one calibration is performed.

Continuous calibration helps to compensate for memory and I/O timing variations. The data_tap_inc command resets the IDELAY taps for the data before setting the new calibration value.

Performing a real-time calibration on a design during the recalibration process causes a read-data failure. This can be avoided if the read commands are held or stopped during this process.

I/O Timing Analysis

This section provides a timing analysis of the reference design. The analysis uses an XC4VLX25 FF668 -10 device and an MT49H16M18FM-25 device from Micron for the timing parameters. Figure 5 is a memory-timing model of the Virtex-4 device connection to the RLDRAM II. The parameters in *italics* in Table 10 through Table 15 are taken from the Micron data sheet [Ref 1].

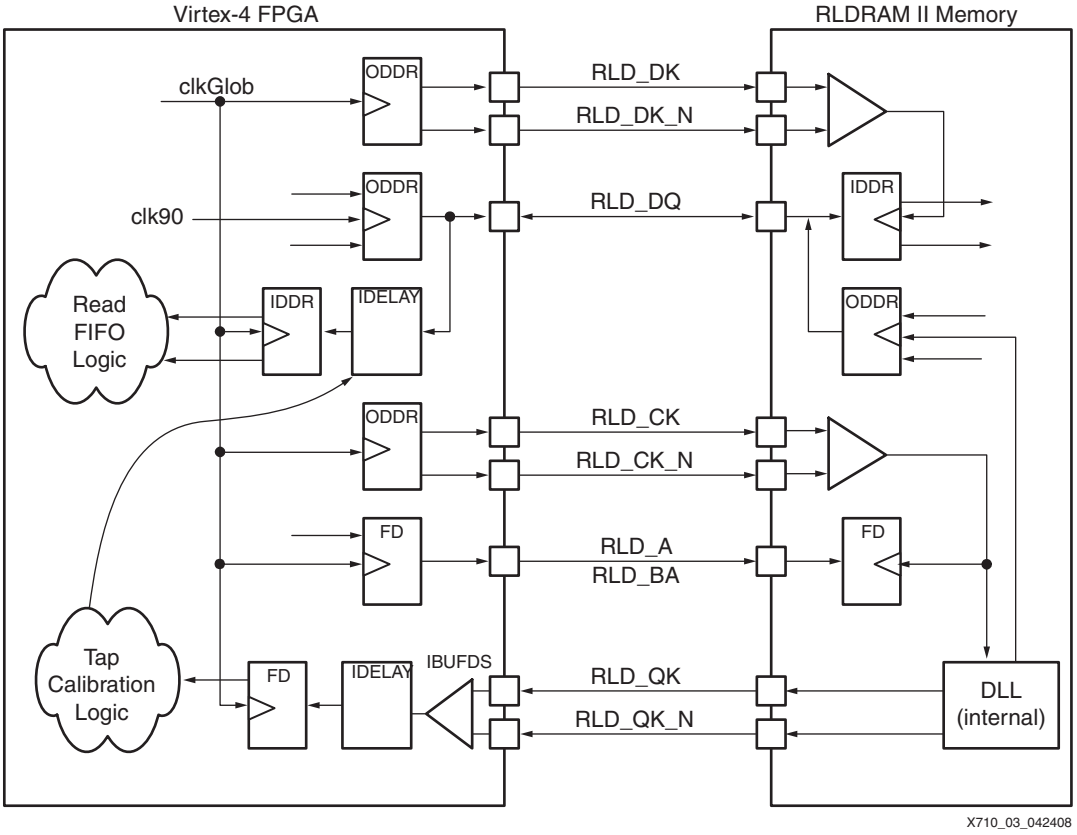

Figure 5: **Virtex-4 FPGA and Memory Timing Model**

Read Timing Analysis

The FPGA clock is transmitted to the memory through CK/CK_N pins; the memory locks on it with a DLL, then uses that internal clock to output data (DQ) and output data clock (QK/QK_N). A small phase error exists between CK/CK_N and QK/QK_N edges (t_{CKQK} = 250 ps). This phase error does not need to be considered because QK/QK_N is used to capture read data, not CK/CK_N. The clock phase jitter of the FPGA is used (T_{DCD_CLK} = 150 ps maximum) to account for duty-cycle distortion and jitter from the FPGA clock.

The worst-case number of IDELAY taps used to center the data to the FPGA clock must be considered because of data dependent jitter added with each tap. The worst-case scenario is to delay the data for three-fourths of a clock cycle, so the jitter associated with the amount of taps needed for this delay is added to the timing analysis [Ref 2]. The board layout skew between QK/QK_N and DQ (around 50 ps) and minimal package skew in the same physical region (around 20 ps assuming board deskew) are also considered.

The valid data output DQ access time for QK/QK_N edges is specified as t_{QKQ} = 400 ps (QK0/QK0_N for lower bytes, and QK1/QK1_N for higher bytes). This parameter cannot be at its maximum and minimum value at the same moment.

The read timing analysis for 200 MHz is shown in Table 10.

Table 10: **Read Timing Analysis at 200 MHz (XC4VLX25-10)**

Parameter	Value (ps)	Description
T_{CLOCK}	5000	Clock period
T_{DATA_PERIOD}	2500	Valid Data Period (DDR mode)
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	100	Global clock tree skew for the smallest/largest clock net delay
T_{DCD_CLK}	150	Global clock tree duty cycle distortion
$T_{PACKAGE\_SKEW}$	20	Package skew for an XC4VLX25 FF668 part/package within the same region(2)
$T_{PCB\_LAYOUT\_SKEW}$	50	Skew between data lines and strobes on the board (167ps/in)
T_{SAMP}	550	Sample window from the Virtex-4 FPGA data sheet [Ref 4]. Includes setup and hold times for an IOB flip-flop, clock jitter, and tap uncertainty(1).
IDELAY Taps (maximum)	50	Worst-case number of taps to delay data 3/4 of the clock period
$T_{IDELAYPAT\_JIT}$	600	Pattern-dependent period jitter in delay chain for random data pattern (10 ± 2 ps per tap)
Memory Uncertainties	400	Worst-case of all the memory parameters (-2.5 device)
Total Uncertainties	-	
Read Window	630	Worst-case window of 630 ps

Notes:

1. This parameter indicates the total sampling error of the Virtex-4 FPGA DDR input registers across voltage, temperature, and process.
2. Package skew in the same physical region or in the same Bank, assuming package trace length information used to deskew the package during board layout.

The read timing analysis for 230 MHz is shown in Table 11.

Table 11: **Read Timing Analysis at 230 MHz (XC4VLX25-11)**

Parameter	Value (ps)	Description
T_{CLOCK}	4347.83	Clock period
T_{DATA_PERIOD}	2173.91	Valid Data Period (DDR mode)
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	100	Global clock tree skew for the smallest/largest clock net delay
T_{DCD_CLK}	150	Global clock tree duty cycle distortion
$T_{PACKAGE\_SKEW}$	20	Package skew for an XC4VLX25 FF668 part/package within the same region(2)
$T_{PCB\_LAYOUT\_SKEW}$	50	Skew between data lines and strobes on the board (167ps/in)
T_{SAMP}	500	Sample window from the Virtex-4 FPGA data sheet [Ref 4]. Includes setup and hold times for an IOB flip-flop, clock jitter, and tap uncertainty(1).
IDELAY Taps (maximum)	44	Worst-case number of taps to delay data 3/4 of the clock period

Table 11: **Read Timing Analysis at 230 MHz (XC4VLX25-11) *(Continued)***

Parameter	Value (ps)	Description
$T_{IDELAYPAT\_JIT}$	528	Pattern-dependent period jitter in delay chain for random data pattern (10 ± 2 ps per tap)
Memory Uncertainties	400	Worst-case of all the memory parameters (-2.5 device)
Total Uncertainties	-	
Read Window	425.91	Worst-case window of 425.91 ps

Notes:

1. This parameter indicates the total sampling error of the Virtex-4 FPGA DDR input registers across voltage, temperature, and process.
2. Package skew in the same physical region or in the same Bank, assuming package trace length information used to deskew the package during board layout.

The direct clocking method is different from classic methods, and is related to source synchronous clocking. The goal is to center the QK/QK_N clocks in the data window, giving an ideal setup and hold time to capture the data.

T_{SAMP} indicates the sampling error at the DDR pins and must be considered to ensure correct read data capture directly using a DCM clock. T_{SAMP} includes the setup and hold times for the DDR flop (in the ILOGIC) along with tap uncertainty. During the calibration process, data edge detection and the metastability condition are both analyzed and considered. DDR flops are used to capture the QK clock and the calibration state machine selects a solid *inside the window* tap delay that represents the clock edges.

When the DDR flops capture the samples, they respect the setup/hold requirements. Otherwise, the sampled data is not constant at those data edges (metastable). Selecting the previous/next tap where the data is *solid* respects the local setup and hold times of the DDR flop.

Write Timing Analysis

The FPGA-clock duty cycle distortion is normally less than 5% (45% – 55%) from the ideal clock duty cycle. The smaller half clock period is used as the basic data window (0.45 of clock cycle). The uncertainty parameters are global clock tree skew (100 ps) between data I/O registers and a phase offset of 140 ps because 90° and 270° clock phases are used for data transmission. A board layout skew between DK/$\overline{DK}$ and DQ (around 20 ps) and package skew in the same physical region (around 10 ps, assuming board deskew) are classified as uncertainties.

Valid data input DQ at the memory has setup and hold time requirements of 250 ps each tied to DK/$\overline{DK}$ edges. The same parameters apply also to the DM.

The timing analysis with all the above parameters is summarized in Table 12.

Table 12: **Write Timing Analysis at 200 MHz (XC4VLX25-10)**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	5000	-	-	Clock period
T_{PHASE}	2500	-	-	Clock phase (DRR mode)
T_{DATA_PERIOD}	2250	-	-	Valid data period (0.45 x T_{CLOCK} for DDR)
T_{JITTER} (maximum)	0	0	0	Same DCM is used to generate Data and Strobe.
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	±100	100	100	Global clock tree skew for the smallest/largest clock net delay
$T_{PACKAGE\_SKEW}$	±10	10	10	Worst-case package skew for an XC4VLX25 FF668 part/package within the same region(1)
$T_{PCB\_LAYOUT\_SKEW}$	± 20	20	20	Skew between data lines on the board (167 ps/in).
$T_{PHASE\_OFFSET\_ERROR}$	± 140	140	140	Offset error between different clocks from the same DCM
Tds	*250*	*250*	*0*	Data and data mask to DK setup time (-2.5 device)
Tdh	*250*	*0*	*250*	Data and data mask to DK hold time (-2.5 device)
Total Uncertainties	-	(left side) 520	(right side) 520	
Write Window	1210	520	1730	Worst-case window of 1210 ps

Notes:

1. Package skew in the same physical region or within the same Bank, assuming package trace length information used to deskew the package during board layout.

Table 13 summarizes the write timing analysis at 230 MHz (XC4VLX25-11).

Table 13: **Write Timing Analysis at 230 MHz (XC4VLX25-11)**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	4347.83	-	-	Clock period
T_{PHASE}	2173.91	-	-	Clock phase (DRR mode)
T_{DATA_PERIOD}	1956.52	-	-	Valid data period (0.45 x T_{CLOCK} for DDR)
T_{JITTER} (maximum)	0	0	0	Same DCM is used to generate Data and Strobe.
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	±100	100	100	Global clock tree skew for the smallest/largest clock net delay
$T_{PACKAGE\_SKEW}$	±10	10	10	Worst-case package skew for an XC4VLX25 FF668 part/package within the same region(1)
$T_{PCB\_LAYOUT\_SKEW}$	± 20	20	20	Skew between data lines on the board (167 ps/in).
$T_{PHASE\_OFFSET\_ERROR}$	± 140	140	140	Offset error between different clocks from the same DCM
Tds	*250*	*250*	*0*	Data and data mask to DK setup time (-2.5 device)
Tdh	*250*	*0*	*250*	Data and data mask to DK hold time (-2.5 device)
Total Uncertainties	-	(left side) 520	(right side) 520	
Write Window	916.52	520	1436.52	Worst-case window of 916.52 ps

Notes:

1. Package skew in the same physical region or within the same Bank, assuming package trace length information used to deskew the package during board layout.

Address and Control Timing Analysis

Address and control signals are non-DDR; therefore, the entire clock period is considered for this analysis, and no duty cycle distortion applies. Uncertainty parameters considered are global clock tree skew (±100 ps), board layout skew between CK/$\overline{CK}$ and address/control signals (around 400 ps), and package skew (around 10 ps, assuming board deskew). The address/control setup and hold times specified by the memory vendor are considered.

Table 14 shows the address and control timing analysis.

Table 14: **Address and Control Timing Analysis at 200 MHz (XC4VLX25-10)**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	5000	-	-	Clock period
T_{JITTER} (maximum)	0	0	0	Same DCM is used to generate Address and Controls.
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	±100	100	100	Global clock tree skew for the smallest/largest clock net delay.
$T_{PACKAGE\_SKEW}$	±10	10	10	Worst-case package skew for a XC4VLX25 FF668 part/package within the same region(1).
$T_{PCB\_LAYOUT\_SKEW}$	±400	400	400	Skew between data lines and clock strobes on the board (167 ps/in).
$T_{PHASE\_OFFSET\_ERROR}$	±140	140	140	Offset error between different clocks from the same DCM

Table 14: **Address and Control Timing Analysis at 200 MHz (XC4VLX25-10) *(Continued)***

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
Tas/Tcs	*400*	*400*	*0*	Address/command and input setup time (-2.5 device)
Tah/Tch	*400*	*0*	*400*	Address/command and input hold time (-2.5 device)
Total Uncertainties	-	(left side) 1050	(right side) 1050	
Address/Command Window	2900	1050	3950	Worst-case window of 2900 ps

Notes:

1. Package skew in the same physical region or within the same bank, assuming package trace length information used to deskew the package during board layout.

Table 15 shows the address and control timing analysis at 230 MHz.

Table 15: **Address and Control Timing Analysis at 230 MHz (XC4VLX25-11)**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	4347.83	-	-	Clock period
T_{JITTER} (maximum)	0	0	0	Same DCM is used to generate Address and Controls.
$T_{CLOCK\_TREE\_SKEW}$ (maximum)	±100	100	100	Global clock tree skew for the smallest/largest clock net delay.
$T_{PACKAGE\_SKEW}$	±10	10	10	Worst-case package skew for a XC4VLX25 FF668 part/package within the same region(1).
$T_{PCB\_LAYOUT\_SKEW}$	±400	400	400	Skew between data lines and clock strobes on the board (167 ps/in).
$T_{PHASE\_OFFSET\_ERROR}$	±140	140	140	Offset error between different clocks from the same DCM
Tas/Tcs	*400*	*400*	*0*	Address/command and input setup time (-2.5 device)
Tah/Tch	*400*	*0*	*400*	Address/command and input hold time (-2.5 device)
Total Uncertainties	-	(left side) 1050	(right side) 1050	
Address/Command Window	2247.83	1050	3297.83	Worst-case window of 2247.83 ps

Notes:

1. Package skew in the same physical region or within the same bank, assuming package trace length information used to deskew the package during board layout.

Design Implementation

The design targets an XC4VLX25 FF668 -10 device. The CIO Controller implements most of the features described in this application note. The datapath at speed has been tested in hardware with BL=4 and Config=2.

Resource utilization on the target device is listed in Table 16.

Table 16: **Resource Utilization**

Resource	Utilization
ILOGICs	41 out of 488 (9%)
OLOGICs	80 out of 488 (17%)
DCMs	1 out of 8 (13%)
PMCDs	0 out of 4 (0%)
BUFGMUXs	5 out of 32 (16%)
SLICEs	1300 out of 10,752 (13%)
RAMB16s	5 out of 72 (7%)
FIFO16s	4 out of 72 (5%)

Board Design Consideration

For any PC board design, Xilinx strongly suggests simulating the board and getting the best termination scheme for the application. If the user guide suggests termination on both ends of HSTL_II buses, the final PCB design can suppress some of them based on simulation. Keeping DCI available is useful for prototypes or for final production boards.

The Micron memory device has an board impedance matching capability that allows selection of a 50Ω impedance. An On-Die Termination (ODT) integrates a DCI-like termination scheme for the data bus. The ODT can be switched on or off at initialization time.

HTSL Class II

HSTL_I and HSTL_III are intended to be used in unidirectional links, and HSTL_II and HSTL_IV are intended to be used in bidirectional links. HSTL-II has a stronger driver (16 mA) than other HSTL classes (8 mA). It can hold bidirectional buses and can be used as Complementary Single-Ended (CES) for differential input or output on Virtex-4 devices with DIFF_HSTL_ II or DIFF_HSTL_II_18 attributes, with and without DCI (see UG070 [Ref 3] for a description).The reference design has some PCB routing rules. Each trace of a data word associated with one read clock QK/QK_N must be the same length as that specific Read Clock. There is also no restriction between the data words or between the read clocks.

Reference Design

The reference design for the RLDRAM II memory controller using the Direct Clocking Data Capture technique is integrated with the Memory Interface Generator (MIG) tool. This tool has been integrated with the Xilinx CORE Generator™ software. For the latest version of the design, download the IP update on the Xilinx website at:

http://www.xilinx.com/support/download/index.htm

Conclusion

RLDRAM II is a solution positioned between high-cost/bit, low-cycle time SRAM and low-cost/bit, high-cycle time DDR/DDR2 SDRAM. RLDRAM II devices provide high density, high bandwidth, and fast SRAM-like random access making them ideal for applications such as networking, graphics, and cache.

References

The following documents provide additional information useful to this application note:

1. Micron Technology, Inc.
   - *Micron TN4902.fm - Rev. A 1/20/04 EN quoted reference*
   - *mt49h16m18_4, 65 Mb CIO RLDRAM II Data Sheet*
   - *TN-49-01 RLDRAM II Design Guide*
     http://www.micron.com/products/dram/rldram/
2. XAPP701, *DDR2 SDRAM Physical Layer Using Direct-Clocking Technique*.
3. UG070, *Virtex-4 FPGA User Guide*.
4. DS302, *Virtex-4 FPGA Data Sheet: DC and Switching Characteristics*.

Appendix A

Physical Layer Interface

The RLDRAM II interface is much simpler to implement with the new Virtex-4 FPGA ChipSync feature; the IDELAY/IDELAYCTRL blocks can independently skew the data to center it to the FPGA clock. XAPP701 [Ref 2] details the implementation.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/10/04	1.0	Initial Xilinx release.
06/17/05	1.1	Added new tables: Table 10, Table 11, Table 12, Table 13, Table 15, and made changes to text.
12/05/06	1.2	Removed Appendix A and Appendix C. Appendix B is now "Appendix A." Updated the following sections: "Summary," "Design Features," and "Read Timing Analysis." Also updated Table 10 through Table 15.
04/19/07	1.3	Updates in performance and timing analysis table values due to frequency changes in MIG 1.7.
04/28/08	1.4	Fixed Figure 4, page 11. Updated "References" section.

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