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Inactive Transceiver Behavior Work-Arounds for Virtex-4 FX RocketIO MGTs

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Summary

This application note contains detailed information related to the Virtex™-4 RocketIO™ Multi-Gigabit Transceiver (MGT) Static Operating Behavior described in EN014 (Errata for Virtex-4 FX CES2 and CES3 devices), EN042, EN044 (Errata for Virtex-4 FX CES4 devices), and EN070 (Errata for Virtex-4 FX Production Step 0 and Production Step 1 devices). All information in this application note applies equally to Virtex-4 FX CES2, CES3, CES4, Production Step 0, and Production Step 1 devices unless stated otherwise.

If the static operating behavior conditions defined in the above errata documents are met for one or more of the transceivers used in a Virtex-4 FX device, the work-arounds outlined in this application note must be used. Transceivers that will never be used do not require any action.

Condition 1: Null FPGA

This condition occurs when the FPGA is powered but left unconfigured. The static operating behavior section of the errata documents EN014, EN042, EN044, and EN070 defines the cumulative time allowed in this state.

There are two possible work-arounds to this condition:

1. Simply leave the FPGA unpowered until such time as configuration can be performed.
2. If this is not possible, a temporary MGT *null bitstream* must be downloaded into the FPGA until the user design bitstream can be downloaded. The null bitstream puts every MGT in the device into a safe activity mode. These null bitstreams also protect the DCMs by keeping DCMs in continuous calibration mode.

   These bitstreams are available at:

   ftp://ftp.xilinx.com/pub/utilities/fpga/v4fx_null_bitstreams.zip

   Note: This link prompts the user to log in to a xilinx.com account and accept a license agreement. After doing so, click on the **Download Design File** link.

   To implement this solution, the board must have one of the following:

   - A permanent (nonremovable) reconfiguration pathway
   - An additional small PROM that is programmed using a qualified null bitstream provided by Xilinx

   For new designs, Xilinx recommends using a PROM and ensuring JTAG connectivity for both the PROM and FPGAs.

Condition 2: Null MGT Tile

This condition occurs when both MGTs in a tile will be used in the future, but neither MGT is instantiated in the current user design.

This condition requires a drop-in macro for both MGTs in each tile. The macro puts each individual MGT into a safe activity mode. These macros are available at:

http://www.xilinx.com/xlnx/xweb/xil_publications_file.jsp?iLanguageID=1&ipoid=24332297&category=-1210767&filename=Null_Tile.zip&file=539

Note: This link prompts the user to log in to a xilinx.com account and accept a license agreement. After doing so, click on the "Download Design File" link.

Condition 3: MGTA or MGTB Only

This condition occurs when both MGTs in a tile will be used in the future, but only one MGT is instantiated in the current user design.

This condition requires the user design to instantiate the currently unused MGT in the tile with the appropriate Calibration Block, if required. The sections below outline what must be done, depending on silicon target.

CES2, CES2L, CES2R, CES3, CES3L, CES3R

1. Connect a reference clock to the MGT.
2. Calibration Block v1.1.1 or v1.2.2 must be instantiated.
3. Calibration Block TX_SIGNAL_DETECT and RX_SIGNAL_DETECT ports must be tied Low.

CES2V2, CES2L2, CES2R2, CES3V2, CES3L2, CES3R2

1. Connect a reference clock to the MGT.
2. Calibration Block v1.2.2 must be instantiated.
3. Calibration Block TX_SIGNAL_DETECT and RX_SIGNAL_DETECT ports must be tied Low.

CES4, Production Step 0 C-Grade, Production Step 1 I-Grade

1. Connect a reference clock to the MGT.
2. No Calibration Block is required.
3. 8B/10B Encoder must be enabled on the transmitter.
   a. Set TXBYPASS8B10B MGT port to `8'h00`.
   b. Set TXENC8B10BUSE MGT port to `1'b1`.
   c. Supply TXUSRCLK and RXUSRCLK.
4. Serial Loopback must be enabled.
   a. Set LOOPBACK MGT port to `2'b11`.
   b. Set TXPOST_TAP_PD MGT Attribute to FALSE.

Production Step 1 C-Grade

1. Connect a reference clock to the MGT.
2. No calibration Block is required.
3. Supply TXUSRCLK and RXUSRCLK.

Condition 4: Inactive MGT

This condition occurs when one or both MGTs in a tile will be used in the future and are instantiated in the user design, but are not currently receiving data.

This condition requires the user design to take certain action when the receiver is inactive. The sections below outline what must be done depending on silicon target.

CES2, CES2L, CES2R, CES3, CES3L, CES3R

1. Calibration Block v1.1.1 or v1.2.2 must be instantiated.
2. Calibration Block TX_SIGNAL_DETECT port must be tied Low because these silicon targets must use 8B/10B data.
3. Calibration Block RX_SIGNAL_DETECT port must be controlled by user logic that detects when the MGT receiver is inactive (dynamic data not present on RXP / RXN).

CES2V2, CES2L2, CES2R2, CES3V2, CES3L2, CES3R2

1. Calibration Block v1.2.2 must be instantiated.
2. Calibration Block TX_SIGNAL_DETECT port must be tied Low because these silicon targets must use 8B/10B data.
3. Calibration Block RX_SIGNAL_DETECT port must be controlled by user logic that detects when the MGT receiver is inactive (dynamic data not present on RXP / RXN).

CES4, Production Step 0 C-Grade, Production Step 1 I-Grade

1. Calibration Block v1.4.1 is required if TXPOST_TAP_PD = TRUE.
   a. Calibration Block TX_SIGNAL_DETECT port must be tied Low because these silicon targets must use 8B/10B data.
   b. Calibration Block RX_SIGNAL_DETECT port must be controlled by user logic that detects when the MGT receiver is inactive (dynamic data not present on RXP / RXN).
2. Calibration Block v1.4.1 is not required if TXPOST_TAP_PD = FALSE.
   a. 8B/10B Encoder must be enabled for this silicon target.
      - Set TXBYPASS8B10B MGT port to `8'h00`.
      - Set TXENC8B10BUSE MGT port to `1'b1`.
      - Supply TXUSRCLK and RXUSRCLK.
   b. Serial Loopback must be enabled.
      - Pre-emphasis is in use: set TXPOST_TAP_PD MGT attribute statically to FALSE.
      - LOOPBACK MGT set to `2'b11` when receiver becomes inactive.

Production Step 1 C-Grade

1. No Calibration Block is required.
2. Supply TXUSRCLK and RXUSRCLK.

Detecting an Inactive Receiver

An MGT receiver is *inactive* when no dynamic data is transitioning on the RXP / RXN pins at the user line rate. This section explains methods by which the user can detect this condition.

Small Form-Factor Pluggable Optical Transceiver

In a system where the RocketIO MGT is connected to a Small Form-factor Pluggable (SFP) Optical Transceiver, the end user can unplug the cable from the SFP module causing the optical link to go dark. This in turn causes the MGT receiver to be inactive. SFP transceivers provide a pin called LOS, indicating loss of signal. This pin can be connected to the FPGA logic that drives either the RX_SIGNAL_DETECT port on the Calibration Block or the LOOPBACK port on the MGT if a Calibration Block is not in use. See section "Condition 4: Inactive MGT" for more information about Calibration Block usage rules.

Using RXSIGDET Port of MGT to Detect Inactive Receiver

In systems where there are no external means to detect an inactive receiver, the RXSIGDET MGT port can be used. RXSIGDET is normally used to detect the presence of out-of-band (OOB) signaling. When High, the RXSIGDET port indicates that an OOB signal is detected at the RXP / RXN pins. Specifically, when the voltage differential between RXP and RXN is below a threshold $RXOOB_{VDPP}$, RXSIGDET is asserted. The attribute RXCDRLOS is used to set the threshold level of the incoming signal that is recognized as OOB.

There are four possible scenarios to consider:

1. *RXP/RXN floating, physically not connected (e.g., SMA cables not connected) and internally AC-coupled (using on-chip AC coupling caps):*

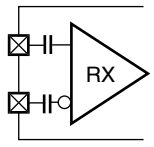

Figure 1: **RXP/RXN Floating, Internally AC-Coupled**

   When floating the RXP/RXN inputs, the internal inputs to the RXSIGDET circuit are connected to a common-mode DC. Set RXCDRLOSS to `001010`. This ensures that the threshold is substantially higher than the common-mode DC of the RXSIGDET circuit, and that noise does not trip the output of RXSIGDET.

   After this threshold has been set, RXSIGDET is asserted if the receiver's inputs are disconnected (receiver rendered inactive).

2. *RXP/RXN floating, physically not connected (e.g., SMA cables not connected) and internally DC-coupled (no internal coupling caps):*

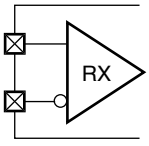

Figure 2: **RXP/RXN Floating, Internally DC-Coupled**

   For this case, VTRX must be left floating. When floating the RXP/RXN inputs, the internal inputs to the RXSIGDET circuit are connected to a common-mode DC. Set RXCDRLOSS to `001010` and make sure VTRX is left floating. This ensures that the threshold is substantially higher than the common-mode DC of the RXSIGDET circuit and that noise does not trip the output of RXSIGDET.

After this threshold has been set, RXSIGDET is asserted if the receiver's inputs are disconnected (receiver rendered inactive).

3. *RXP/RXN connected with static differential DC 0 or DC 1 on inputs (inputs are railed) and AC-coupled serial link (both internal and external coupling caps):*

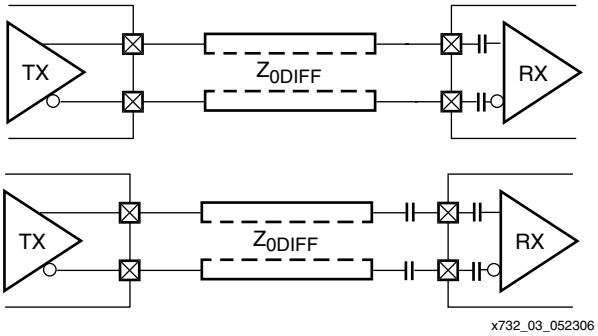

Figure 3: **RXP/RXN Connected with Static DC 0 or DC 1, AC-Coupled**

When the link is internally AC-coupled, no DC signal is actually getting through to the internal nodes of the receiver. This is similar to disconnecting the inputs of the MGT for a DC signal. Set RXCDRLOSS to `001010`. The case of external AC coupling with internal AC coupling caps bypassed is not a supported use case with the RXSIGDET circuit.

Note: For RXSIGDET to reliably be used as an indicator of signal presence on the RX, the minimum differential signal amplitude must be at least 450 mV_{ppd} (225 mV_{ppse}) when RXCDRLOS is set to `001010`. This data is based on Monte Carlo simulation functional extreme corners (for repetitive patterns).

After the threshold has been set, RXSIGDET is asserted if dynamic data is not seen at the receiver.

4. *RXP/RXN connected with static differential DC 0 or DC 1 on inputs (inputs are railed) and DC-coupled serial link (no internal or external coupling caps):*

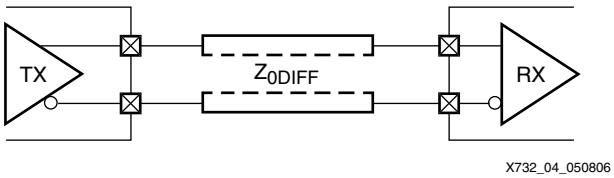

Figure 4: **RXP/RXN Connected with Static DC 0 or DC 1, DC-Coupled**

If the transmitter is driving static differential DC 0 or DC 1 on a DC-coupled link, the RXSIGDET port cannot be used to detect an inactive receiver.

References

1. UG076, *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide*
2. DS302, *Virtex-4 Data Sheet: DC and Switching Characteristics*
3. Virtex-4 Family Errata Page on the Xilinx website

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/23/06	1.0	Initial Xilinx release.
09/25/07	1.1	• Added author name. • Modified "Summary." • Changed Calibration Block version, removed 8B/10B encoding, and added RXUSRCLK to "Condition 3: MGTA or MGTB Only" and "Condition 4: Inactive MGT." • Renamed "CES4, Production Step 0 C-Grade, Production Step 1 I-Grade." • Added "Production Step 1 C-Grade" in "Condition 3: MGTA or MGTB Only." • Changed TX_SIGNAL_DETECT port to Low in "CES2, CES2L, CES2R, CES3, CES3L, CES3R." • Renamed and modified "CES4, Production Step 0 C-Grade, Production Step 1 I-Grade." • Added "Production Step 1 C-Grade" in "Condition 4: Inactive MGT." • Removed reference to transmit in definition of Condition 4. • Deleted section **Affects of TXINHIBIT and TXENOOB**. • Changed 400 mV_{ppse} to 400 mV_{ppd} in scenario 3 of "Using RXSIGDET Port of MGT to Detect Inactive Receiver." • Removed references to Answer Records. • Updated URL link to null bitstreams.