XAPP771 (v1.0) June 13, 2005

Synthesizable CIO DDR RLDRAM II Controller for Virtex-II Pro FPGAs

Author: Rodrigo Angel

Summary

This application note describes how to use a Virtex™-II Pro device to interface to Common I/O (CIO) Double Data Rate (DDR) Reduced Latency DRAM (RLDRAM II) devices. The reference design targets two CIO DDR RLDRAM II devices at a clock rate of 270 MHz with data transfers at 540 Mb/s per pin.

Introduction

This application note describes a CIO DDR RLDRAM II controller design implemented in a Virtex-II Pro device. The first section briefly reviews RLDRAM II functionality; the following sections describe implementation and timing analysis details.

RLDRAM II Devices

The second generation of reduced latency DRAM is a high-performance memory combining the performance-critical features that networking and cache applications need, such as high density (up to 288 Mb), high bandwidth (up to 28.8 Gb/s), and fast SRAM-like random access.

RLDRAM II is based on a new internal eight-bank architecture that minimizes the time between the beginning of the access cycle and the availability of the first data. So, this memory provides minimized latency and reduced row cycle times ideal for applications such as networking, graphics, and cache that require critical response times and very fast random access.

RLDRAM II operates at a clock frequency of up to 400 MHz and uses a DDR interface. The DDR interface transfers two 36-bit, 18-bit, or 9-bit-wide data words per clock cycle at the I/O pins. Output data is referenced to the free-running output data clock. Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock.

The CIO RLDRAM II device has a shared data READ/WRITE port requiring a bidirectional data bus. During READ commands, the data is output from the device and is referenced to both edges of the QK clocks. During WRITE commands, the data is input to the device and is sampled at both edges of the DK clocks.

Read and write accesses to the RLDRAM II are burst-oriented. The burst length is programmable at 2, 4, or 8 through the Mode register.

RLDRAM II I/Os use the 1.5V or 1.8V HSTL I/O standard.

Clocking

The RLDRAM II device requires a differential input master clock pair, CK and CK#. Ideally, CK and CK# are 180° out of phase to provide the best system margins. Only the rising edge of CK is utilized for address and control latching.

Another requirement is a differential input data clock pair, DK and DK#. Both rising edges of DK and DK# are center-aligned with the write data and utilized to latch the write data into the memory device. Ideally, DK and DK# are 180° out of phase, providing the best margin on write data. For the x36 configuration, two differential input data clock pairs are available, with DQ0 through DQ17 referenced to DK0 and DK0#, and DQ18 through DQ35 referenced to DK1 and DK1#.

The last set of clocks is the differential output data clock pair, QK and QK#. During a READ from the device, QK and QK# are transmitted by the RLDRAM II and edge-aligned with the

© 2005 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc.
All other trademarks are the property of their respective owners.

output data. For the x36 configuration, two differential data clock pairs are available, with DQ0 through DQ17 referenced to QK0 and QK0#, and DQ18 through DQ35 referenced to QK1 and QK1#.

Mode Register

The Mode register stores data that controls the operating modes of the memory. It programs the RLDRAM II configuration, burst length, test mode, and I/O options. During a MODE REGISTER SET command, the address inputs A[17:0] are sampled and stored in the Mode register (see Table 1). The Mode register may be configured at any time during device operation.

Table 1: **Mode Register Fields**

Address Bits	Field Name	Description
A[17:10]	Reserved	Must be set to zero
A9	On-Die Termination	0 - Disabled 1 - Enabled
A8	Impedance Matching	0 - Internal 50Ω 1 - External
A7	DLL Reset	0 - DLL reset 1 - DLL enabled
A6	Unused	-
A5	Address Mux	0 - Non-multiplexed 1 - Multiplexed
A[4:3]	Burst Length (BL)	00 - 2 01 - 4 10 - 8 11 - Not valid
A[2:0]	Configuration	000 - 0 (BL of 8 not available) 001 - 1 (BL of 8 not available) 010 - 2 011 - 3 100 to 111 - Reserved

Configuration Table

Table 2 shows the different RLDRAM II configurations that can be programmed into the Mode register for different operating frequencies. The read and write latency (t_{RL} and t_{WL}) values and the row cycle times (t_{RC}) are shown in clock cycles as well as in nanoseconds.

Table 2: **RLDRAM II Configurations**

Frequency	Symbol	Configuration			Unit
		1	2	3	
	t_{RC}	4	6	8	cycles
	t_{RL}	4	6	8	cycles
	t_{WL}	5	7	9	cycles
400 MHz	t_{RC}	-	-	20.0	ns
	t_{RL}	-	-	20.0	ns
	t_{WL}	-	-	22.5	ns
300 MHz	t_{RC}	-	20.0	26.7	ns
	t_{RL}	-	20.0	26.7	ns
	t_{WL}	-	23.3	30.0	ns
200 MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	20.0	30.0	40.0	ns
	t_{WL}	25.0	35.0	45.0	ns

Address Bus

Table 3 shows the address bus usage for different burst lengths and configurations.

Table 3: **Address Bus Usage**

Burst Length (BL)	Configuration		
	x36	x18	x9
2	[18:0]	[19:0]	[20:0]
4	[17:0]	[18:0]	[19:0]
8	Not Available	[17:0]	[18:0]

Commands

Table 4 describes commands used with the RLDRAM II device.

Table 4: **RLDRAM II Commands**

Command	Description
DESEL/NOP	The NOP (No operation) instruction to the RLDRAM II deselects the device.
MRS	The Mode register is set via the address inputs A[17:0]. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command initiates a burst read access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank.

Table 4: **RLDRAM II Commands *(Continued)***

Command	Description
WRITE	The WRITE command initiates a burst write access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank. Input data appearing on the DQ bus is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is Low, the corresponding data is written to memory. If the DM signal is High, the corresponding data inputs are ignored (that is, this part of the data word is not written).
AREF	The AREF command is used during normal operation of the RLDRAM II to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA[2:0] inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a “Don’t Care” during the AREF command. The RLDRAM II requires 64K cycles at an average periodic interval of 0.49 µs (maximum). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM II at periodic intervals of 3.9 µs.

Bank Usage

The Mode register controls both the burst length and the RLDRAM II configuration. The selected t_{RC} defines how frequently any one bank can be accessed, while the burst length determines how often a new address is required.

Banks can be accessed in any order at any time as long as t_{RC} is met before revisiting a bank. One method to optimize the use of the eight-bank architecture offered by the RLDRAM II is to read data from or write data to the device using a round-robin approach.

CIO DDR RLDRAM II Controller Implementation Details

Figure 1 shows a top-level block diagram of the CIO DDR RLDRAM II Controller.

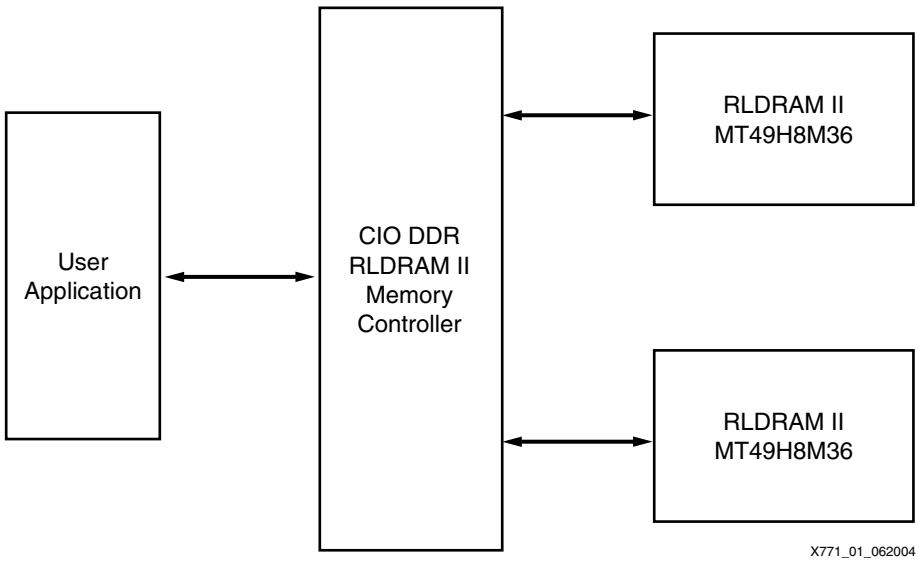


Figure 1: **CIO DDR RLDRAM II Controller (Top Level)**

Design Features

The key features of the CIO DDR RLDRAM II Controller design are:

- Compliance with the RLDRAM II specification from Micron. [Ref 1]
- Data interface width of 72 bits using two MT49H8M36FM-33 devices from Micron, supporting two devices x 8M x 36 bits
- Common I/O mode for the data bus (that is, bidirectional data bus)
- Physical layer delays QK (read memory clock) using LUTs, which are configured as delay elements. A separate calibration circuit continuously calibrates the delay through each LUT. The delayed QK is routed on low skew hex line resources to clock read data from the memories into CLB flip-flops. The Physical layer for this interface is explained in detail in XAPP678C and XAPP688C. [Ref 2]
- Memory interface speed of 270 MHz, DDR 540 Mb/s
- FIFO-based user interface
- Burst lengths of 2 and 4
- Mode register set to Configuration 2
- Non-multiplexed address bus
- Auto-refresh and/or user-controlled refresh

Block Diagram Description

Figure 2 shows a detailed block diagram of the CIO DDR RLDRAM II Memory Controller. The major blocks are described after the figure.

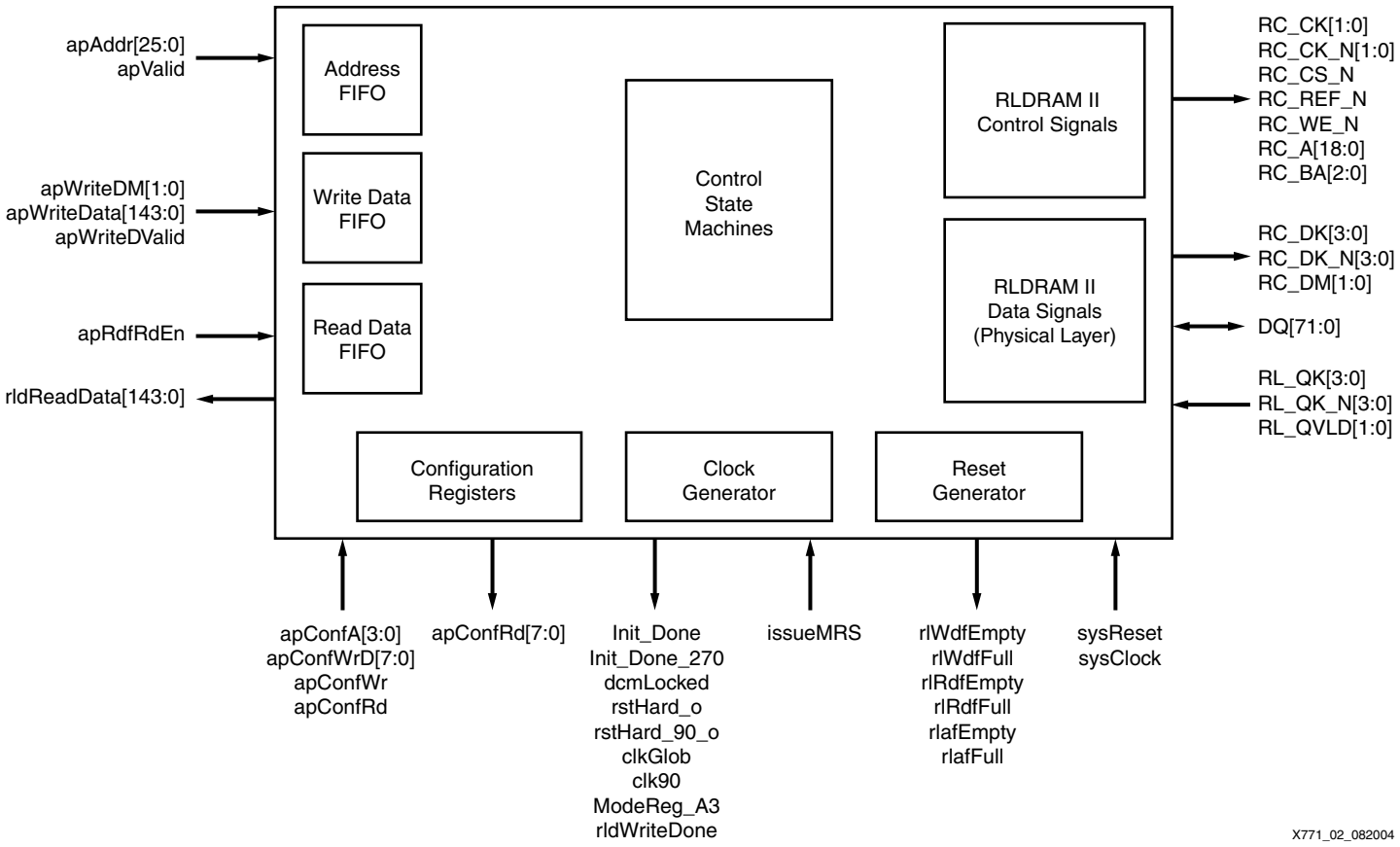


Figure 2: **CIO DDR RLDRAM II Controller (Detailed)**

User Interface

The backend interface of the controller is a FIFO-based implementation. Three FIFOs are used: an Address FIFO, a Write Data FIFO, and a Read Data FIFO. The user interface also provides a configuration register and some other control signals.

Address FIFO

This FIFO serves as the buffer for the backend interface to store addresses corresponding to the read and write data as well as the user-controlled refreshes. All reads, writes, and user refreshes are scheduled in this FIFO. This synchronous FIFO is 26 bits wide and 16 words deep. Table 5 defines the configuration of the 26 bits.

Table 5: **Address FIFO Bit Configuration**

Bit Configuration	Description
25	User Refresh
24	Read/Write#
[23:22]	Reserved
[21:3]	Memory Address bits A[18:0]
[2:0]	Memory Bank Address bits BA[2:0]

Write Data FIFO

This FIFO serves as a buffer for the backend interface to store data that needs to be written into the memory. This synchronous FIFO is 146 bits wide and 15 words deep. For a burst length of 2, each location in the Write Data FIFO constitutes the required data. For a burst length of 4, two locations in the Write Data FIFO constitute the required data. Table 6 defines the configuration of the 146 bits.

Table 6: **Write Data FIFO Bit Configuration**

Bit Configuration	Description
[145:144]	Write Data Mask
[143:0]	Write Data

Read Data FIFO

This 4x36-bit wide FIFO serves as a buffer for the controller to store data it has read from the memory. It is 16 words deep. For a burst length of 2, each location in the Read Data FIFO constitutes the data read from the memory. For a burst length of 4, two locations in the Read Data FIFO constitute the data read from the memory. Table 7 defines the configuration of the 144 bits.

Table 7: **Read Data FIFO Bit Configuration**

Bit Configuration	Description
[143:0]	Read Data

Configuration Registers

This block provides an interface for the application to read from and write to the configuration registers (MRS). For example, Auto Refresh is ON by default, making the controller send AREF commands to the memories at the required intervals. The user can turn Auto Refresh OFF via the confCycRef bit. In this case, the user is responsible for issuing USER REFRESH commands.

Similarly, the Burst Length can be changed at either compile time in the code or it can be reprogrammed during run time via the confMReg[4:3] bits.

Clock Generator

This block generates the clocks for the controller by using the system clock and a DCM.

Reset Generator

This block generates different reset signals. It also performs the initialization and configuration (MRS) of the RLDRAM II memories.

Control State Machines

This block has a state machine that controls NOP, READ, WRITE, AUTO REFRESH, and USER REFRESH operations from and to the memories.

RLDRAM II Control Signals Physical Layer

This block has the pads that interface with the RLDRAM II control and address signals.

RLDRAM II Data Signals Physical Layer

This block has the pads that interface with the RLDRAM II data signals. The calibration circuit and the data path circuit are also implemented here. Refer to XAPP678C and XAPP688C for more details. [Ref 2]

Pin Descriptions

Table 8 provides pin descriptions for the CIO DDR RLDRAM II Controller.

Table 8: **CIO DDR RLDRAM II Controller Pin Descriptions**

Pin Name	Pin Direction	Description
Interface to User Application		
apAddr[25:0]	In	Address FIFO data input, synchronous with clkGlob
apConfA[3:0]	In	Configuration registers address bus, synchronous with clkGlob
apConfRd	In	Configuration registers read enable, synchronous with clkGlob
apConfRdD[7:0]	Out	Configuration registers read data, synchronous with clkGlob
ApConfWr	In	Configuration registers write data valid, synchronous with clkGlob
apConfWrD[7:0]	In	Configuration registers write data, synchronous with clkGlob
apRdfRdEn	In	Read Data FIFO read enable, synchronous with clk90
apValid	In	Address FIFO data valid input, synchronous with clkGlob
apWriteData[143:0]	In	Write Data FIFO data input, synchronous with clkGlob
apWriteDM[1:0]	In	Write Data FIFO data mask input, synchronous with clkGlob
apWriteDValid	In	Write Data FIFO data valid input, synchronous with clkGlob

Table 8: **CIO DDR RLDRAM II Controller Pin Descriptions *(Continued)***

Pin Name	Pin Direction	Description
clk90	Out	270 MHz CLK90 output from DCM
clkGlob	Out	270 MHz CLK0 output from DCM
dcmLocked	Out	Indicates that DCM is locked, synchronous with clkGlob
Init_Done	Out	Indicates that memory initialization has completed, synchronous with clkGlob
Init_Done_270	Out	Indicates that memory initialization has completed, synchronous with clk270
issueMRS	In	A pulse on this input makes controller program Mode register into the memory, synchronous with clkGlob. (At power-up, MRS is done as part of the initialization)
ModeReg_A3	Out	Mode register A3 bit, which can be used to differentiate between burst lengths of 2 and 4, synchronous with clkGlob
rlafEmpty	Out	Address FIFO empty flag, synchronous with clkGlob
rlafFull	Out	Address FIFO full flag, synchronous with clkGlob
rldReadData[143:0]	Out	Read Data FIFO data output, synchronous with clk90
rldWriteDone	Out	Indicates that a write to memory has completed, synchronous with clkGlob
rlRdfEmpty	Out	Read Data FIFO empty flag, synchronous with clk90
rlRdfFull	Out	Read Data FIFO full flag, synchronous with clk90
rlWdfEmpty	Out	Write Data FIFO empty flag, synchronous with clkGlob
rlWdfFull	Out	Write Data FIFO full flag, synchronous with clkGlob
rstHard_90_o	Out	Active-High reset until DCM is locked, synchronous with clk90
rstHard_o	Out	Active-High reset until DCM is locked, synchronous with clkGlob
sysClk	In	System clock
sysReset	In	Active-High system reset
Interface to two CIO DDR RLDRAM II Devices		
DQ[71:0]	In/Out	Data input/outputs. During READ commands, the data is sampled at both edges of QK. During WRITE commands, the data is referenced to both edges of DK.
RC_A[18:0]	Out	Row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings.
RC_BA[2:0]	Out	Bank addresses that select to which internal bank a command is being applied
RC_CK[1:0] RC_CK_N[1:0]	Out	Master differential clocks

Table 8: **CIO DDR RLDRAM II Controller Pin Descriptions *(Continued)***

Pin Name	Pin Direction	Description
RC_CS_N	Out	Chip select command
RC_DK[3:0] RC_DK_N[3:0]	Out	Differential write data clocks
RC_DM[1:0]	Out	Data mask signals for write data
RC_REF_N	Out	Refresh command
RC_WE_N	Out	Write enable command
RL_QK[3:0] RL_QK_N[3:0]	In	Differential read data clocks transmitted by the RLDRAM II devices and edge-aligned with read data.
RL_QVLD[1:0]	In	Data valid signals transmitted by the RLDRAM II devices. Indicate valid read data.

Memory Initialization

The RLDRAM II device must be powered up and initialized in a predefined manner. The initialization sequence is handled by the controller as follows:

1. After all power supply and reference voltages are stable and the master clock (RC_CK) is stable, the RLDRAM II requires a 200 µs (minimum) delay prior to applying an executable command.
2. After the 200 µs (minimum) delay has passed, three MODE REGISTER SET commands are issued: two dummies plus one valid MRS.
3. Six clock cycles (t_{MRSC}) after the valid MRS, eight AUTO REFRESH commands are issued, one on each bank and separated by 2,048 cycles.
4. After six clock cycles (t_{RC}) for Configuration 2, initialization is complete. The chip is ready for normal operation as indicated by the Init_Done(_270) outputs to the application.

Clocking Methodology and Read/Write Datapaths

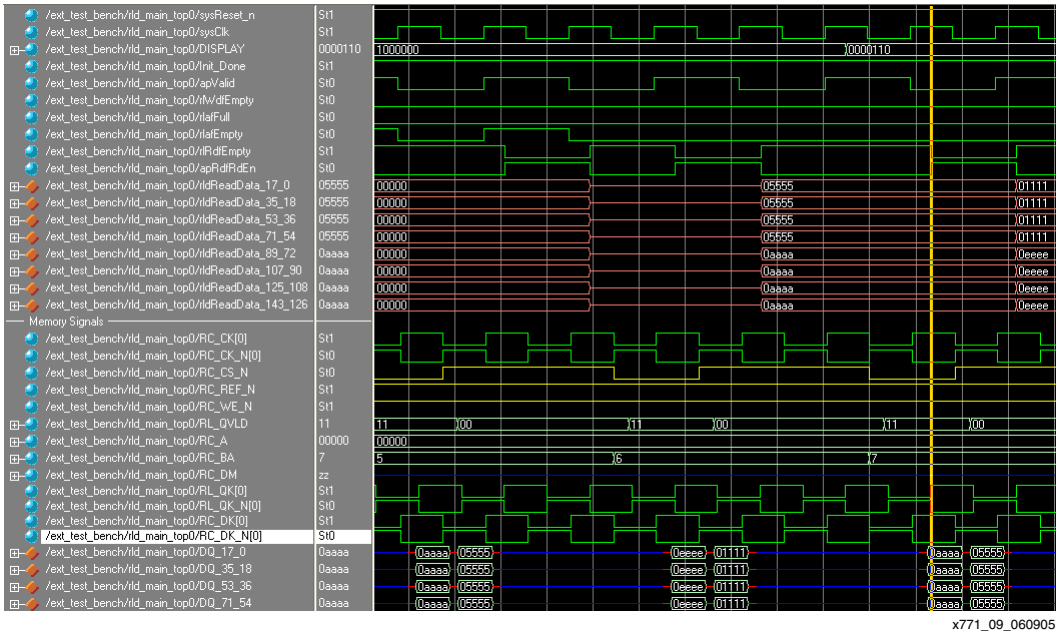
The clocking methodology, read datapath, and write datapath implemented in this design are explained in detail in XAPP678C and XAPP688C. [Ref 2]

User Interface and RLDRAM II Interface Simulation Waveforms

This section provides read and write waveforms for burst lengths of 2 and 4. A screen capture from the Xilinx ChipScope™ tool appears in Figure 7.

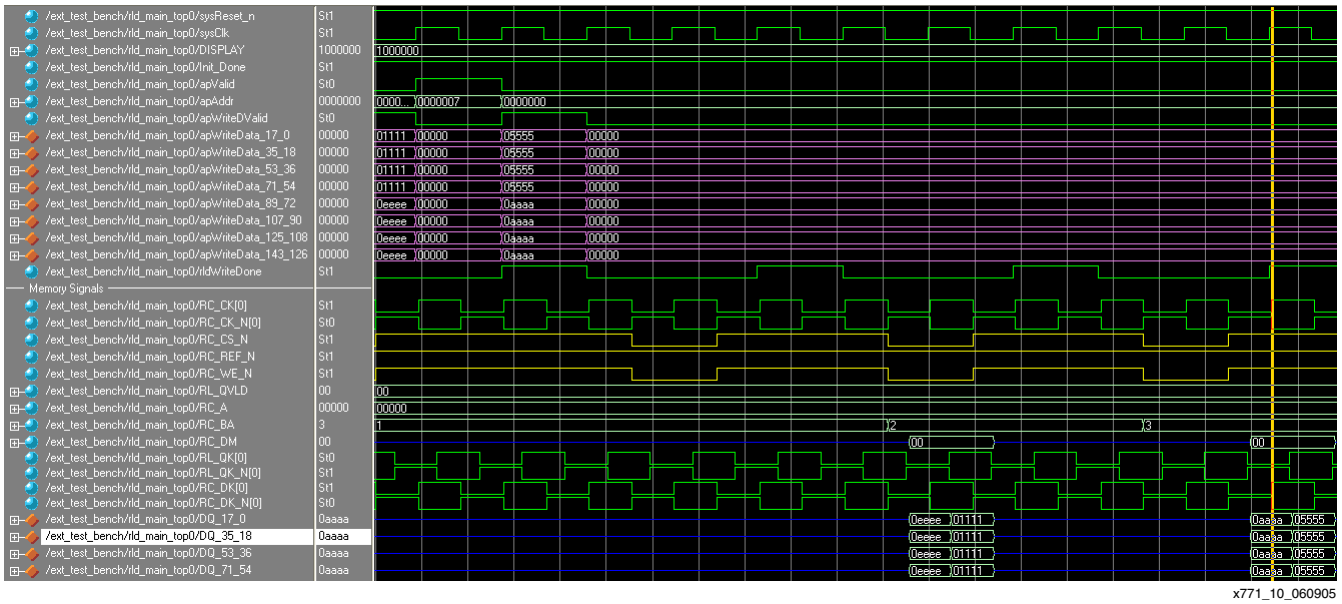
Burst Length = 2

Figure 3 shows the simulation waveforms for an RLDRAM II read operation with BL = 2. Figure 4 shows the simulation waveforms for an RLDRAM II write operation with BL = 2.



x771_09_060905

Figure 3: **Read Simulation Waveforms (BL = 2)**

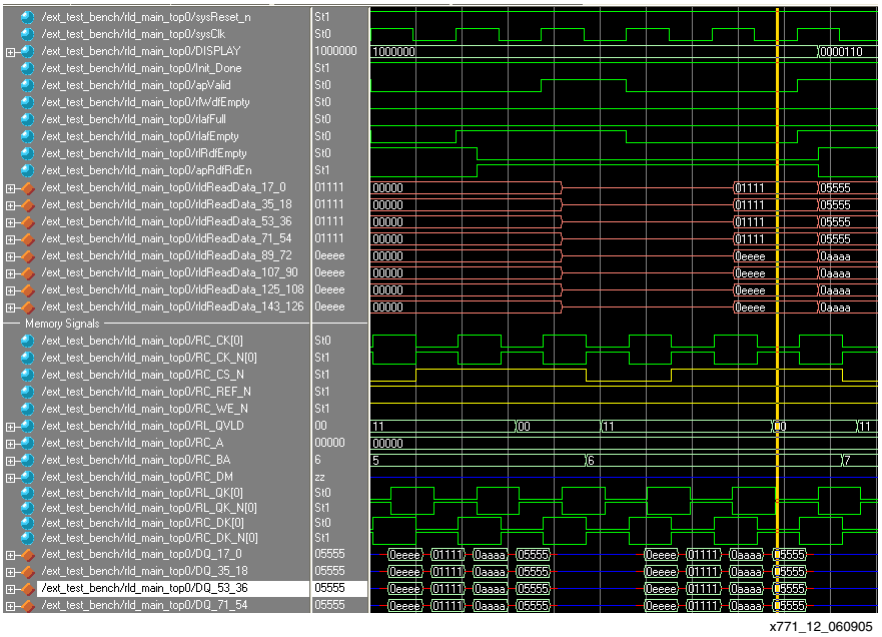


x771_10_060905

Figure 4: **Write Simulation Waveforms (BL = 2)**

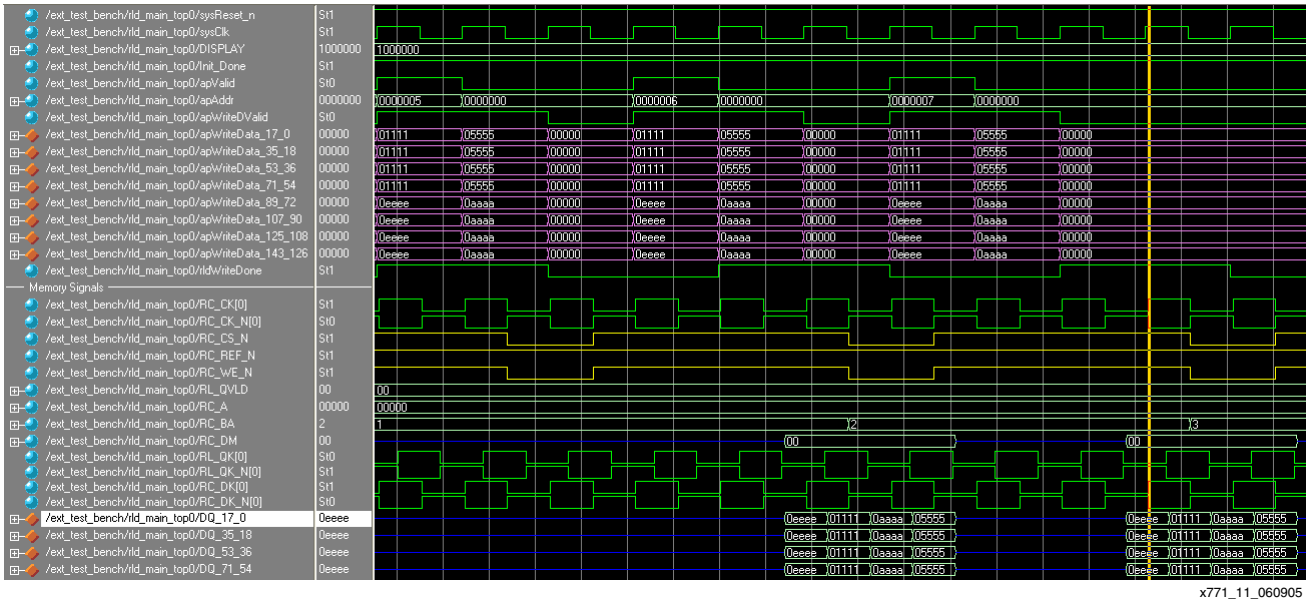
Burst Length = 4

Figure 5 shows the simulation waveforms for an RLDRAM II read operation with BL = 4.
Figure 6 shows the simulation waveforms for an RLDRAM II write operation with BL = 4.



x771_12_060905

Figure 5: **Read Simulation Waveforms (BL = 4)**



x771_11_060905

Figure 6: **Write Simulation Waveforms (BL = 4)**

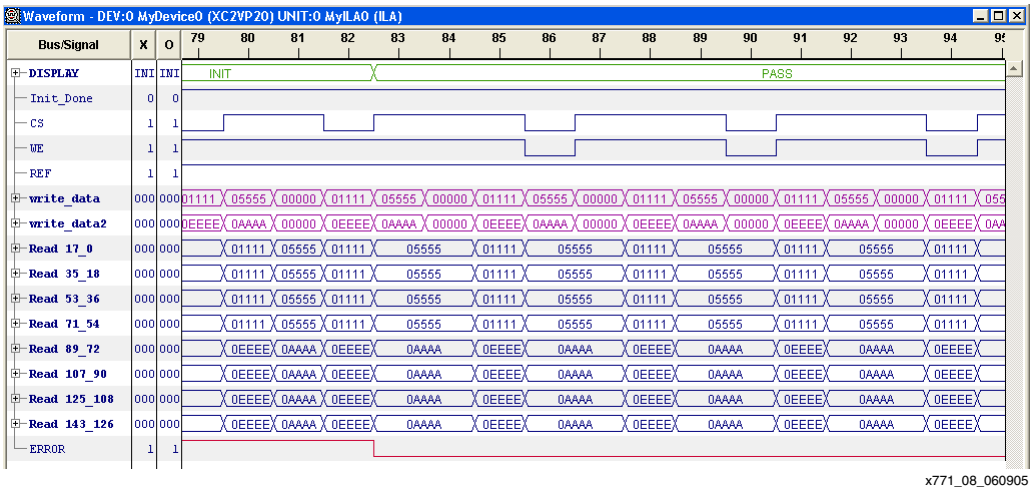


Figure 7: **ChipScope Display of Design**

I/O Timing Analysis

This section provides a timing analysis of the reference design. The analysis uses an XC2VP20-FF1152-7 device and an MT49H8M36FM-33 device from Micron for the timing parameters. The parameters in *italic*s in Table 9 through Table 11 are taken from Micron's data sheet. [Ref 1]

Table 9: **Read Timing Analysis @ 270 MHz**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
Tclock	3703			Clock period
Tphase	1851.5			Clock phase
Tmem_dcd	*185.15*			*Duty-cycle distortion from memory DLL (Tphase x 0.10)*
Tdata_period	1666.35			Total data period (Tphase – Tmem_dcd)
Tqkq	*350*	*350*	*350*	*QK edge to any output data edge*
Tsetup	210	210	0	Setup time from Virtex-II Pro data sheet, 2VP -7 part
Thold	40	0	40	Hold time from Virtex-II Pro data sheet, 2VP -7 part
Tlocal_clock_line	30	30	30	Worst-case skew on the local clock resource
Tpackage_skew	0(1)	0	0	Worst-case package skew for 2VP20 FF1152 part/package
Tpcb_layout_skew	100	100	100	Skew between data lines on the board
Tjitter	0	0	0	Data and strobe jitter together because they are generated off the same clock
Total Uncertainties		690	520	
Read Window	456.35	690	1146.35	Worst-case window of 456.35 ps

Notes:
1. 0 because this parameter is included in Tpcb_layout_skew.

Table 10: **Write Timing Analysis @ 270 MHz**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
Tclock	3703			Clock period
Tphase	1851.5			Clock phase
Tmem_dcd	*185.15*			*Duty cycle distortion from memory DLL (Tphase x 0.10)*
Tdata_period	1666.4			Total data period (Tphase - Tmem_dcd)
Tds	*300*	*300*	*0*	*Data-in and data mask to DK setup time*
Tdh	*300*	*0*	*300*	*Data-in and data mask to DK hold time*
Tglobal_clock_skew	50	50	50	Worst-case skew on the global clock resource
Tpcb_layout_skew	100	100	100	Skew between data lines on the board
Tpackage_skew	0(1)	0	0	Worst-case package skew for a 2VP20 FF1152 part/package
Tphase_offset_error	140	140	140	Offset error between different clocks from the same DCM
Tjitter	0	0	0	Same DCM is used to generate clock and data, hence they jitter together
Total Uncertainties		590	590	
Write Window	486.35	590	1076.35	Worst-case window of 486.35 ps

Notes:
1. 0 because this parameter is included in Tpcb_layout_skew.

Table 11: **Address and Control Timing Analysis @ 270 MHz**

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
Tclock	3703			Clock period
Tas/Tcs	*500*	*500*	*0*	*Address/Command and input setup time*
Tah/Tch	*500*	*0*	*500*	*Address/Command and input hold time*
Tglobal_clock_skew	50	50	50	Worst-case skew on the global clock resource
Tpcb_layout_skew	100	100	100	Skew between data lines on the board
Tpackage_skew	0(1)	0	0	Worst-case package skew for a 2VP20 FF1152 part/package
Tphase_offset_error	140	140	140	Offset error between different clocks from the same DCM
Tduty_cycle_distortion	0	0	0	Duty-cycle distortion does not apply
Tjitter	0	0	0	Same DCM is used to generate clock and data, hence they jitter together
Total Uncertainties		790	790	
Address/Command Window	2123	790	2913	Worst-case window of 2123 ps

Notes:
1. 0 because this parameter is included in Tpcb_layout_skew.

Board Considerations

Board design considerations, such as signal integrity analysis, pinouts per Weighted Average Simultaneously Switching Outputs (WASSO) guidelines, layout considerations, and schematics are provided in the ML367 User Guide. [Ref 2]

Design Implementation

The design targets an XC2VP20-FF1152-7 device. Table 12 lists the tools used for verification and design implementation.

Table 12: **Verification and Design Implementation Tools**

Tool Name	Type	Version
ModelSim SE	Simulation	5.7e
Xilinx ISE	XST Synthesis and Implementation	6.3i SP0 (G.30)

Resource utilization on the target part is listed in Table 13.

Table 13: **Resource Utilization**

Resource	Utilization
DCMs	2 out of 8 (25%)
SLICEs	2602 out of 9280 (28%)
BUFGMUXs	5 out of 16 (31%)
RAMB16s	6 out of 88 (6%)

Hardware Verification

This design is verified and characterized on the ML367 platform using a XC2VP20-7FF1152 device. The performance in the worst corner is 288 MHz.

Conclusion

RLDRAM II is a solution between high-cost/bit low-cycle time SRAM and low-cost/bit high-cycle time DDR/DDR2 SDRAM. Offering fast, high-density, high-bandwidth, SRAM-like random access makes RLDRAM II devices ideal for applications such as networking, graphics, and cache.

The Verilog reference design is a 72-bit CIO version of the controller supporting two 36-bit wide devices from Micron. This reference design is available for downloading at:

http://www.xilinx.com/bvdocs/appnotes/xapp771.zip

References

The following documents provide additional information useful to this application note:

1. Micron Technology, Inc.
   - MT49H8M36_4, *288Mb CIO RLDRAM II Data Sheet*
     TN-49-01, *RLDRAM II Design Guide,* http://www.rldram.com
2. Xilinx, Inc.
   - XAPP678C, *Data Capture Technique Using CLB Flip-Flops*
     XAPP688C, *Creating High-Speed Memory Interfaces with Virtex-II and Virtex-II Pro FPGAs*
     http://www.xilinx.com/products/design_resources/mem_corner/resource/xaw_dram_ddr.htm
     First time users: Click on "HDL Code" next to XAPP688 to register and sign the license agreement.
   - UG141, *ML367 Demo Board User Guide*
     http://www.xilinx.com/userguides/ug141.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/13/05	1.0	Initial Xilinx release.