XAPP803 (v1.1) July 18, 2006

Leveraging "In-System ECO" Capability of Virtex-4 EasyPath FPGAs

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Summary

Xilinx EasyPath™ FPGAs provide the industry's only low-cost and flexible high-volume solution. The migration from a standard FPGA prototype to the corresponding high-volume EasyPath solution is conversion-free and one-for-one in terms of all the features. Even after volume shipments have begun, customers can take advantage of the "In-System ECO" (Engineering Change Orders) capability in Virtex™-4 EasyPath FPGAs to make changes to LUTs and I/Os. This application note describes how to make these changes in a simple way using the FPGA Editor tool.

Introduction

Xilinx EasyPath FPGAs are the industry's only customer-specific solution for volume production that is priced below Structured ASIC prices and retains some flexibility features. These flexibility features include the following:

- Ability to make In-System ECOs
- Ability to test a single device for multiple bitstreams
- Ability to start volume production 8-12 weeks after design freeze

The post-deployment ECO capability allows for bug fixes in silicon even after systems are in volume production. This Application Note provides designers with an overview of how to take advantage of the In-System ECO capability in the latest generation of Virtex-4 EasyPath FPGAs.

EasyPath FPGAs leverage the inherent redundancy of FPGA devices and use a patented testing methodology to lower costs and provide flexibility beyond what Structured ASICs can provide.

EasyPath customer-specific FPGAs use the same silicon as a standard FPGA. The key difference between standard and EasyPath FPGAs is that EasyPath FPGAs are tested for a specific customer design, or if needed, two specific customer designs. By testing to a specific design, EasyPath FPGAs provide up to an 80% reduction in unit price as compared to the equivalent standard FPGAs, while at the same time preserving some, but not all of the flexibility of a traditional FPGA.

Generally, designers move to EasyPath FPGAs once their design is frozen and they are ready to move to high-volume production. The In-System ECO enables modifications to be made to the combinatorial logic in an EasyPath FPGA (contained in Look-Up-Tables or LUTs) and IOB (I/O Block) parameters even after volume shipments have begun and devices are deployed in end customer systems. As part of the standard EasyPath design flow, designers submit their design files (NCD, PCF, TWR, BGN and BIT file), which are used to generate design-specific test patterns. The Xilinx FPGA Editor tool allows original netlist (NCD), used to generate the original EasyPath BIT file submitted to Xilinx, to be graphically viewed and modified. In-System ECOs allow users to take advantage of the following flexibility features:

- Changing the configuration of a LUT inside of a slice
- Modifying the IOB drive strength
- Modifying the IOB slew rate

Note that modifications that change the placement or routing of the original design are not currently supported by the In-System ECO capability. Also, note that changes can only be made to LUTs and I/Os that were used in the original EasyPath FPGA. New LUTs or I/Os cannot be added to an EasyPath FPGA using the In-System ECO capability. To add new LUTs or I/Os, a new EasyPath FPGA design must be created. This Application Note describes how to make changes to an EasyPath FPGA without modifying the design's placement or routing by using the FPGA Editor software tool. Changes made in the FPGA Editor are made directly to the NCD file. Synthesis does not to be rerun nor does the netlist need to be re-implemented; however, the BitGen tool must be run on the modified NCD file to generate an updated BIT file.

Main FPGA Editor Windows

The FPGA Editor Main window is shown in Figure 1, page 3. The List window allows the user to view, search for, and select nets, components, bels, macros, and constraints in the design. The name filter allows the use of wildcards to search for elements.

The Array window displays a graphical representation of the FPGA device. The device components and the interconnections (both logical and routed) between these components are displayed in this window.

When editing the internal logic of a slice or IOB, a schematic of the interior of the component is displayed in a separate Block window.

Changing Internal Component Configurations

Double-click a component to enter the Block window. To edit the configuration of a component, use the Begin Editing button near the left side of the buttons on the top of the Block window (the editing mode must also be set to read/write). When exiting, save the changes. Select the **Save Changes** and **Close Window** or **Apply** button in the Block window to save the changes.

Changing a LUT Equation

The configuration equation of a LUT in the FPGA Editor can be modified without having to rerun synthesis and implementation. Follow the steps below to ensure that no placement or routing changes are made. Use Table 1 for reference when modifying LUT logic.

Table 1: **Boolean Representation of the Logic for LUT**

Symbol	Logic Gate
~	NOT
+	OR
*	AND
@	XOR

Starting the FPGA Editor

1. To start the FPGA Editor, use one of the following methods:
   - Enter the following on the command line:

     ```
     fpga_editor
     ```

   - Click the Windows Start button and select **Programs** →**Xilinx ISE** →**Accessories** → **FPGA_Editor**.
2. Open the post place-and-route NCD file by selecting **File** →**Open** or by clicking the **Open** icon shown below.

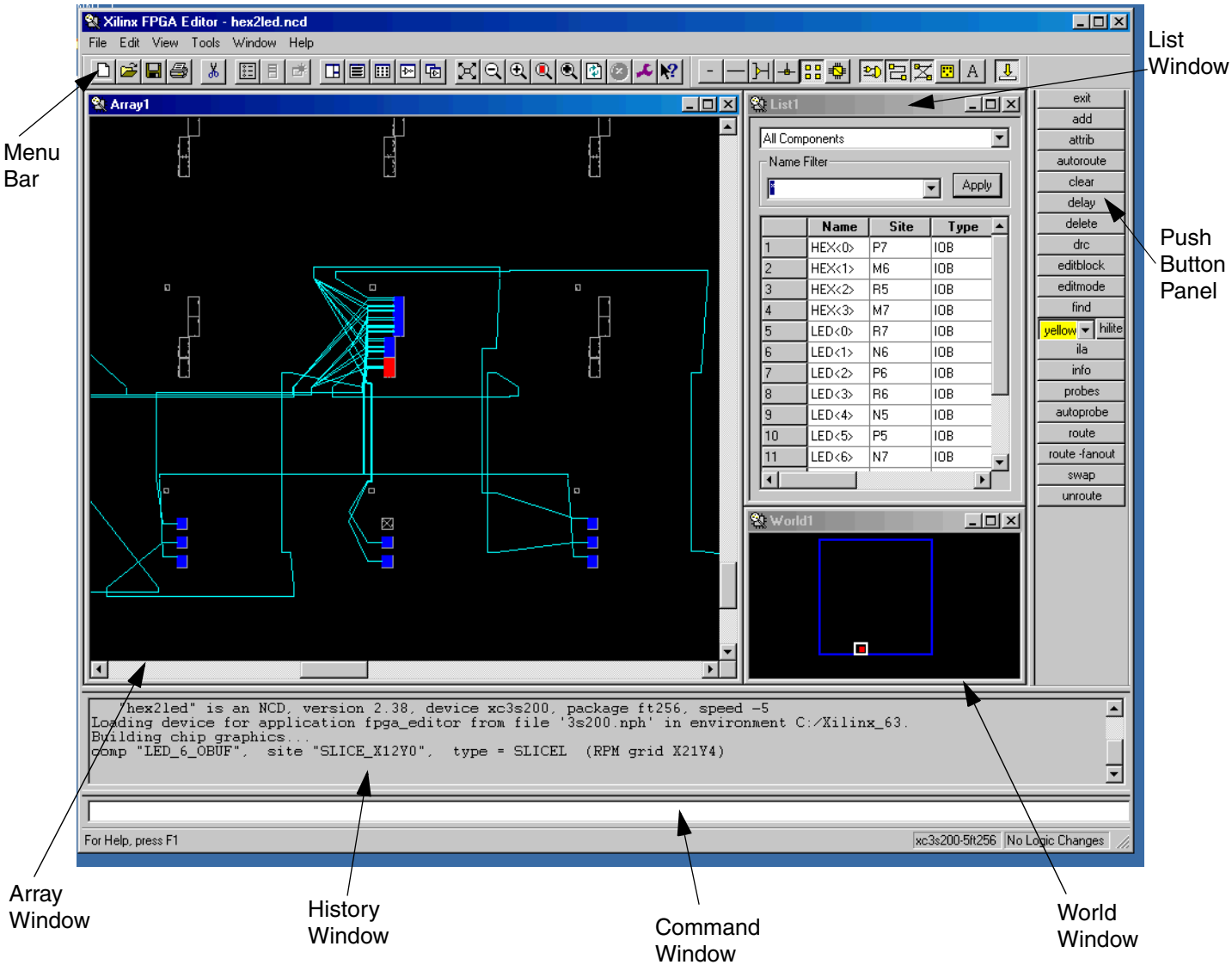

Figure 1: **FPGA Editor Main Window**

3. Set Edit Mode to Read Write and then select **OK**. It is not necessary to specify the Physical Constraints File.
4. Select **File** →**Save As**. In the Design File text box enter *new_design_name*.ncd and select **OK**. Renaming the NCD file ensures that the original design file is not overwritten.
5. Select **File** →**Main Properties** →**Global Physical Constraints** tab. Check the Lock Routing check box and select **OK**. This disables any placement or routing changes.
6. In the List window, change the list display so that it displays **All Components**. Select the component that contains the LUT to be modified. Click the **Zoom Selection** icon from the menu bar to zoom to the component site.

7. Double-click on the site to display the Block window, as shown in Figure 2, page 4.

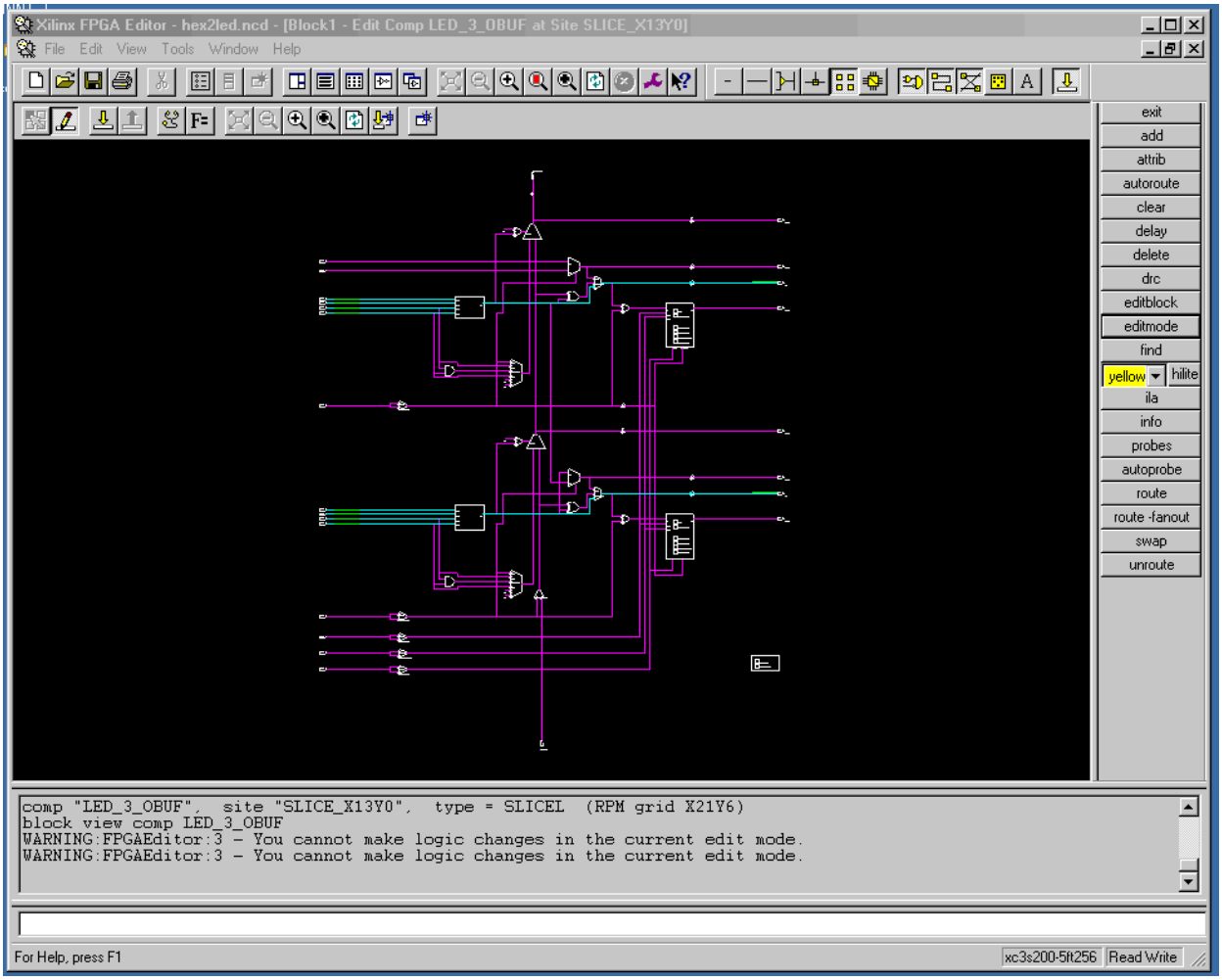

Figure 2: **Block Window Slice View**

8. Click on the **Begin Editing** icon on the top of the Block window to starting modification. After enabling component editing, the background of the Component window changes from gray to black.

9. Click on the **Show/Hide Attribute** icon in the Block window to bring up the equations and attributes section in the Block window.

10. Now change the Feqn and Geqn for the two LUTs in the slice. When the mouse is held over a LUT, a text box appears to indicate the F LUT or the G LUT. Figure 3, page 5 shows the Block window after the **Show/Hide Attribute** icon is selected.
11. Click on the **Apply** icon to apply the modifications.

12. Select **File** →**Save** to save the design to the new NCD file name and exit the FPGA Editor. Run **BitGen** to generate a new BIT file to download to the device.

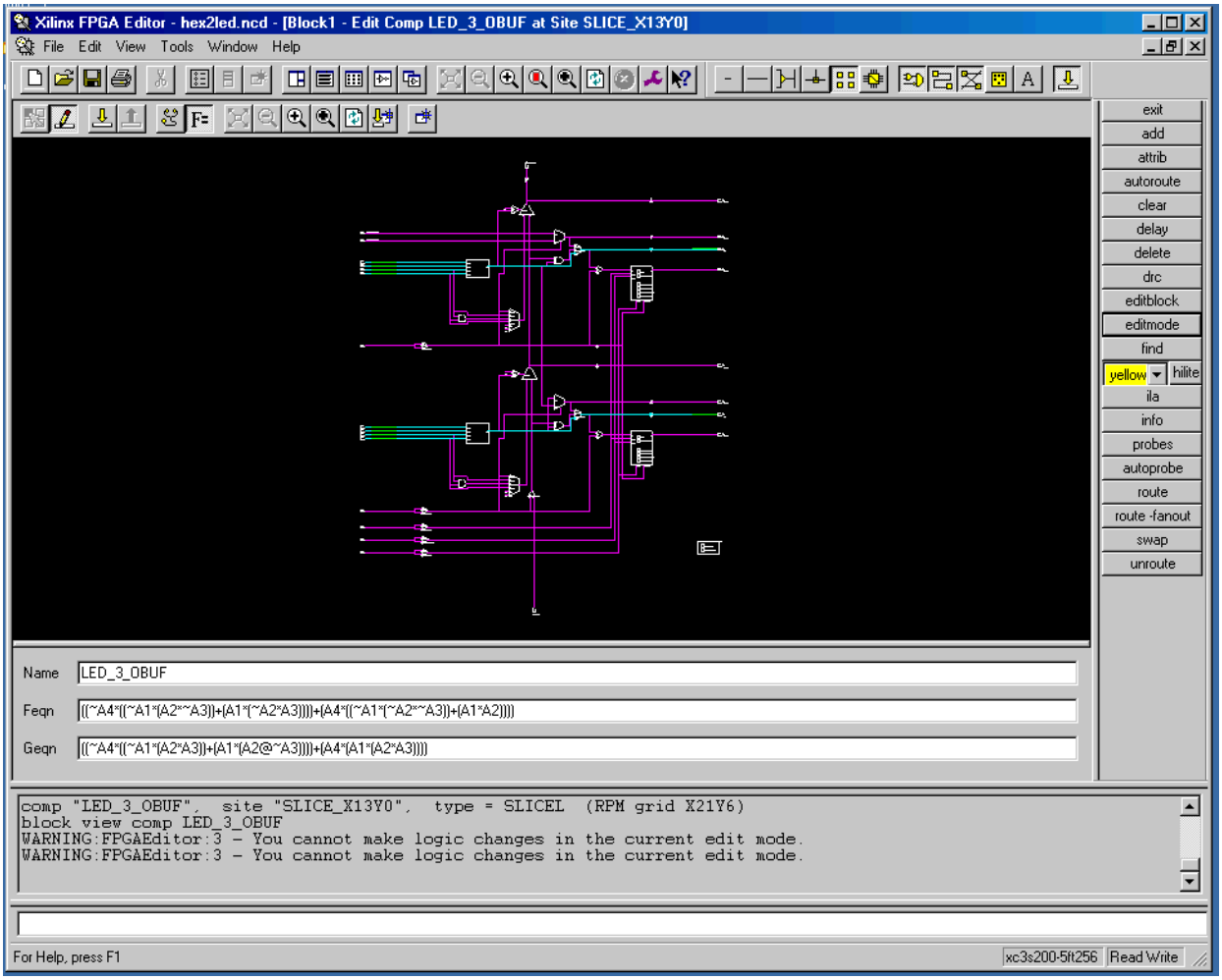

Figure 3: **Block Window View with Show/Hide Selected**

Changing IOB Drive Strength and Slew Rate

1. To start the FPGA Editor, use one of the following methods:
   - Enter the following on the command line:

     `fpga_editor`
   - Click the Windows **Start** button and select **Programs** →**Xilinx ISE** →**Accessories** → **FPGA_Editor**.
2. Open the post Place and Route NCD file by selecting **File** →**Open** or by clicking the **Open** icon. Set Edit Mode to Read Write. It is not necessary to specify the Physical Constraints File.
3. Select **File** →**Save As**. In the Design File text box, enter *new_design_name*.ncd and select **OK**. Renaming the NCD file ensures that the original design file is not overwritten.
4. Select **File** →**Main Properties** →**Global Physical Constraints** Tab. Check the Lock Routing check box and select **OK**. This disables any placement or routing changes.
5. In the List window, change the list display so that it displays All Components. Select the IOB to be modified. Click on the **Zoom Selection** icon from the menu bar to zoom to the component site.
6. Double-click on the site to display the Block window, as shown in the Figure 4, page 6.
7. Click on the **Begin Editing** icon at the top of the Block window to start editing. After enabling component editing, the background of the component window changes from gray to black.

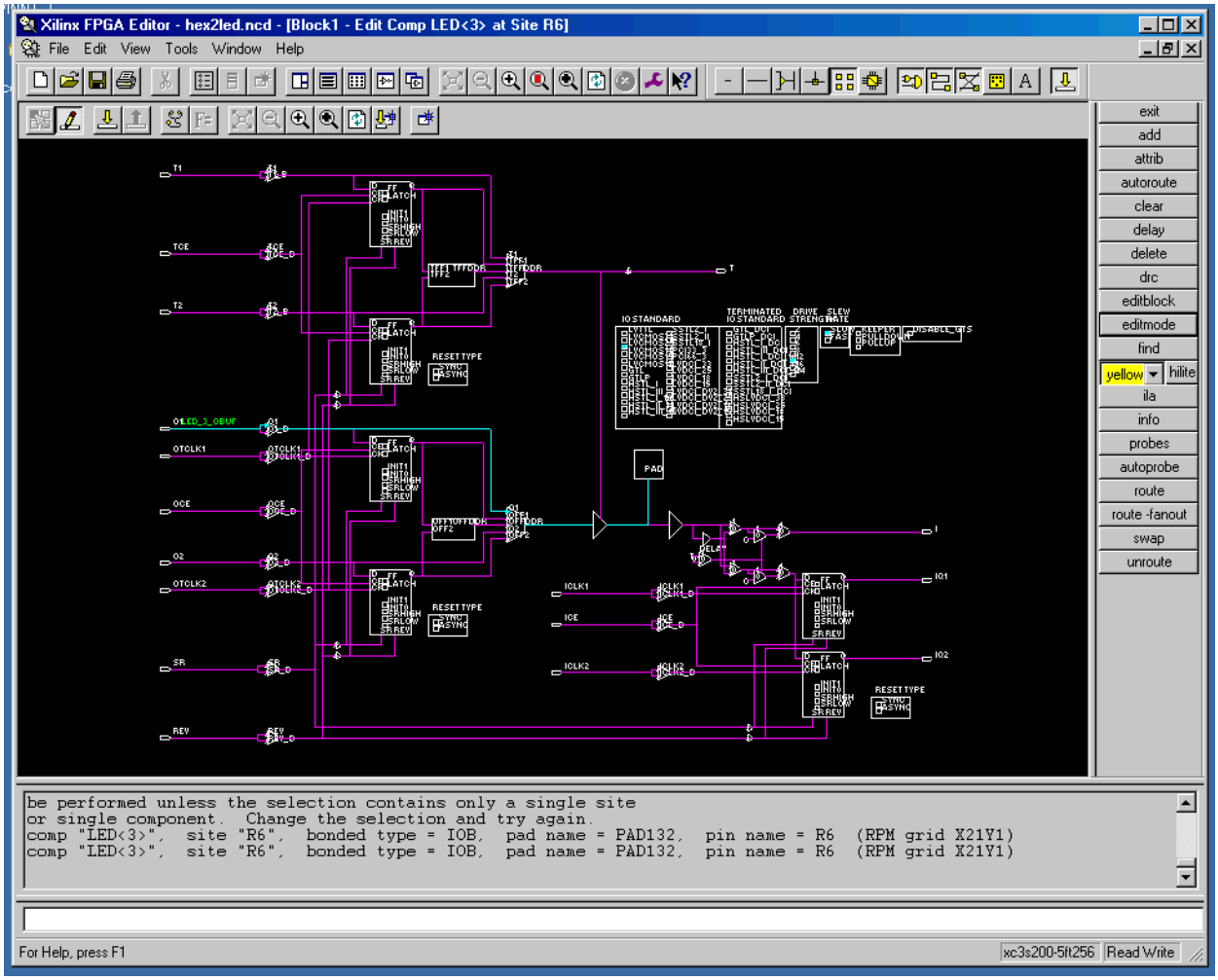

Figure 4: **Block Window IOB View**

8. To change the drive strength or slew rate for the I/O, click in the appropriate square in the Drive Strength or Slew Rate box, as shown in Figure 5.

Figure 5: **Drive Strength and Slew Rate Boxes from IOB Block**

9. Click on the **Apply** icon to apply the modifications.
10. Select **File** →**Save** to save the design to the new NCD file name, and exit the FPGA Editor.
11. Run **BitGen** to generate a new BIT file to download to the device.

Running BitGen

1. **BitGen** can be run from the command line. Previous **BitGen** command line options used can be found in the **BitGen** report file, *design_name*.bgn file, in the project directory.

   Note: It is important to run BitGen with the exact same options that used when creating the original NCD file.

2. The *design_name*.ncd file must be changed to *new_design_name*.ncd in the command line options.

   Note: It is important that only the allowed changes, as described in this document, are made to the design. Occasionally, Xilinx may ask for the new BIT file to be submitted to the EasyPath contact to verify that changes were only made to the LUT equation, IOB Drive Strength, or IOB Slew Rate.

Conclusion

With the introduction of Virtex-4 EasyPath FPGAs, prototyping can be done with standard FPGAs and then moved to the corresponding lower-cost EasyPath FPGA in a seamless fashion. The unique In-System ECO capability in EasyPath FPGAs allows changes in logic and I/Os to be made even after the devices have been deployed in the field in high volume. The FPGA Editor tool provides a simple way for making these changes in the unlikely event that a bug is discovered in the design after volume deployment. Together with the multiple bitstream option, EasyPath FPGAs are the only flexible, high-volume solutions available at prices below those of Structured ASICs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/21/05	1.0	Initial Xilinx release.
07/18/06	1.1	Removed all references to Spartan™-3 FPGAs