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# MMCM and PLL Dynamic Reconfiguration

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## Summary

This application note provides a method to dynamically change the clock output frequency, phase shift, and duty cycle of the mixed-mode clock manager (MMCM) for the Xilinx® 7 series, UltraScale™, and UltraScale+™ FPGAs. Similarly, the phase-locked loop (PLL) can be changed through the dynamic reconfiguration port (DRP). An explanation of the behavior of the internal DRP control registers is accompanied by a reference design that uses a state machine to drive the DRP, which ensures the registers are controlled in the correct sequence.

While the reference design performs the operations for the user, familiarity with the functional operation of the MMCM is recommended. For more information on MMCM and PLL functionality, see the *7 Series FPGA Clocking Resources User Guide* ([UG472](#)) and the *UltraScale Architecture Clocking Resources User Guide* ([UG572](#)).

The reference design supports two reconfiguration state addresses and can be extended to support additional states. Each state does a full reconfiguration of the MMCM or PLL so that most parameters can be changed. The design does not support outputs configured with fine-phase shifting enabled.

You can download the [reference design files](#) for this application note from the Xilinx website. For detailed information about the design files, see [Reference Design](#).

## Introduction

This application note describes the information necessary to reconfigure the MMCM or PLL and provides a reference design that implements all of the algorithms covered. The PLL and MMCM share very similar functionality but are not identical. Due to some subtle functionality differences and the requirement for different settings, a separate PLL reference design is provided. To ensure correct operation, use the correct reference design for the clock management tile (CMT) being reconfigured. Furthermore, there are differences in attributes and frequency specifications for the various families. Consult the appropriate user guide and data sheet for the selected device family.

Reconfiguration is performed through the DRP. The DRP provides access to the configuration bits that would normally only be initialized in the bitstream. This allows the user to dynamically change the MMCM or PLL clock outputs without loading a new bitstream. The MMCM or PLL must be held in reset during dynamic reconfiguration or must be reset after the dynamic reconfiguration changes have completed. Frequency, phase, and duty cycle can all be changed

through the DRP port. Fine-phase shifting is not allowed for the initial configuration or during reconfiguration.

The [MMCM and PLL Configuration Bit Groups](#) section presents the configuration bits as five bit groups, and provides an overview of their usage. The [DRP Registers](#) section details the configuration bit locations as registers. This information is not necessary to use the DRP reference design; it is intended to give an overview of the internal MMCM attributes that must be changed along with their register locations. Specific information on how the attributes are calculated is provided through the reference design. The reference design functionality and use are explained in the [Reference Design](#) and [Using the Reference Design](#) sections.

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## MMCM and PLL Configuration Bit Groups

The MMCM has six user-accessible configuration bit groups that allow reconfiguration of individual clock outputs. The six groups are the divider group, the phase group, the fractional group, the lock group, the filter group, and the power group. These configuration bit groups are internal to the MMCM primitive and clarify the operation of the MMCM\_DRP reference design module. The user modifiable parameters for the MMCM\_DRP module are described in the [Reconfiguration Module Ports and Attributes](#) section.

### Divider Group

Every clock output has a divider group associated with it. The divider group is composed of the following parameters:

- High Time
- Low Time
- No Count
- Edge

The first two parameters associated with the divider group are the High and Low Time counters. These counters set the number of voltage-controlled oscillator (VCO) clock cycles through which the output clock should stay High or Low. For example, if you set both High and Low Time to 2, the effective divide value is 4 and the duty cycle is 50%.

The No Count parameter disables the High and Low Time counters. This in turn makes the divider output a clock with an effective divide value of 1.

The Edge parameter controls the High to Low transition. It forces the High Time counter to transition on a falling edge at the end of its count. This has the effect of increasing the High Time while decreasing the Low Time. Another way to think of the edge bit is that it adds half a VCO clock cycle to the High Time and subtracts half a clock cycle from the Low Time.

As an example, if a 50/50 duty cycle is desired with a divide value of 3, the Edge bit would be set. The High Time counter would be set to one and the Low Time counter would be set to 2. With the edge bit set, the net count for the High and Low times would be 1.5 clock cycles each.

## Phase Group

Each clock output except the DIVCLK has a phase group associated with it. This group is composed of the following set of parameters:

- Phase MUX
- Delay Time
- MX

The Phase MUX selects a coarse phase from the VCO for a clock output with a resolution of  $45^\circ$  ( $360^\circ/8$ ) relative to the VCO clock period.

Delay Time is a counter that counts the number of VCO clock cycles to delay the output. This means that there is a direct correlation between the possible phase shift for the clock output and the divide value for that particular output. As the divide value increases, finer phase shift steps are available. The Delay Time counter allows for a phase offset of up to 64 VCO clock cycles.

MX must be set to `2'b00` during reconfiguration, regardless of the previous value. This parameter ensures the desired phase is output as expected.

## Fractional Group

The MMCM supports fractional (non-integer) values for the CLKOUT0 and CLKFBOUT counters. When using fractional values, CLKOUT0 and CLKFBOUT add the following parameters:

- FRAC\_EN (For fractional values of CLKOUT0 or CLKFBOUT)
- FRAC (For fractional values of CLKOUT0 or CLKFBOUT)
- PHASE\_MUX\_F (For fractional values of CLKOUT0 or CLKFBOUT)
- FRAC\_WF\_R (For fractional values of CLKOUT0 or CLKFBOUT)
- FRAC\_WF\_F (For fractional values of CLKOUT0 or CLKFBOUT)

FRAC\_EN enables the fractional circuitry. When enabling the fractional counters, parameters for the divider group and phase group must be recalculated.

The FRAC parameter represents the fractional divide portion of the divider in 0.125 increments. For example  $FRAC(4) = 0.500$ .

PHASE\_MUX\_F is the coarse phase for the falling edge with a resolution of  $45^\circ$  relative to the VCO clock period. PHASE\_MUX\_F is additionally used with the Low Time and High Time parameters to adjust the duty cycle. For odd fractional divide values (e.g., 0.125 or 0.375), an exact 50% duty cycle is not possible, resulting in a duty cycle that is off by  $1/8$  VCO period.

FRAC\_WF\_R and FRAC\_WF\_F adjust internal MMCM timings required for fractional values.

The PHASE\_MUX\_F and FRAC\_WF\_F parameters for CLKOUT0 are located in ClkReg2 for CLKOUT5 (see [Table 5](#)). The fractional settings for CLKOUT0 do not affect CLKOUT5. Similarly,

the PHASE\_MUX\_F and FRAC\_WF\_F parameters for CLKFBOUT do not affect CLKOUT6 (see [Table 6](#)).

## Lock Group

This group cannot be calculated with an algorithm and is based on lookup tables created from device characterization. The appropriate lock bit settings are dependent on the feedback divider setting. This divider is set with the CLKFBOUT\_MULT attribute when instantiating the MMCM\_DRP module. The lock group has an effect on the MMCM's ability to detect that it is locked. The lookup table is located in the reference design within `mmcm_drp_func.h`.

## Filter Group

This group cannot be calculated and is based on lookup tables created from device characterization. There are effectively two tables, one for each bandwidth setting. The feedback divider setting (CLKFBOUT\_MULT) acts as the index to the chosen table. There are three bandwidth settings allowable in the tools (High, Low, and Optimized), but in effect there are only two. High and Optimized use the same table, while the Low bandwidth setting uses a separate table. The filter group has an effect on the phase skew and the jitter filtering capability of the MMCM. The lookup table is located in the reference design within `mmcm_drp_func.h`.

## Power Group

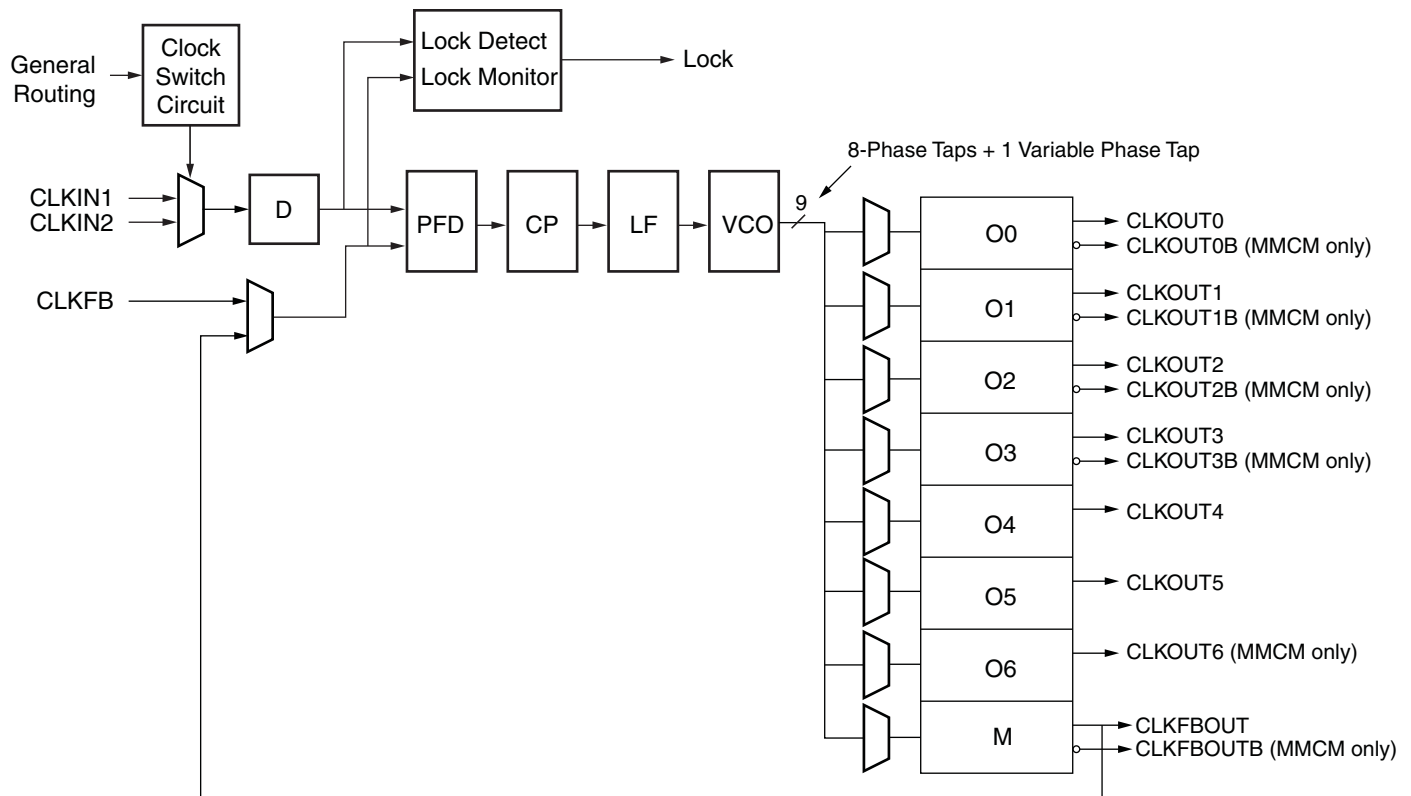
This group allows the dynamic reconfiguration operations to properly function. The bits associated with this group must be all enabled when performing reconfiguration.

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## DRP Registers

For the MMCM seventeen configuration registers store the divide and phase bit groups. For each of the eight clock outputs (CLKOUT[6:0] and CLKFBOUT) there are two configuration registers for a total of sixteen. These 16 registers represent the O[6:0] and M in [Figure 1](#). One additional register is associated with DIVCLK\_DIVIDE, which is along the input path to the MMCM. DIVCLK\_DIVIDE is shown in [Figure 1](#) as D.

The PLL is organized similar to the MMCM with exceptions noted in the [Figure 1](#) block diagram and in the subsequent tables.



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Figure 1: MMCM and PLL Block Diagram

The sixteen registers that have the same layout are divided into two registers CLKREG1 and CLKREG2. The register layout for CLKREG1 and CLKREG2 are shown in [Table 1](#) through [Table 7](#). The register layouts are shown in [Table 1](#) through [Table 14](#).

Table 1: ClkReg1 Bitmap for CLKOUT[6:0] and CLKFBOUT

ClkReg1	7 Series Bit	UltraScale Bit	Description
PHASE MUX	[15:13]	[15:13]	Chooses an initial phase offset for the clock output, the resolution is equal to 1/8 VCO period. Not available in UltraScale PLLE3 and UltraScale+ PLLE4.
RESERVED	[12]	[12]	Retain the previous value stored here.
HIGH TIME	[11:6]	[11:6]	Sets the amount of time in VCO cycles that the clock output remains High.
LOW TIME	[5:0]	[5:0]	Sets the amount of time in VCO cycles that the clock output remains Low.

Table 2: ClkReg2 Bitmap for CLKOUT[0]

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15]	[15]	Reserved.
FRAC	[14:12]	[14:12]	Fractional divide counter setting for CLKOUT0. Equivalent to additional divide of 1/8.
FRAC_EN	[11]	[11]	Enable fractional divider circuitry for CLKOUT0.
FRAC_WF_R	[10]	[10]	Adjusts CLKOUT0 rising edge for improved duty cycle accuracy when using fractional counter.
MX	[9:8]	[9:8]	Must be set to 2'b00.
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

Table 3: ClkReg2 Bitmap for CLKOUT[1]

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:10]	[15]	Retain the previous value stored here.
CLKOUTPHY_MODE		[14:13]	For the PLLE3 and PLLE4, determines CLKPHYOUT frequency based on the VCO frequency.
RESERVED		[12:11]	Retain the previous value stored here.
RESERVED		[10]	Reserved for CDDC.
MX	[9:8]	[9:8]	Must be set to 2'b00.
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

Table 4: ClkReg2 Bitmap for CLKOUT[4:2]

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:10]	[15:11]	Retain the previous value stored here.
RESERVED		[10]	Reserved for CDDC.
MX	[9:8]	[9:8]	Must be set to 2'b00
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

Table 5: ClkReg2 Bitmap for CLKOUT[5] and CLKOUT[0] (Fractional)

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:14]		Retain the previous value stored here.
PHASE_MUX_F_CLKOUT0	[13:11]	[15:13]	CLKOUT0 data required when using fractional counter. Chooses an initial phase offset for the falling edge of the clock output. The resolution is equal to 1/8 VCO period. Not available in UltraScale PLLE3 and UltraScale+ PLLE4.
FRAC_WF_F_CLKOUT0	[10]	[12]	Adjusts CLKOUT0 falling edge for improved duty cycle accuracy when using fractional counter.
RESERVED		[11]	Retain the previous value stored here.
RESERVED		[10]	Reserved for CDDC.
MX	[9:8]	[9:8]	Must be set to 2'b00.
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

Table 6: ClkReg2 Bitmap for CLKOUT[6] and CLKFBOUT (Fractional)

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:14]		Retain the previous value stored here.
PHASE_MUX_F_CLKFB	[13:11]	[15:13]	CLKFBOUT data required when using fractional counter. Chooses an initial phase offset for the falling edge of the clock output. The resolution is equal to 1/8 VCO period.
FRAC_WF_F_CLKFB	[10]	[12]	Adjusts CLKFBOUT falling edge for improved duty cycle accuracy when using fractional counter.
RESERVED		[11]	Retain the previous value stored here.
RESERVED		[10]	Reserved for CDDC.
MX	[9:8]	[9:8]	Must be set to 2'b00.
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

Table 7: ClkReg2 Bitmap for CLKFBOUT

ClkReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15]	[15]	Retain the previous value stored here.
FRAC	[14:12]	[14:12]	Fractional divide counter setting for CLKFBOUT. Equivalent to additional divide of 1/8.
FRAC_EN	[11]	[11]	Enable fractional divider circuitry for CLKFBOUT.
FRAC_WF_R	[10]	[10]	Adjusts CLKFBOUT rising edge for improved duty cycle accuracy when using fractional counter.

Table 7: ClkReg2 Bitmap for CLKFBOUT (Cont'd)

ClkReg2	7 Series Bit	UltraScale Bit	Description
MX	[9:8]	[9:8]	Must be set to 2'b00.
EDGE	[7]	[7]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[6]	[6]	Bypasses the High and Low Time counters.
DELAY TIME	[5:0]	[5:0]	Phase offset with a resolution equal to the VCO period.

The register bitmap associated with the input divider D is shown in Table 8. Only a single register is needed because there is no phase adjustment on the input divider.

Table 8: DivReg Bitmap

DivReg	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:14]	[15:14]	Retain the previous value stored here.
EDGE	[13]	[13]	Chooses the edge that the High Time counter transitions on.
NO COUNT	[12]	[12]	Bypasses the High and Low Time counters.
HIGH TIME	[11:6]	[11:6]	Sets the amount of time in VCO cycles that the clock output remains High.
LOW TIME	[5:0]	[5:0]	Sets the amount of time in VCO cycles that the clock output remains Low.

Three additional LOCK configuration registers must also be updated based on how the MMCM is programmed. These values are automatically setup by the reference design.

Table 9: LockReg1 Bitmap

LockReg1	7 Series Bit	UltraScale Bit	Description
RESERVED	[15:10]	[15:10]	Retain the previous value stored here.
LKTABLE[29:20]	[9:0]	[9:0]	These bits are pulled from the lookup table provided in the reference design.

Table 10: LockReg2 Bitmap

LockReg2	7 Series Bit	UltraScale Bit	Description
RESERVED	[15]	[15]	Retain the previous value stored here.
LKTABLE[34:30]	[14:10]	[14:10]	These bits are pulled from the lookup table provided in the reference design.
LKTABLE[9:0]	[9:0]	[9:0]	These bits are pulled from the lookup table provided in the reference design.

Table 11: LockReg3 Bitmap

LockReg3	7 Series Bit	UltraScale Bit	Description
RESERVED	[15]	[15]	Retain the previous value stored here.
LKTABLE[39:35]	[14:10]	[14:10]	These bits are pulled from the lookup table provided in the reference design.
LKTABLE[19:10]	[9:0]	[9:0]	These bits are pulled from the lookup table provided in the reference design.



The filter group is composed of 10 bits that are stored on two registers. The register layouts are shown in [Table 12](#) and [Table 13](#).

**Table 12: FiltReg1 Bitmap**

<b>FiltReg1</b>	<b>7 Series Bit</b>	<b>UltraScale Bit</b>	<b>Description</b>
TABLE[9]	[15]	[15]	This bit is pulled from the lookup table provided in the reference design.
RESERVED	[14:13]	[14:13]	Retain the previous value stored here.
TABLE[8:7]	[12:11]	[12:11]	These bits are pulled from the lookup table provided in the reference design.
RESERVED	[10:9]	[10:9]	Retain the previous value stored here.
TABLE[6]	[8]	[8]	This bit is pulled from the lookup table provided in the reference design.
RESERVED	[7:0]	[7:0]	Retain the previous value stored here.

**Table 13: FiltReg2 Bitmap**

<b>FiltReg2</b>	<b>7 Series Bit</b>	<b>UltraScale Bit</b>	<b>Description</b>
TABLE[5]	[15]	[15]	This bit is pulled from the lookup table provided in the reference design.
RESERVED	[14:13]	[14:13]	Retain the previous value stored here.
TABLE[4:3]	[12:11]	[12:11]	These bits are pulled from the lookup table provided in the reference design.
RESERVED	[10:9]	[10:9]	Retain the previous value stored here.
TABLE[2:1]	[8:7]	[8:7]	These bits are pulled from the lookup table provided in the reference design.
RESERVED	[6:5]	[6:5]	Retain the previous value stored here.
TABLE[0]	[4]	[4]	This bit is pulled from the lookup table provided in the reference design.
RESERVED	[3:0]	[3:0]	Retain the previous value stored here.

The power bits are stored in one register whose layout is shown in [Table 14](#).

**Table 14: PowerReg Bitmap**

<b>PowerReg</b>	<b>7 Series Bit</b>	<b>UltraScale Bit</b>	<b>Description</b>
POWER	[15:0]	[15:0]	These bits must all be set High when performing DRP.

The DRP register addresses are shown in [Table 15](#).

**Table 15: DRP Address Map**

<b>Address</b>	<b>Layout</b>	<b>Description</b>
0x06	ClkReg1	CLKOUT5 Register 1
0x07	ClkReg2	CLKOUT5 Register 2
0x08	ClkReg1	CLKOUT0 Register 1
0x09	ClkReg2	CLKOUT0 Register 2

Table 15: **DRP Address Map (Cont'd)**

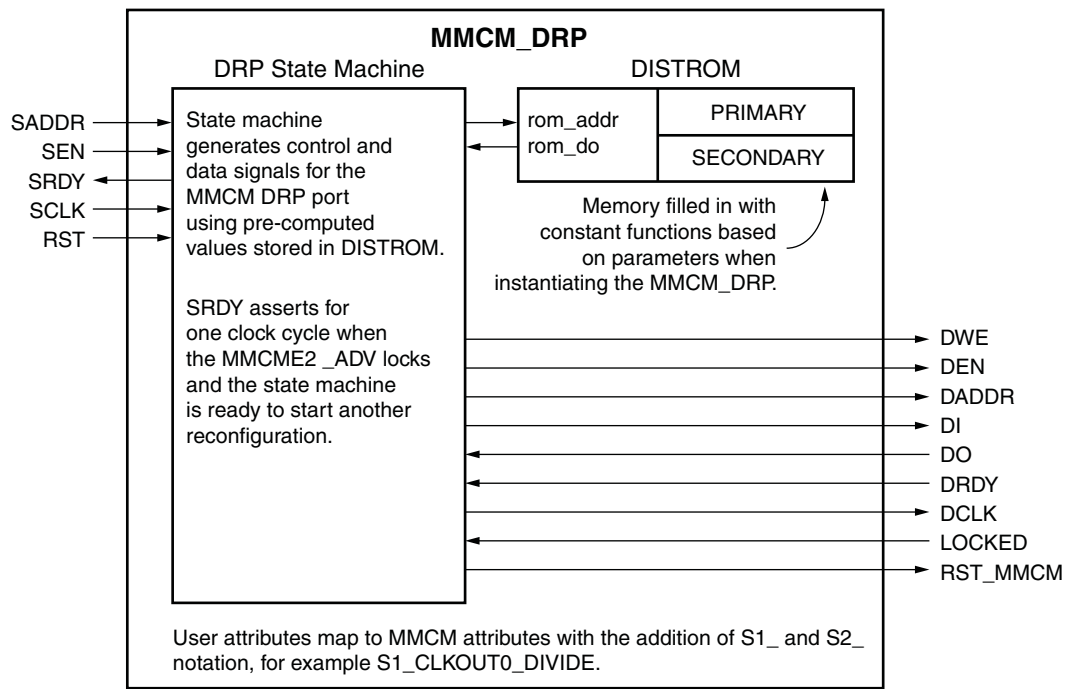
Address	Layout	Description
0x0A	ClkReg1	CLKOUT1 Register 1
0x0B	ClkReg2	CLKOUT1 Register 2
0x0C	ClkReg1	CLKOUT2 Register 1 (Not available for PLLE3 or PLLE4)
0x0D	ClkReg2	CLKOUT2 Register 2 (Not available for PLLE3 or PLLE4)
0x0E	ClkReg1	CLKOUT3 Register 1 (Not available for PLLE3 or PLLE4)
0x0F	ClkReg2	CLKOUT3 Register 2 (Not available for PLLE3 or PLLE4)
0x10	ClkReg1	CLKOUT4 Register 1 (Not available for PLLE3 or PLLE4)
0x11	ClkReg2	CLKOUT4 Register 2 (Not available for PLLE3 or PLLE4)
0x12	ClkReg1	CLKOUT6 Register 1 (Not available for PLLE2, PLLE3, or PLLE4)
0x13	ClkReg2	CLKOUT6 Register 2 (Not available for PLLE2, PLLE3, or PLLE4)
0x14	ClkReg1	CLKFBOUT Register 1
0x15	ClkReg2	CLKFBOUT Register 2
0x16	DivReg	DIVCLK Register
0x18	LockReg1	Lock Register 1
0x19	LockReg2	Lock Register 2
0x1A	LockReg3	Lock Register 3
0x27	PowerReg	Power Register (UltraScale and UltraScale+)
0x28	PowerReg	Power Register (7 series)
0x4E	FiltReg1	Filter Register 1
0x4F	FiltReg2	Filter Register 2

## Reference Design

The reference design files include a Verilog MMCM and PLL reconfiguration module. This module uses only a small number of slices, comprising the reconfiguration logic and state memory.

The reference design drives the DRP port with a state machine that addresses the MMCM, reads the previous value, masks the bits that need to be changed, sets the new value, and finally writes the value to the MMCM DRP port. The addresses, masks, and new values are stored in a pre-initialized ROM that is filled during elaboration in synthesis. The ROM initialization is done with constant functions provided with the reference design.

Figure 2 is a block diagram of the reconfiguration module.

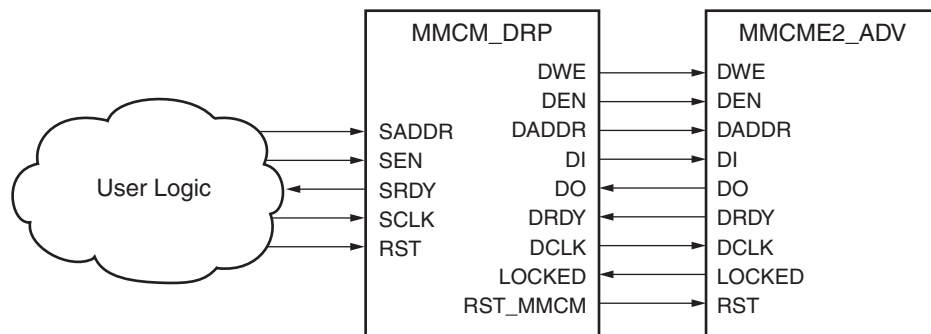


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Figure 2: MMCM\_DRP Internal Block Diagram

The `mmcm_drp.v` module contains the state machine and ROM, and calls the constant functions which are provided in `mmcm_drp_func.h`.

Figure 3 shows an example of a block diagram of the system with the `mmcme2_adv` primitive and the `mmcm_drp` modules attached.



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Figure 3: Reference Design Block Diagram

## DRP State Machine

The DRP state machine is composed of the nine states shown in [Table 16](#). It controls all of the signals from the `mmcm_drp` module.

Table 16: DRP States

State	Description	Next State	Transition Condition
RESTART	This state is entered whenever the SRST pin is asserted or if the current_state goes into an undefined state.	WAIT_LOCK	SRST = 0
WAIT_LOCK	This state waits for the lock signal from the MMCM to assert. When lock is asserted, SRDY = 1.	WAIT_SEN	LOCK = 1
WAIT_SEN	This state waits for SEN to be asserted and sets the appropriate ROM address according to SADDR.	ADDRESS	SEN = 1
ADDRESS	This state is entered from either WAIT_SEN or from WAIT_DRDY. The state sets DADDR according to the current value stored in the ROM and asserts DEN.	WAIT_A_DRDY	<always>
WAIT_A_DRDY	This state is always entered from ADDRESS. It waits for the MMCM to assert the DRDY signal.	BITMASK	DRDY = 1
BITMASK	This state is entered from WAIT_A_DRDY. It performs a bitwise AND on DO from the MMCM with the mask value stored in the ROM.	BITSET	<always>
BITSET	This state is always entered from BITMASK. It performs a bitwise OR with the bitset stored in the ROM and the output from the BITMASK operation.	WRITE	<always>
WRITE	This state asserts DEN, DWE, and RST_MMCM. It updates the state counter which is used to keep track of the number of register writes needed to perform one full reconfiguration.	WAIT_DRDY	<always>
WAIT_DRDY	This state waits for DRDY to assert from the MMCM.	ADDRESS (state_count > 0) WAIT_LOCK (state_count ≤ 0)	DRDY = 1

The operations that must be implemented to reconfigure one value in the MMCM are:

- Assert RST to the MMCM (do not deassert)
- Set DADDR on the MMCM and assert DEN for one clock cycle
- Wait for the DRDY signal to assert from the MMCM
- Perform a bitwise AND between the DO port and the MASK (DI = DO and MASK)
- Perform a bitwise OR between the DI signal and the BITSET (DI = DI | BITSET)

- Assert DEN and DWE on the MMCM for one clock cycle
- Wait for the DRDY signal to assert from the MMCM
- Deassert RST to the MMCM
- Wait for MMCM to lock

## Reconfiguration Module Ports and Attributes

The reconfiguration module is composed of the ports shown in [Table 17](#).

*Table 17: Dynamic Reconfiguration Ports*

Port	Direction	Description
SADDR	Input	This port chooses the state to reconfigure the MMCM to. A value of 0 corresponds to state 1; a value of 1 corresponds to state 2.
SEN	Input	This port enables the reconfiguration state machine. Reconfiguration is triggered if this port is asserted at a rising SCLK edge.
SCLK	Input	This is the clock for the reconfiguration module. It is passed through to the DCLK output.
RST	Input	This resets the state machine and the downstream MMCM.
SRDY	Output	This port asserts for one clock cycle at the end of a reconfiguration sequence. It is to be used to notify the user that a new reconfiguration can be started.
DO[15:0]	Input	This port should be directly attached to the MMCM DO port. It is used to read register values from the MMCM.
DRDY	Input	This port should be directly attached to the MMCM DRDY port. It is used to notify the reference design when the MMCM is ready to read or write a new value.
LOCKED	Input	This port should be directly attached to the MMCM LOCKED port. It is used to notify the reference design that the MMCM is locked and to then transition from the WAIT_LOCK state.
DWE	Output	This port should be directly attached to the MMCM DWE port. It is used to enable a register write.
DEN	Output	This port should be directly attached to the MMCM DEN port. It is used to initiate a register read or write.
DADDR[6:0]	Output	This port should be directly attached to the MMCM DADDR port. It is used to address a register location for reads or writes.
DI[15:0]	Output	This port should be directly attached to the MMCM DI port. It is used to output a new register value for writes.
DCLK	Output	This port should be directly attached to the MMCM DCLK port. It is used to clock the reconfiguration port on the MMCM. It is the SCLK forwarded out of the MMCM reconfiguration module.
RST_MMCM	Output	This port should be directly attached to the MMCM RST port. It is used to reset the MMCM during a reconfiguration or when the RST input port is asserted.

The reconfiguration module also has the attributes shown in [Table 18](#). The MMCM\_DRP attributes correlate with the standard MMCM primitive attributes with some slight naming differences.

**Table 18: Dynamic Reconfiguration Attributes**

Attribute	Description	Valid Format Values
CLKFBOUT_MULT	This attribute modifies the input clock multiplier to change the VCO output frequency of the MMCM.	Consult the appropriate user guide for the valid integer ranges.
CLKFBOUT_PHASE	Modifies the phase of the input clock. This affects all of the MMCM outputs.	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKFBOUT_FRAC	CLKFBOUT fractional divide value	This can be from 0 to 875. This represents the fractional multiply multiplied by 1000. For example CLKFBOUT_DIVIDE(8) and CLKFBOUT_FRAC(125) results in a fractional multiply of 8.125. Only applies to the MMCMs.
CLKFBOUT_FRAC_EN	CLKFBOUT enable for fractional divide	If 1, the fractional divide algorithm is used to calculate register settings. If 0, default calculation is used and CLKFBOUT_FRAC is ignored.
CLKOUTPHY_MODE	Determines CLKOUTPHY frequency based on the VCO frequency	VCO_2X, VCO, VCO_HALF. Only applies to PLLE3 and PLLE4.
BANDWIDTH	Sets the bandwidth setting of the MMCM.	OPTIMIZED, HIGH, LOW, or POSTCRC. POSTCRC is only available for UltraScale components and when used in combination with a SEM IP core.
DIVCLK_DIVIDE	Sets the divide value for the DIVCLK output.	Consult the appropriate user guide for the valid integer ranges.
CLKOUT0_DIVIDE	CLKOUT0 output divide value.	1–128; Integer values only.
CLKOUT0_PHASE	CLKOUT0 output phase value.	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT0_FRAC	CLKOUT0 fractional divide value	This can be from 0 to 875. This represents the fractional divide multiplied by 1000. For example, CLKOUT0_DIVIDE(8) and CLKOUT0_FRAC(125) result in a fractional divide of 8.125. Only applies to the MMCMs.
CLKOUT0_FRAC_EN	CLKOUT0 enable for fractional divide	If 1, the fractional algorithm is used to calculate register settings. If 0, the default calculation is used and CLKOUT0_FRAC is ignored.
CLKOUT0_DUTY	Changes the CLKOUT0 duty cycle Low time.	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.
CLKOUT1_DIVIDE	CLKOUT1 output divide value.	1–128; Integer values only.

Table 18: Dynamic Reconfiguration Attributes (Cont'd)

Attribute	Description	Valid Format Values
CLKOUT1_PHASE	CLKOUT1 output phase value.	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT1_DUTY	Changes the CLKOUT1 duty cycle Low time.	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.
CLKOUT2_DIVIDE	CLKOUT2 output divide value.	1–128; Integer values only.
CLKOUT2_PHASE	CLKOUT2 output phase value.	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT2_DUTY	Changes the CLKOUT2 duty cycle Low time.	Integer values multiplied by 1,000. For example, a 60/40 duty cycle would be 60,000.
CLKOUT3_DIVIDE	CLKOUT3 output divide value (MMCMs and PLLE2 only).	1–128; Integer values only.
CLKOUT3_PHASE	CLKOUT3 output phase value (MMCMs and PLLE2 only).	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT3_DUTY	Changes the CLKOUT3 duty cycle Low time (MMCMs and PLLE2 only).	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.
CLKOUT4_DIVIDE	CLKOUT4 output divide value (MMCMs and PLLE2 only).	1–128; Integer values only.
CLKOUT4_PHASE	CLKOUT4 output phase value (MMCMs and PLLE2 only).	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT4_DUTY	Changes the CLKOUT4 duty cycle Low time (MMCMs and PLLE2 only).	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.
CLKOUT5_DIVIDE	CLKOUT5 output divide value (MMCMs and PLLE2 only).	1–128; Integer values only.
CLKOUT5_PHASE	CLKOUT5 output phase value (MMCMs and PLLE2 only).	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT5_DUTY	Changes the CLKOUT5 duty cycle Low time (MMCMs and PLLE2 only).	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.
CLKOUT6_DIVIDE	CLKOUT6 output divide value. (MMCM only).	1–128; Integer values only.
CLKOUT6_PHASE	CLKOUT6 output phase value. (MMCM only).	Integer values multiplied by 1,000. For example, a 45° phase shift would be 45,000.
CLKOUT6_DUTY	Changes the CLKOUT6 duty cycle Low time. (MMCM only).	Integer values multiplied by 100,000. For example, a 0.60 duty cycle would be 60,000.

# Using the Reference Design

## Design Functionality

The `mmcm_drp.v` file has been written with two available reconfigurable states. They are denoted with an `S1_` or `S2_` before each of the attributes in [Table 18](#). The parameters within each state can be modified independently. Additional states can be added or register writes removed as covered in the [Design Modification](#) section.

To change between the two states, first wait for `SRDY` to be asserted. When `SRDY` has been asserted, the state machine is ready to begin reconfiguration. The `SADDR` port specifies which state is loaded into the MMCM using the `DRP` port. In an unmodified design, a 0 loads state 1 and a 1 loads state 2. Pulsing `SEN` for one clock cycle triggers the reconfiguration and loads all attributes set in the MMCM `DRP` design. Once the reconfiguration is complete, the `SRDY` port is asserted and the MMCM is in its newly reconfigured state.

## Design Modification

The reference design is intended to be modified to suit the specific needs of a design. The process of doing these changes is left to the user, but there are a couple of common needs that warrant some general instructions on the modification process. It should be noted that the header file `mmcm_drp_func.h` should *not* be changed. The file `mmcm_drp.v` is the primary file where design-specific modifications should be done. To perform design modifications, it is expected that the user has become intimately familiar with the functionality of the reconfiguration interface in `mmcm_drp.v` by reading through the provided source.

The first common situation is to retain the previous `CLKOUT#` configuration for both states. For example, if it is desired to retain the previous configuration of `CLKOUT4`, `mmcm_drp.v` must be modified in two locations.

- The ROM initialization must be modified to remove the two `CLKOUT4` registers. This requires removing the entries that modify the `0x10` and `0x11` registers on the MMCM. When the register entries have been removed, the ROM initialization must be changed so that the initialization addresses are sequential.
- Because two registers have been removed from the ROM initialization, `STATE_COUNT_CONST` must be updated to reflect the two fewer register writes.

A second potential design modification is to add a third state to the reference design. To do this, everything that contains an `S#_` (where `#` is a number) must be replicated to create an `S3_` set of parameters, constant function calls, and ROM initializations. The `SADDR` port must be updated to be a vector allowing the third state to be addressed, and the `WAIT_SEN` state must be updated to include the ability to set the initial ROM reconfiguration address based on `SADDR`.



## Design Verification

The reference design was verified in hardware and with simulation. This ensures that the simulation models and the hardware functionality are equivalent. The verification process chose a number of corner cases for reconfiguration along with some standard configurations to verify that the calculations worked across each scenario. The functions that calculate the various bit settings have also gone through a complete analysis to ensure they match the calculations performed by the Vivado® tools during implementation.

## Conclusion

This application note and reference design provide a complete implementation of the MMCM DRP functionality. Due to its modular nature, the design can be used as a full solution for DRP or can be easily extended to support additional reconfiguration states. The design also consumes a minimal amount of resources.

## Reference Design Additional Information

### Files

The reference design files can be downloaded from:

<https://secure.xilinx.com/webreg/clickthrough.do?cid=179222>

### Characteristics

The reference design characteristics are summarized in [Table 19](#).

*Table 19: Reference Design Matrix*

Parameter	Description
<b>General:</b>	
Developer Name	Jim Tatsukawa
Target devices	7 series, UltraScale, and UltraScale+ devices
Source code provided	Yes
Source code format	Verilog
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator™ software, or 3rd party	No
<b>Simulation:</b>	
Functional simulation performed	Yes

Table 19: Reference Design Matrix (Cont'd)

Parameter	Description
Timing simulation performed	Yes
Testbench used for functional and timing simulations	Yes
Testbench format	Verilog
Simulator software/ version used	Vivado simulator
<b>Implementation:</b>	
Synthesis software tools/version used	Vivado 2014.1–2019.1
Implementation software tools /versions used	Vivado 2014.1–2019.1
Static timing analysis performed	Yes
<b>Hardware Verification:</b>	
Hardware verified	Yes
Hardware platform used for verification	FPGA Characterization Boards

## Device Utilization

The reference design device utilization is summarized in [Table 20](#).

Table 20: Device Utilization for MMCM\_DRP

Parameters	Specification/Details
Device Utilization without Testbench	<a href="#">Note 1</a>
HDL Language Support	Verilog

**Notes:**

1. Consult the Vivado tools utilization report.

## Revision History

The following table shows the revision history for this document:

Date	Version	Revision
01/04/2012	1.0	Initial Xilinx release.
05/22/2012	1.1	Updated reference design file ( <a href="#">Files</a> ).
08/07/2013	1.2	Updated third paragraph of <a href="#">Summary</a> and second paragraph of <a href="#">Introduction</a> . Updated number of user-accessible configuration bit groups and added fractional bit group to <a href="#">MMCM and PLL Configuration Bit Groups</a> . Added <a href="#">Fractional Group</a> . Updated <a href="#">Table 2</a> , and added <a href="#">Table 3</a> through <a href="#">Table 7</a> . In <a href="#">Table 18</a> , updated CLKFBOUT_MULT and DIVCLK_DIVIDE, and added CLKFBOUT_FRAC, CLKFBOUT_FRAC_EN, CLKOUT0_FRAC, and CLKOUT0_FRAC_EN. Updated second bullet in <a href="#">Design Modification</a> . Updated Simulation and Implementation sections of <a href="#">Table 20</a> .

Date	Version	Revision
10/08/2014	1.3	Updated document to add UltraScale device information. Added UltraScale Bit columns to <a href="#">Table 1</a> through <a href="#">Table 14</a> . Split <a href="#">Table 3</a> into <a href="#">Table 3</a> and <a href="#">Table 4</a> . In <a href="#">Table 15</a> , added one UltraScale row and updated description of addresses <code>0x0C</code> to <code>0x13</code> . Added CLKOUTPHY_MODE attribute to <a href="#">Table 17</a> . Removed third paragraph in <a href="#">Design Functionality</a> . Added Vivado software to <a href="#">Design Verification</a> . In <a href="#">Table 19</a> , updated Vivado software version, and removed support for ISE Design Suite and XST. Removed "and Performance" from <a href="#">Device Utilization</a> . In <a href="#">Table 20</a> , updated table title, removed maximum frequency rows, and replaced slices with LUT flip-flop pairs.
07/23/2015	1.4	Added the statement <i>Not available in UltraScale PLLE3</i> to the description column of <a href="#">PHASE MUX</a> in <a href="#">Table 1</a> and <a href="#">PHASE_MUX_F_CLKOUT0</a> in <a href="#">Table 5</a> .
11/12/2015	1.5	Replaced CLKOUT0 with CLKFBOUT in description of <a href="#">FRAC_EN</a> in <a href="#">Table 7</a> .
05/16/2016	1.6	In <a href="#">Table 6</a> , added row for RESERVED[15:14], and updated 7 series bits for <a href="#">PHASE_MUX_F_CLKFB</a> , <a href="#">FRAC_WF_F_CLKFB</a> , and <a href="#">RESERVED</a> .
06/01/2016	1.6.1	Republished to remove extraneous markings.
04/11/2017	1.7	Added UltraScale+ FPGAs and PLLE4 throughout. Updated first two paragraphs of <a href="#">Introduction</a> , first paragraph of <a href="#">Reference Design</a> , and <a href="#">Table 18</a> , <a href="#">Table 19</a> , and <a href="#">Table 20</a> . Updated description of <a href="#">RESERVED</a> bit in <a href="#">Table 2</a> . Removed ISE software from <a href="#">Design Verification</a> . Updated last sentence in <a href="#">Conclusion</a> .
08/20/2019	1.8	In <a href="#">Table 18</a> , added POSTCRC value to <a href="#">BANDWIDTH</a> attribute. In <a href="#">Table 19</a> , updated upper end for synthesis and implementation software version to 2019.1.

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