Switching Power Supplies for Virtex-4 RocketIO MGTs

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Summary

This document presents design techniques and reference circuits that power Virtex™-4 FX RocketIO™ multi-gigabit transceivers (MGTs) operating at data rates below 3.125 Gb/s.

When using multiple transceivers, it is sometimes preferred to power them from a switching power supply. However, switching power supplies generate noise that affects transceiver performance. This application note describes techniques that can be used to avoid power supply-induced performance degradation on RocketIO links. It presents performance data obtained with an ideal power supply, a low-noise switching regulator, and a noisy switching regulator for 2.5 Gb/s and 3.125 Gb/s data rates.

Introduction

Because the RocketIO tranceivers contain analog circuits such as phase-locked loops, bias generators, and amplifiers, noise on the power supply can couple into critical parts of the circuit and degrade jitter tolerance or output jitter. The most absolute method of avoiding this issue is to use relatively quiet power supplies such as linear regulators. Easy to implement and low in cost, linear regulators typically don't generate noise great enough to affect transceiver performance, and they can filter noise from upstream supplies. However, their efficiency can be very low, especially when they operate from a high input voltage such as 3.3V or 5V. Converting 3.3V to 1.2V with a linear regulator is only 36% efficient. This low efficiency can be easily tolerated when a small number of transceivers are in use. However, if 12 or 20 transceivers are used, linear regulator presents a considerable thermal management design challenge.

One solution to this problem uses a switching regulator. The switching regulator can easily achieve greater than 85% efficiency and often can peak near 95%. The switching regulator frees board designers to use any input rail (3.3V, 5V, or 48V) to implement their design while still achieving manageable thermal constraints. This is the primary motivation for implementing switching regulators in large systems.

However, there exists one challenge. All switching regulators generate output voltage ripple. Output ripple is an AC waveform that rides on the DC value of the output. This ripple can be minimized but never eliminated. Although generally insignificant when powering digital circuits, output ripple can have adverse effects on sensitive analog circuits within the transceiver. This application note describes the sensitivies of the Virtex-4 RocketIO transceivers and how to minimize the effects of ripple on links running at data rates lower than 3.125 Gb/s.

Power Supply Ripple

The Sources of Ripple

Switching regulators (informally called *switchers*) operate by storing energy in an inductor and releasing the energy into a load. The topology of this *buck regulator* concept is illustrated in Figure 1.

There are two cycles of operation:

1. In the first cycle, the base of P-Channel MOSFET Q is driven Low. This creates a voltage ($V_{IN} - V_{OUT}$) across inductor L, which stores magnetic energy.

2. In the second cycle, the controller drives the gate of Q High. This opens the high-side connection to V_{IN}, and diode D becomes forward biased. Current flows through D and into the load, discharging the inductor.

The output voltage is regulated using a feedback technique that modifies the ratio of each cycle in response to load requirements.
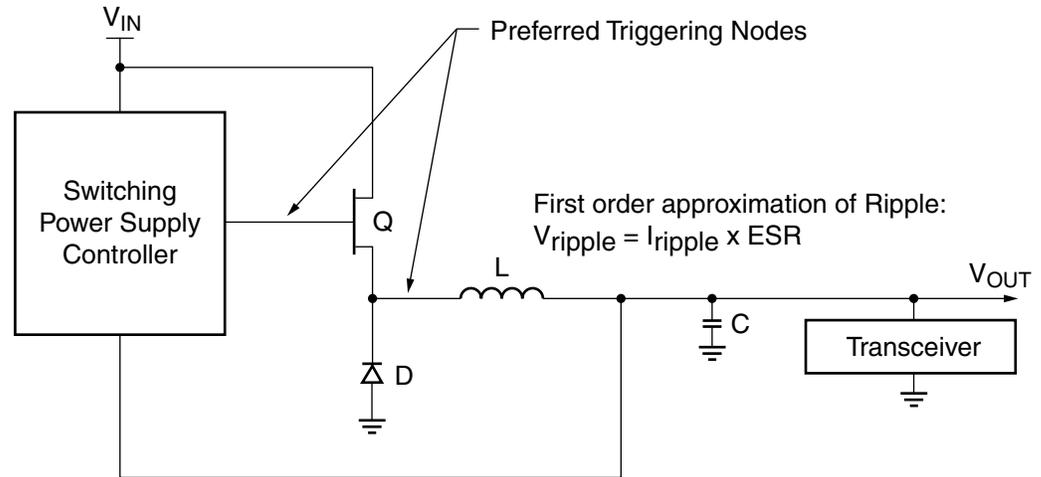
Preferred Triggering Nodes

Switching Power Supply Controller

First order approximation of Ripple:
$$V_{ripple} = I_{ripple} \times ESR$$

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Figure 1: **Buck Regulator Topology**

Notice that in either cycle, Q is turned completely on or off. In the first cycle, the current through Q is great, but the voltage is small. In the second cycle, the voltage is great, but the current is small. Q consumes very low power. The majority of the power is delivered into the load. This makes switching regulators very efficient.

However, the oscillating action creates a ripple current through the inductor that generates a voltage drop across the *equivalent series resistance* (ESR) of output filter capacitor C. This capacitor (or bank of capacitors) smooths out the ripple and creates a pole that is used for compensating the feedback loop. The smoothing effect of the output capacitor is limited by the ripple current that the switcher requires and by the ESR of the bank of capacitors. A practical setting for ripple current is 20% of the maximum load current; when a switcher is optimized for low ripple, a 20% ripple current is acceptable. A 5A switcher should have about 1Ap-p ripple. A capacitor bank with 10 mΩ ESR induces 10 mVp-p of voltage ripple. In most cases, this is a practical limitation. Obtaining less than 10 mVp-p at the regulation point of the output is very challenging. For this reason, achieving low-noise operation requires a post-filter.

Measuring Ripple

Accurately measuring power supply ripple can be tricky, especially low-amplitude ripple. High-speed sampling oscilloscopes are limited by front end noise and usually contribute 1 mVp-p or more of noise. Observing sub-10 mVp-p ripple is not a 100% accurate process.

There are a couple of techniques that help measure low-amplitude ripple. In the time domain, deriving a low-noise trigger is the most important consideration. Triggering from the output signal (top trace, Figure 2) generally yields very noisy results. This is because trigger uncertainty contributes much of the noise, and the signal appears to be noisier than it really is.

Triggering from a wide-amplitude signal synchronized to the output switching waveform (bottom trace, Figure 2) helps minimize trigger noise. Such waveforms exist on every switching power supply. Since the pass MOSFET must be toggled on and off, the gate of the FET has a considerable voltage swing, typically from the input supply rail to ground. Probing the gate of the external FET with a wide-bandwidth, low-capacitance, high-impedance probe provides a

low-noise trigger. Many power supplies have internal FETs; in this case, probing the inductor pin on the power supply provides a good trigger.

To illustrate this, a low-noise switching regulator was used to directly drive the Virtex-4 AVCCAUXTX pin with minimal filtering, yielding 4.76 mVp-p of ripple at the pin, as shown in Figure 2. (This was done for the purposes of demonstrating the probing technique; the actual target amplitude of 1 mVp-p is practically unmeasurable with a high-speed sampling oscilloscope and standard probes.)

In this situation, triggering from the top trace located at the Virtex-4 AVCCAUXTX pin would yield inconclusive results. A better trigger is the bottom trace, obtained from the wide-swinging node at the inductor of the power supply.
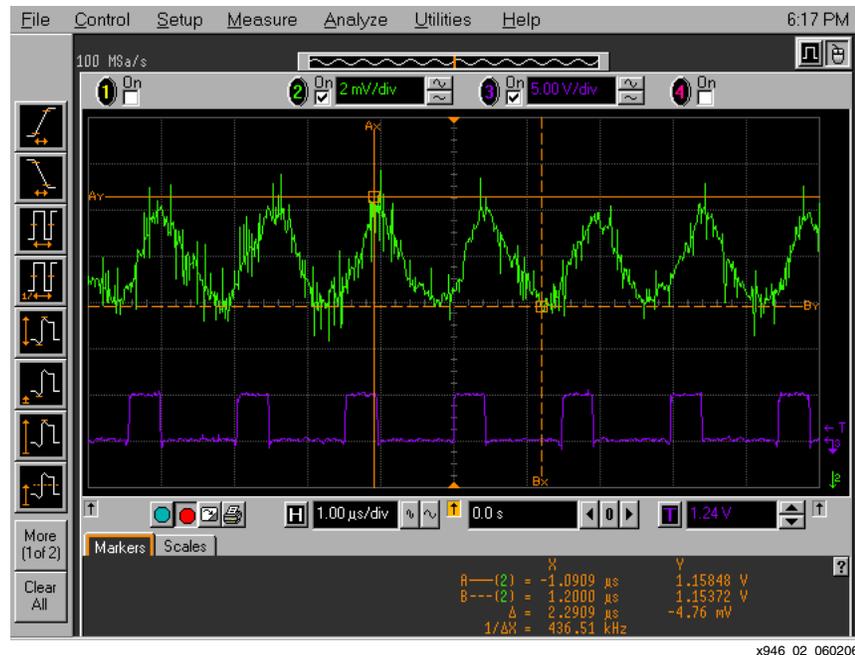

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Figure 2: **External (Top) and Internal (Bottom) Oscilloscope Trigger Points**

When probing the pin, it is important to note that there is a small amount of high-frequency noised generated from within the transceiver. This noise appears on an oscilloscope as a small set of spikes riding on top of the power supply ripple. Because there is no correlation between the switching frequency of the regulator circuit and the data-dependent noise induced from within the transceiver, these spikes occur randomly along the sampled waveform. It is important to measure the peak-to-peak ripple of the power supply without adding the effect of this inherent high-frequency noise. Figure 2 shows the sub-1mV spikes riding on top of the 600 kHz fundamental ripple frequency. The cursors are manually positioned to ignore that noise. A lower frequency scope automatically ignores those high-frequency noise components, which normally occur at hundreds of megahertz. It is also possible to set up the oscilloscope to filter them out digitally.

Another method for measuring power supply ripple involves the use of a spectrum analyzer. Less commonly used than an oscilloscope, spectrum analyzers are much more sensitive and require no triggering mechanism. When using a spectrum analyzer, set it to measure voltage, not power (dBm). Typically, a span of 0 to 10 MHz is wide enough to capture the fundamental switching ripple plus pertinent harmonics. (Some power supplies switch at 5 MHz or higher, making a wider span necessary.) Also consider that the termination into the spectrum analyzer is 50Ω A voltage division might be induced if an attenuating probe is used—10 kΩ in series with 50Ω for example. To avoid this, use a coaxial connection soldered directly on the vias below the device ball and coupled to the spectrum analyzer using SMA, BNC, or Type N connectors. Always AC-couple the signal into the spectrum analyzer using a DC-blocking capacitor.

Regardless of the instrumentation used, power supply noise must be measured at the Virtex-4 AVCCAUXTX or other pertinent pin. Measuring elsewhere presents unknown frequency-dependent disparity between the measured signal and what is actually happening at the pin. All guidelines presented in this application note refer only to noise measured at the pin.

The Effects of Ripple on the Transmitter

Power supply ripple affects the transmitter primarily through the AVCCAUXTX and AVCCAUXMGT pins. These pins power and bias the sensitive high-speed phase-locked loops and other analog components in the transmitter. As the power supply increases and decreases, it modulates the timing of the transmitter PLL. Since the fluctuations on power supply are periodic in nature, the timing variations are also periodic. The best way to determine the impact of ripple is by direct measurement of periodic jitter variations. The noise appears as periodic jitter and can be measured by a digital communications analyzer (DCA) or a jitter-optimized analyzer (DCA-J).

Periodic jitter is a component of deterministic jitter. A transmitter can generate a small amount of periodic jitter that can be correlated to the data or reference clock. The jitter produced by the ripple on the power supply pins is bounded—that is, not random—but it is not correlated to the data or the reference clock. This type of periodic jitter adds directly to the total jitter on the output.

The peak-to-peak periodic jitter is proportional to the amplitude of the ripple, typically about 2 ps/mV to 3 ps/mV for the Virtex-4 RocketIO transmitter. The exact dependence varies with data rate, temperature, and a host of operating conditions. The best way to avoid ripple-induced jitter is by keeping the ripple low, rather than trying to predict performance degradation based on a given set of conditions. A conservative estimate for tolerable peak-to-peak ripple is less than 1mVp-p over the band of 100 kHz to 5 MHz.

Ripple from 1m Vp-p to 4 mVp-p begins to degrade operation and should be carefully studied. System constraints such as link margin, receiver jitter tolerance frequency roll-off, and transmitter jitter generation requirements must be closely considered in each application.

Ripple greater than 4 mVp-p increases the total jitter of the transmitter by measurable amounts. Operating with ripple greater than 4 mVp-p is not recommended, although it can be functional in specific instances. If used, the customer must carefully study the effects of high-noise power supplies that can limit overall operation.

The Effects of Ripple on Bit Error Rate

The receiver also contains an internal PLL powered through the AVCCAUXRX pin. Enough modulation on the power supply induces receiver errors. However, it is important to look at in-band modulation versus out-of-band modulation. Typically, serial communication protocols require that the receiver ignore a certain amount of high-frequency jitter generated by the transmitter and track jitter induced at lower frequencies. Jitter induced at lower frequencies is considered out-of-band because the receiver can track it and it does not impair communication. In fact, an amount of jitter so excessive as to create transmitter eye closure can often be well tolerated by the receiver, provided it falls within the low-frequency cutoff of its response.

Luckily, most power supply noise modulation falls well below the cutoff of the receiver. On a typical transceiver, modulation induced by the power supply has little effect on bit error rate as long as it is below 1 MHz. Beyond 1 MHz, the receiver PLL begins to lose track of power supply modulation, and BER can rise.

As with the transmitter, the most conservative approach is to limit ripple in the band of 100 kHz to 5 MHz to under 1 mVp-p. In general, ripple has less influence on the receiver than on the transmitter. For that reason, following the constraints of the transmitter is the conservative approach to receiver power supply conditioning.

AVCCAUXMGT, VTTX, and VTRX

Virtex-4 AVCCAUXMGT ripple in the band of 100 kHz to 5 MHz should be under 1 mVp-p for all conditions. Using a switching regulator is possible provided it meets the low ripple limit. However, since this pin consumes considerably lower current than the other pins, it can easily be supplied by a linear regulator. Make sure that the linear regulator has adequate power supply rejection to attenuate noise generated by upstream switching regulators. Most linear regulators pass a considerable amount of noise from their inputs to their outputs at frequencies above 100 kHz. If this noise violates the ripple constraints, it degrades output jitter.

The termination voltages VTTX and VTRX sustain much better power supply noise rejection than the other supplies. In general, low-noise (on the order of 10 mVp-p) switching regulators can source the pins directly. Adverse effects are limited to common-mode deviations that track the ripple on the power supply pin. Observed differentially, transmit and receive signals remain relatively unaffected. If low common-mode noise on the transmitter output is required, VTTX power sources must remain clean. Ripple amplitude must be considerably lower than the maximum-output common deviation.

Techniques for Reducing Ripple

Switching power supplies unavoidably produce a finite amount of ripple. For this reason, the most practical method for reducing ripple at the transceiver power pin is to post-filter the switcher. Post-filtering involves using an LC or RC low-pass filter between the power supply and the transceiver power plane. There are two requirements:

First, the filter must sufficiently attenuate the primary switching frequency and harmonics. A good rule of thumb to follow is to place the pole a decade or so below the switcher's operating frequency. For example, a switcher running at 300 kHz should use a post-filter which begins to cut off around 30 kHz. In addition, switchers are known to generate very high frequencies in the form of LC tank ringing. Typically, high-frequency hash spikes in the tens of megahertz should also be attenuated. This can commonly be achieved with the use of an additional ceramic decoupling capacitor placed after the post-filter.

A second consideration involves the DC tolerance requirement of the transceivers. The power pin is specified with a ±5% absolute constraint. At 1.2V, this means the voltage at the pin cannot stray by more than 60 mV each way. Assuming the regulator and power distribution tolerances (including trace or plane losses) add up to 40 mV, the post-filter should not drop more than 20 mV worst-case over the operating range of the system. It must be kept in mind that the drop across the filter is dependent on variations in current consumption by the MGTs using the supply. (Turning MGTs on or off increases or decreases the drop.) An overly lossy filter can be overcome by placing additional filters in parallel or by tuning the power supply voltage slightly higher.

Switching Power Supply Design Examples

Go to http://focus.ti.com/analog/docs/gencontent.tsp?familyId=64&genContentId=1069 for these and other TI power supply reference designs.

1.2V/6A Supply for VCCAUXTX/RX

When selecting a switching power supply, there is a tradeoff between total board size, DC regulation, dynamic performance (i.e., transient response and output ripple), and efficiency. For power rails requiring more than 2A of current, a synchronous switcher (a switching power supply with a FET instead of diode for the low-side switch) provides the best efficiency. Switchers with integrated FETs minimize board space. Therefore, for these and other reasons to be discussed later, the TPS54x10 family of integrated FET switching converters was chosen for powering the transceivers. Figure 3 shows the schematic for the switching converter and post-filter used to power the AVCCAUXTX and AVCCAUXRX 1.2V power rails.

The TPS54610 6A switcher converts from 5V to 1.2V, providing 6A at approximately 85% efficiency, dissipating only 1.2W of the 7.2W of output power. A linear regulator would have 1.2V/5V = 25% efficiency and therefore need to dissipate (5 − 1.2)V x 6A = 22.8W through additional heat sinks. The switcher's regulation accuracy[1] must meet the ±5% accuracy specification for the transceiver power rail: in other words, the output voltage must not rise above +5% or droop below −5% of the regulated voltage. Most recent switching regulators, like the TPS54x10 series, have ±1% internal references and exceptional line and load regulation. Assuming operation over the full 6A current range with V_{IN} = 5V ±10%, the table below shows how the TPS54610 with ±1% external resistors provides exceptional steady-state regulation, leaving 3.37% or 41 mV for transient droop and output ripple.

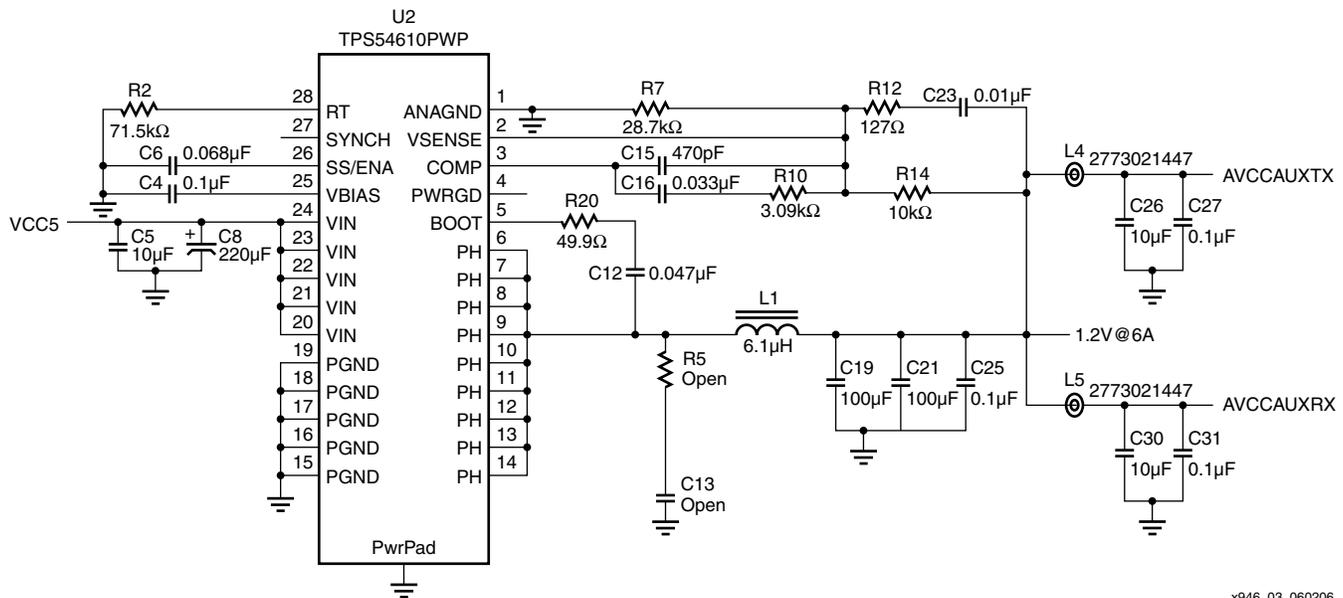x946_03_060206

Figure 3: **1.2V/6A Switching Power Supply Design**

Table 1: **TPS54610 Droop Factors and Computation**

Contributing Factor	Computation	Droop %
V_{REF} accuracy: ±1%		−1
1% external feedback resistors	2 x (1 − V_{REF} / V_{OUT}) x 1%	−0.5
Line regulation: 0.04% / V	0.04% / V x (5.5 − 4.5)V	−0.04
Load regulation: 0.03% / A	0.03% / A x (6 − 0)A	−0.09
Worst-case minimum DC tolerance		−1.63
% of V_{OUT} = 1.2V remaining for load transient droop and output ripple	5% − 1.63%	3.37% (41 mV)

Current to meet a step-load transient response is provided first by the small-valued, high-frequency decoupling capacitors at the transceiver power pins, followed by the mid-size, mid-frequency capacitors, followed by the switching regulator's bulk output capacitors, and finally followed by the switching regulator itself. Faster switching converters allow for lower-valued inductors and for wider-bandwidth feedback loops. Both of these factors contribute to faster

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1. Total regulation accuracy is determined by internal reference accuracy, feedback resistor tolerances, line and load regulation, transient response, and ½ the output ripple.

transient response times and therefore to lower transient droop of the voltage. Low ESR bulk capacitors also minimize transient droop.

A simple rule of thumb for determining the amount of bulk capacitance at the output of the switcher (assuming it has low equivalent series resistance or ESR) is given in Equation 1:

$$C_{OUT} = \frac{\Delta I_{TRANS}}{2\pi \cdot BW \cdot \Delta V_{TRANS}}$$

Equation 1

where I_{TRANS} is the expected load transient step, V_{TRANS} is the voltage droop and BW is the control loop bandwidth in the control. With C_{BULK} = 200 µF, this converter was designed with BW = 50 kHz and assuming I_{TRANS} = 2A and V_{TRANS} = 30 mV. For converters with post-filtering (like the one in Figure 3), the majority of the current to meet a step load is provided by the decoupling and bulk capacitors following the post-filter (not shown on the schematic). The switching converter feedback loop must be compensated for the amount of output capacitance prior to the post-filter.

Perhaps the most important design specification when powering transceivers is the output ripple. Switching converter output ripple is computed in Equation 2:

$$\Delta V_{RIPPLE} = \Delta I_L \left(ESR_{COUT} + \frac{1}{8 \cdot C_{OUT} \cdot f_{SW}} \right)$$

Equation 2

where I_L is the inductor ripple current and f_{SW} is the switching frequency. From this equation, it is apparent that to minimize ripple, the switcher should be designed for minimal inductor ripple current and fast switching, and should use low-ESR output capacitors.

To minimize I_L, power supply designers typically design buck converters with 30% of the maximum output current. When designing for low output ripple, designers oversize the inductor to give much lower inductor-current ripple. In this design, the designer used the fastest switching frequency for the TPS54610 (700 kHz) and an oversized inductor to give I_L = (5 − 1.2)V / 6.1 uH / 700 kHz = 0.9A, or 15% of the maximum output current.

When using larger inductors, efficiency suffers due to their higher DC resistance. These tradeoffs are not unexpected in power supply design. From the equation above, the output ripple is 5.3 mVp-p. Referring back to the tolerance calculation in Table 1, 41 mV – 30 mV transient droop – (5.3 mVp-p) / 2 = 8.35 mV tolerance margin remaining. Lower output ripple values are theoretically possible at the expense of efficiency and load transient response, but they are difficult to achieve due to PCB parasitic resistances and inductances, both neglected in the above calculations.

The post-LC filters (L4/C26/C27 and L5/C30/C31) were used to provide further reduction in the output ripple and higher-frequency switching spikes. L4 and L5 are Fair Rite 2773021447 ferrite beads and, in conjunction with the 10 µF output capacitor, form a filter that attenuates the 700 kHz ripple by a factor of approximately 5, or 14 dB at the transceiver pin. The 0.1 µF capacitors C30 and C31 provide additional filtering of higher-frequency switching spikes.

It is important to meet the DC tolerance requirements of the transceiver. The DC resistance of the post-filter bead produces a load-current dependent droop that must be considered. If the droop of the traces and the post-filter exceed 40 mV, the power supply at the pin can be considered out of regulation. Therefore, it might be necessary to design the switcher to regulate at a higher voltage—e.g., 1.24V instead of 1.2V—to account for this drop, depending on the maximum current comsumption.

The AVCCAUXTX worst-case current consumption operating at 3.125 Gb/s is 307 mA per tile (two transceivers running). The AVCCAUXRX worst-case current consumption operating at 3.125 Gb/s is 382 mA per tile (two transceivers running). Operating with twelve transceivers gives an overall required operating current of 2.3A for the receivers and 1.9A for the transmitters. The reference circuit presented here separates the filter into a transmitter side and receiver side. This lowers the DC current requirement of the filter. The Fair Rite 2730021447 ferrite has a worst-case DC resistance of 0.0009Ω This induces a worst-case drop of 2.07 mV

for the receiver and 1.71 mV for the transmitter, both well within the 8.35 mV of remaining DC tolerance.

1.5V/1.5A Supply for VTTX/VTRX

Figure 4 shows the schematic for the switching converter used to power the V4 VTTX and V4 VTRX 1.5-V termination power rails. Although ultra-low output ripple is not required for this rail, a lower current version of the same family of converters was used to simplify design. No ferrite bead was used to provide post-LC filtering. For a simplified design, it is possible to power VTTX and VTRX from 1.2V if the device at the other side of the communication link is similarly supplied. This would result in a lower output voltage swing; however, for short chip-to-chip links, this may acceptable.
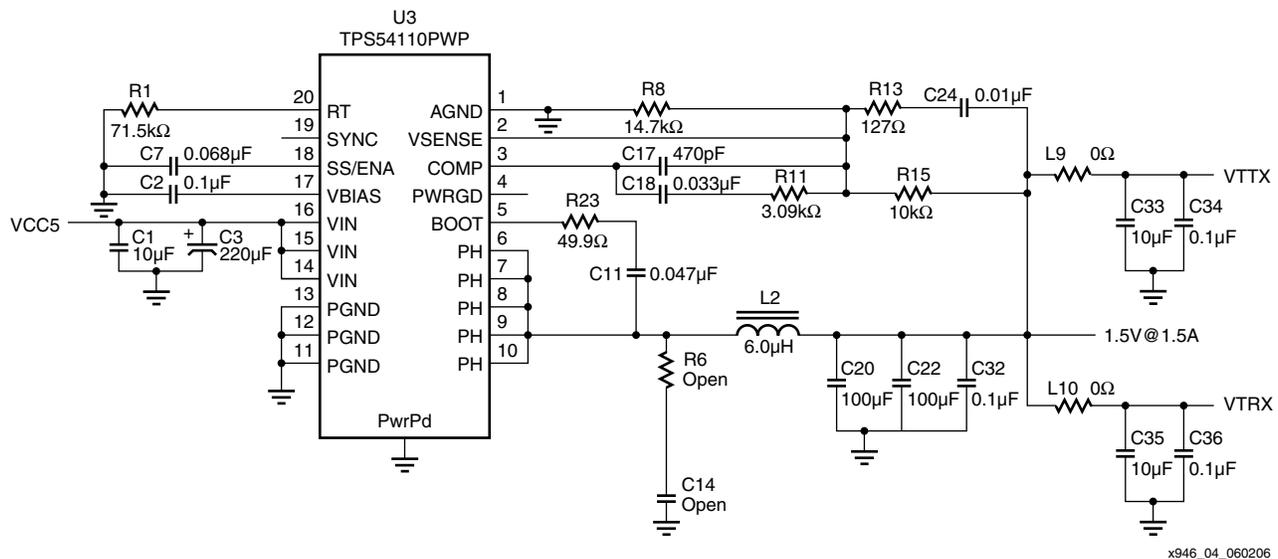

Figure 4: **1.5V/1.5A Switching Power Supply Design**

Linear Regulator for AVCCAUXMGT

Linear regulators are lower in cost than switching converters and do not have output ripple noise. In fact, linear regulators provide high-input power supply ripple rejection (PSRR) up to their 50–100 kHz or so control-loop bandwidth. Above their loop bandwidth, linear regulators still provide some filtering through the board and IC parasitic capacitances interacting with the output capacitors. As previously mentioned, the linear regulator's major drawback is inefficiency. Therefore, when selecting a linear regulator, it is imperative that the regulator's package can dissipate the necessary amount of lost power. Figure 5 shows the schematic for the linear regulator circuit used to power the 250 mA AVCCAUXMGT 2.5V rail.
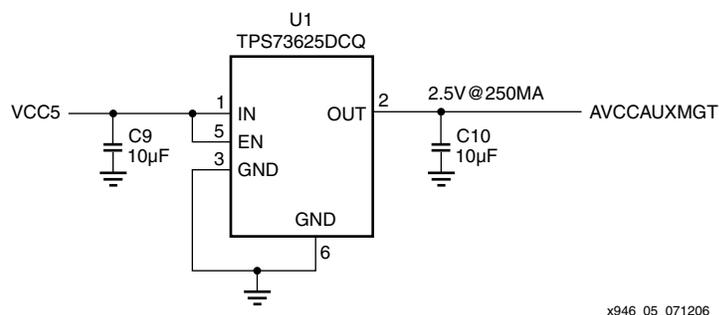

Figure 5: **2.5V Linear Regulator Circuit Design**

For this low-power rail with minimum load transients, the TPS73625 400 mA linear regulator with only a 10 µF output capacitor is acceptable. It has 37 dB PSRR at 10 kHz, and its SOT-223 package, capable of dissipating 0.76W at 85°C, can easily dissipate the 0.625W ([5V – 2.5V] x 0.250A) of heat produced in this configuration.

Test Results

The following table summarizes the data captured in the included DCA-J screen shots.

Table 2:

Data Rate	2.5 Gb/s / 250 MHz Reference Clock			3.125 Gb/s / 312.5 MHz Reference Clock		
Noise at the AVCCAUXTX pin	**Ideal**	**1 mVp-p**	**4.76 mVp-p**	**Ideal**	**1m Vp-p**	**4.76 mVp-p**
Power source description	Bench-top supply	Switching regulator with post-filter	Switching regulator with no post-filter	Bench-top supply	Switching regulator with post-filter	Switching regulator with no post-filter
Total Jitter (ps)	56.3	59.6	64.9	48.3	51.3	63.3
Periodic Jitter (ps)	17.5	20.1	25.9	11	15	25
Increase from ideal (ps)	n/a	2.6	9	n/a	4	14

2.5 Gb/s

This section shows the results of tests carried out in a 2.5 Gb/s data-rate configuration.

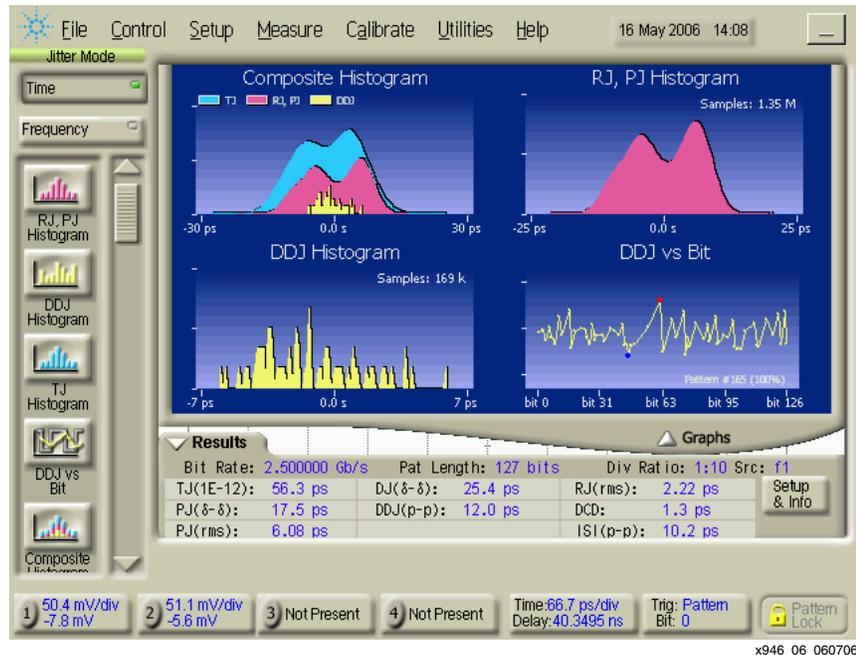Figure 6 shows DCA-J measurements with a clean bench-top supply.

Figure 6: **DCA-J, 2.5 Gb/s, Clean Bench-Top Supply**

Figure 7 shows DCA-J measurements with a switching supply (1 mVp-p noise at the pin).
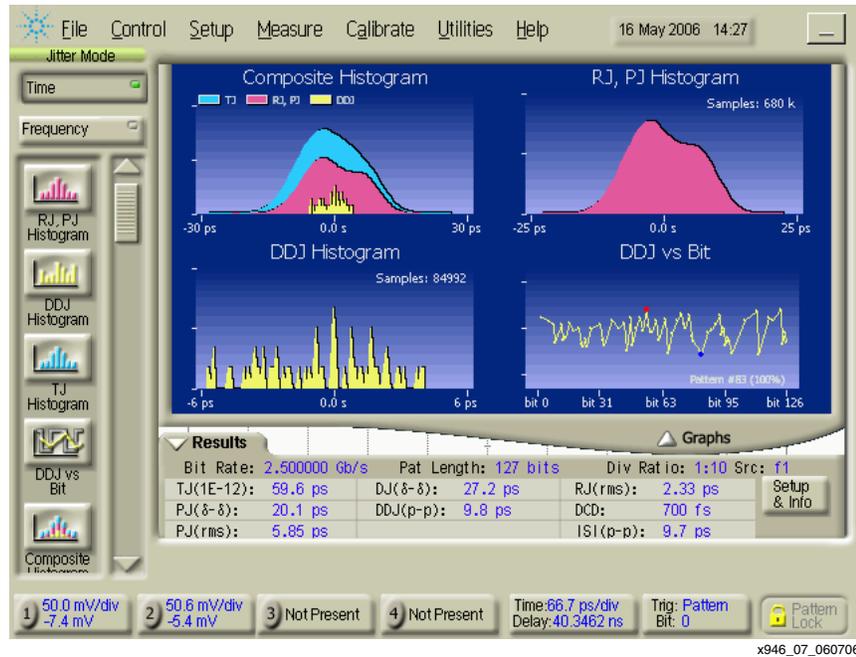

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Figure 7: **DCA-J, 2.5 Gb/s, Switching Power Supply (1 mV Noise)**

Figure 8 shows DCA-J measurements with a switching supply (4.76 mVp-p noise at the pin).
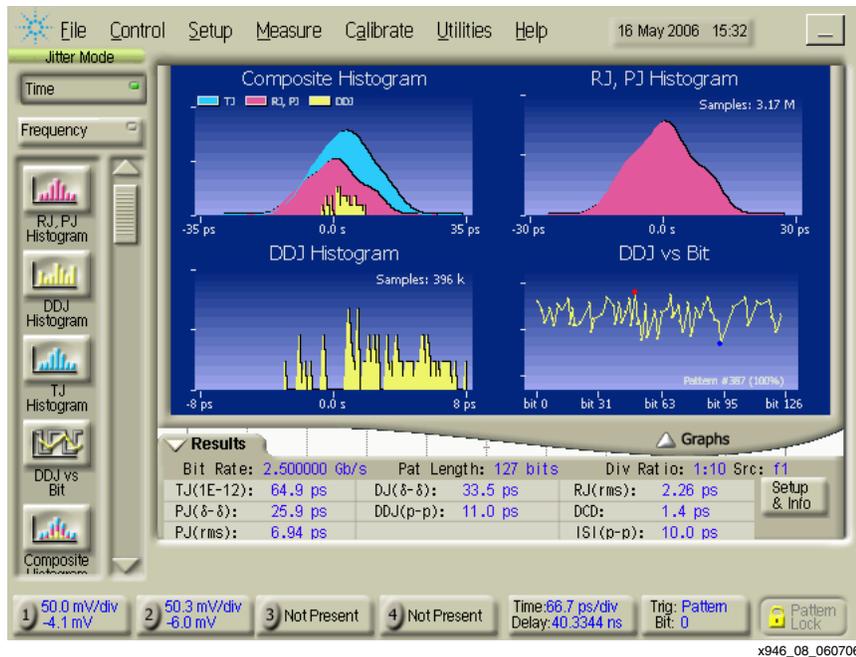

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Figure 8: **DCA-J, 2.5 Gb/s, Switching Power Supply (4.76 mV Noise)**

3.125 Gb/s

This section shows the results of tests carried out in a 3.125 Gb/s data-rate configuration.

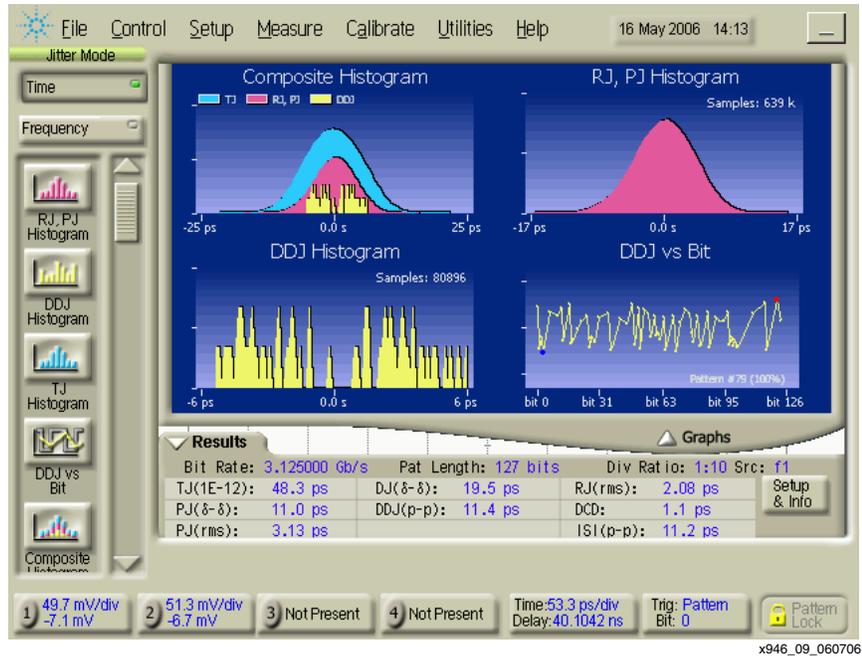Figure 9 shows DCA-J measurements with a clean bench-top supply.

Figure 9: **DCA-J, 3.125 Gb/s, Clean Bench-Top Supply**

Figure 10 shows DCA-J measurements with a switching supply (1 mVp-p noise at the pin).
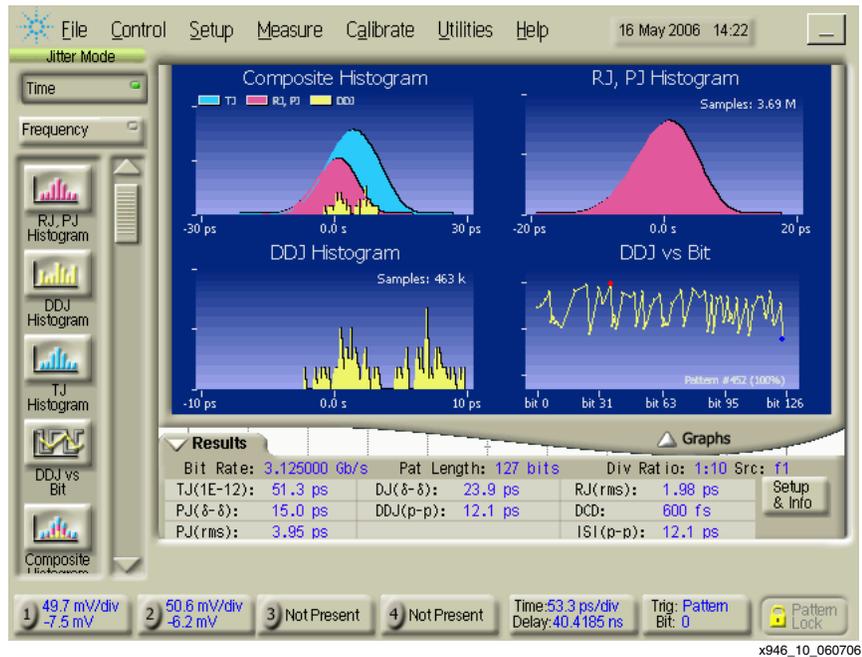

Figure 10: **DCA-J, 3.125 Gb/s, Switching Power Supply (1 mV Noise)**

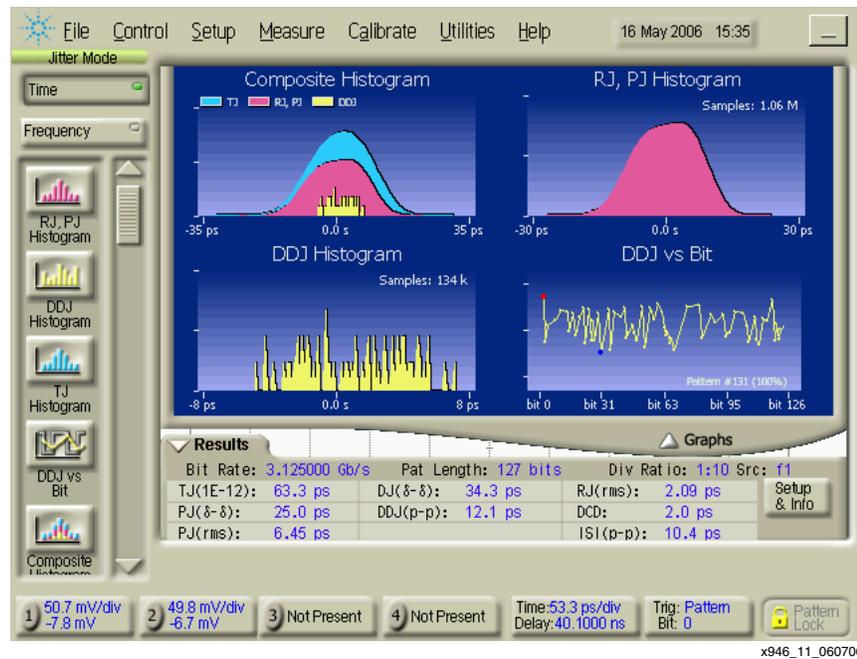Figure 11 shows DCA-J measurements with a switching supply (4.76 mVp-p noise at the pin).

Figure 11: **DCA-J, 3.125 Gb/s, Switching Power Supply (4.76 mV Noise)**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/10/06	v1.0	Initial Xilinx release.
08/14/06	v1.0.1	Removed Spartan-3E from applicabale device families.