MGT CHARACTERIZATION BOARD FOR V5 AFXII COMPATIBLE

POWER IN 5.0V

FPGA POWER SOURCE
ON BOARD REGULATION
CORE 1.0V @ 7 AMPS
VCCO 2.5V AT 6 AMPS
VCCAUX 2.5V AT 3 AMPS
PAGE 5

CPACITIVE LOADS
ALL UNUSED I/O'S
10pF LOADS
PAGE 18

AFXII RING
PAGES 6-8

GTP116
PAGE 3

GTP112
PAGE 4

GTP114
PAGE 4

GTP118
PAGE 3

FF665

SYSTEM ACE
PAGE 2

XGI
PAGE 13

DDR2 MEMORY
64 bit wide
UP TO128MB
200-400 MHz
PAGES 10-12

MGT POWER
PAGE 9

XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
BLOCK DIAGRAM

Date: 12-22-2006_11:36	Ver: B
Sheet Size: B	Rev: 01
Sheet 1 of 20	Drawn By PATRICK J.

JTAG HEADER

HDR_1X6

J2

VCC33

1
2
3 TCK — 2
4 TDO — 2
5 TDI — 2
6 TMS — 2

H-1X6

VCC33

C13 100UF 10V TANT
C11 4.7UF 10V TANT
C15 X7R 16V 0.1UF
C16 X7R 16V 0.1UF
C17 X7R 16V 0.1UF
R6 4.7K 5% 1/16W

VCCAUX

C14 100UF 10V TANT
C12 4.7UF 10V TANT
C20 X7R 16V 0.1UF
C19 X7R 16V 0.1UF
C18 X7R 16V 0.1UF

VCC33

ERRLED# — LED-GRN-SMT DS2 — R15 100 5% 1/16W
STATLED# — LED-GRN-SMT DS1 — R14 100 5% 1/16W

VCCAUX

SYSTEM ACE CLOCK

C21 X7R 16V 0.1UF
C22 X7R 16V 0.1UF
R4 4.7K 5% 1/16W
J4
H-1X3

X1
4236-118-14
33 MHz

ACE_CLK-R
ACE_CLK — R1 0 5% 1/10W
R5 4.7K 5% 1/16W

CFD[15:00]

CFA[10:00]

U16
XCCACE-TQ144I

U16			XCCACE-TQ144I
	NC	2	TCK
2	CFREG#	3	CFREG
2	CFA00	4	CFA00
	CFD00	5	CFD00
	CFD01	6	CFD01
	CFD08	7	CFD08
	CFD02	8	CFD02
	CFD09	11	CFD09
	CFD10	12	CFD10
2	CFCD2#	13	CFCD2
	NC	14	CFGTCK3
	NC	16	CFGINIT3
	NC	19	CFGINIT2
	NC	20	CFGTDI3
	NC	21	CFGTDO2
	NC	22	CFGPROG2
	NC	23	CFGTMS2
	NC	24	CFGTCK2
	NC	27	CFGTDI2
	NC	28	CFGTDO1
	NC	29	CFGPROG1
	NC	30	CFGTMS1
	NC	31	CFGTCK1
	NC	32	CFGTDI1
		33	RESET
	NC	34	TDI
	NC	36	TDO

2	CFA10	121	CFA10
2	CFCE1#	119	CFCE1#
2	CFD15	118	CFD15
	NC	143	TMS
	CFA01	142	CFA01
	CFA02	141	CFA02
2	CFWAIT#	140	CFWAIT#
2	CFA03	139	CFA03
2	CFCE2#	138	CFCE2#
	CFA04	137	CFA04
	CFA05	135	CFA05
	CFA06	134	CFA06
	CFA07	133	CFRDYNBSY
2	CFWE#	132	CFA07
	CFA08	131	CFWE#
	NC	130	CFA08
	CFGTMS3	127	NC
	CFA09	125	CFA09
	CFGPROG3	124	NC
2	CFOE#	123	CFOE#
	CFGTDO3	122	NC
	CFD07	117	CFD07
	CFD14	116	CFD14
	CFD06	115	CFD06
	CFD13	114	CFD13
	CFD05	113	CFD05
	M1	112	M1
	M0	110	M0
	M2	108	M2
	CFD12	107	CFD12
	CFD04	106	CFD04
	CFD11	105	CFD11
	CFD03	104	CFD03
	CFCD1	103	CFCD1# 2
	TSTTDI	102	TDI 2
	TSTTCK	101	TCK 2
	TSTTMS	98	TMS 2
	TSTTDO	97	TDO 2
	ERRLED	96	ERRLED# 2
	STATLED	95	STATLED# 2
	CLK	93	ACE_CLK 2
	CFGINIT1	90	NC
	CFGMODE	89	
	CFGADDR2	88	CFGADDR2
	CFGADDR1	87	
	CFGADDR0	86	CFGADDR0
	CFGTMS0	85	FL_TMS
	CFGTDO0	82	FL-TDO
	CFGTDI0	81	FL-TDI
	CFGTCK0	80	FL_TCK
	CFGPROG0	79	PROG 7,14,15
	CFGINIT0	78	INIT 2,7,14,15
	MPOE	77	MPOE# 16
	MPWE	76	MPWE# 16
	DONE	74	NC

	PROGRAM	72	
	NC	71	INIT
16	MPA00	70	MPA00
16	MPA01	69	MPA01
16	MPA02	68	MPA02
16	MPD00	66	MPD00
16	MPA03	67	MPA03
16	MPD01	65	MPD01
16	MPD02	63	MPD02
16	MPD03	62	MPD03
16	MPD04	61	MPD04
16	MPD05	60	MPD05
16	MPD06	59	MPD06
16	MPD07	58	MPD07
	NC	56	NC
	NC	55	MPD08
	NC	53	MPD09
	NC	52	MPD10
	NC	51	MPD11
	NC	50	MPD12
	NC	49	MPD13
	NC	48	MPD14
	NC	47	MPD15
16	MPA04	45	MPA04
16	MPA05	44	MPA05
16	MPA06	43	MPA06
16	MPIRQ	42	MPCE
	NC	40	MPIRQ
16	MPBRDY	39	DIN
	NC	38	MPBRDY
			CCLK

SIGNAL=VCC33;1,17,37,55,73,92,109,128
SIGNAL=GND;83,91,100,111,120,129,136,144
SIGNAL=GND;9,18,26,35,46,54,64,75
SIGNAL=VCCAUX;10,15,25,57,84,94,99,126

SW?	FUNCTION
1	CONFIG FILE ADDESS 2
2	CONFIG FILE ADDESS 1
3	CONFIG FILE ADDESS 0
1 2 3	SELETION
○ ○ ○	FILE INDEX 0
○ ○ ●	FILE INDEX 1
○ ● ○	FILE INDEX 2
● ● ●	FILE INDEX 7

NOTATION
○ OPEN
● CLOSED

VCC33 — R9 4.7K 5% 1/16W

VCCAUX

SW1
CFGADDR2
CFGADDR1
OMROM_A6S-5102

J131 H-1X2
CFG_TMS 7,13,15
CFG_TCK 7,13,15
J132 H-1X2
H-1X2 J129
REMOVE JUMPER TO ISOLATE FLASH J-TAG
CFG_TDO 7,15
CFG_TDI 7,13
H-1X2 J128

VCCAUX

J5
H-1X3

RS-232

U3
MAX3388ECUG+

C23 X7R 16V 0.1UF
C24 X7R 16V 0.1UF
C26 X7R 16V 0.1UF
C25 X7R 16V 0.1UF

	C1+	1	
	C1-	3	
	C2+	4	
	C2-	5	
	T1IN	7	
15	T2IN	8	
15	T3IN	9	
15	R1OUT	13	
15	R2OUT	12	
	LOUT	10	NC
	SWOUT	11	NC
	SHDN	24	
	VCC	23	
	VL	14	
	V+	2	
	V-	6	
	T1OUT	21	TXD
	T2OUT	20	RTS
	T3OUT	19	NC
	R1IN	18	RXD
	R2IN	17	CTS
	LIN	16	NC
	SWIN	15	NC
	GND	22	

DB-9 CONECTOR
5747250-4
J3

1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
11	GND3
10	GND2

CF CONNECTOR

U2
N7E50-7516PG-20

		1	
	CFD03	2	
	CFD04	3	
	CFD05	4	
	CFD06	5	
	CFD07	6	
	CFCE1#	7	
2	CFA10	8	
2	CFOE#	9	
	CFA09	10	
	CFA08	11	
	CFA07	12	
		13	
	CFA06	14	
	CFA05	15	
	CFA04	16	
	CFA03	17	
	CFA02	18	
	CFA01	19	
	CFA00	20	
	CFD00	21	
	CFD01	22	
	CFD02	23	
	NC	24	
2	CFCD2#	25	
2	CFCD1#	26	
	CFD11	27	
	CFD12	28	
	CFD13	29	
	CFD14	30	
	CFD15	31	
2	CFCE2#	32	
	NC	33	
	IORD#	34	
	IOWR#	35	
2	CFWE#	36	
	NC	37	
		38	
	CSEL#	39	
	NC	40	
		41	
	CFWAIT#	42	
2	NC	43	
2	CFREG#	44	
	NC	45	
	NC	46	
	CFD08	47	
	CFD09	48	
	CFD10	49	
		50	

CFD[15:00]

SW2 EVQ-11L07K
RESET#
VCC33
R7 4.7K 5% 1/16W
R8 4.7K 5% 1/16W
CFRESET
R12 1.00K 1% 1/16W
R13 1.00K 1% 1/16W

8 I2C_DUT_WP
8 I2C_DUT_SCL
8 I2C_DUT_SDA

U12
24LC32
SCL
SDA
WP
A0
A1
A2
VCC
GND

VCC33
C183 X7R 16V 0.1UF

I2C EEPROM

VCCO

J1

		2	1
2	TMS	4	3
2	TCK	6	5
2	TDO	8	7
2	TDI	10	9
	NC	12	11
2,7,15	INIT	14	13

87832-1420

GND TEST POINTS

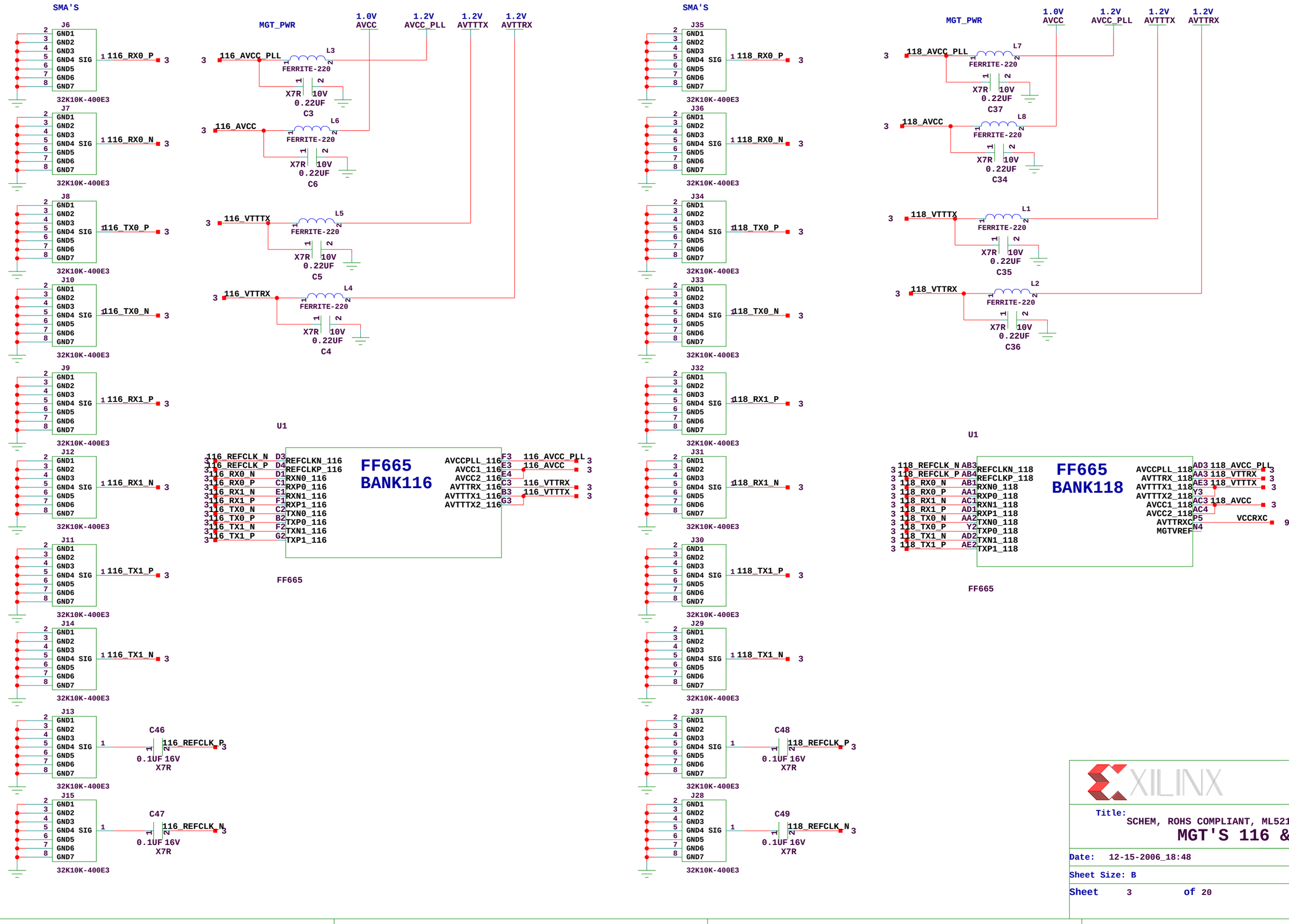
J16 10-109-3-01
J18 10-109-3-01
J23 10-109-3-01
J22 10-109-3-01
J20 10-109-3-01

XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
SYSTEM ACE/UART/CONFIGURATION PINS

Date: 12-15-2006_18:48	Ver: B
Sheet Size: B	Rev: 01
Sheet 2 of 20	Drawn By PATRICK J.



XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
MGT'S 116 & 118

Date: 12-15-2006_18:48	Ver: B
Sheet Size: B	Rev: 01
Sheet 3 of 20	Drawn By PATRICK J.

SMA'S

J54 — 32K10K-400E3 — 112_RX0_P
J56 — 32K10K-400E3 — 112_RX0_N
J55 — 32K10K-400E3 — 112_TX0_P
J53 — 32K10K-400E3 — 112_TX0_N
J52 — 32K10K-400E3 — 112_RX1_P
J51 — 32K10K-400E3 — 112_RX1_N
J50 — 32K10K-400E3 — 112_TX1_P
J49 — 32K10K-400E3 — 112_TX1_N
J57 — 32K10K-400E3 — C50 — 112_REFCLK_P — 0.1UF 16V X7R
J48 — 32K10K-400E3 — C51 — 112_REFCLK_N — 0.1UF 16V X7R

MGT_PWR

1.0V AVCC
1.2V AVCC_PLL
1.2V AVTTTX
1.2V AVTTRX

112_AVCC_PLL — L11 FERRITE-220 — X7R 10V 0.22UF C41
112_AVCC — L12 FERRITE-220 — X7R 10V 0.22UF C38
112_VTTTX — L9 FERRITE-220 — X7R 10V 0.22UF C39
112_VTTRX — L10 FERRITE-220 — X7R 10V 0.22UF C40

U1

FF665 BANK112

112_REFCLK_N	K3	REFCLKN_112	
112_REFCLK_P	K4	REFCLKP_112	
112_RX0_N	K1	RXN0_112	
112_RX0_P	J1	RXP0_112	
112_RX1_N	L1	RXN1_112	
112_RX1_P	M1	RXP1_112	
112_TX0_N	J2	TXN0_112	
112_TX0_P	H2	TXP0_112	
112_TX1_N	M2	TXN1_112	
112_TX1_P	N2	TXP1_112	
AVCCPLL_112	M3	112_AVCC_PLL	
AVTTRX_112	J3	112_VTTRX	
AVTTTX1_112	H3	112_VTTTX	
AVTTTX2_112	N3		
R_TERM_112	M5	RTERM112	
AVCC1_112	L3	112_AVCC	
AVCC2_112	L4		
RREF	P4		

FF665

112_VTTTX — R135 49.9 1% 1/10W — NC — R136 DNP 1% 1/16W — R137 49.9 1% 1/16W

FEATURE AVAILABLE ON FX DEVICE

SMA'S

J45 — 32K10K-400E3 — 114_RX0_P
J46 — 32K10K-400E3 — 114_RX0_N
J44 — 32K10K-400E3 — 114_TX0_P
J43 — 32K10K-400E3 — 114_TX0_N
J42 — 32K10K-400E3 — 114_RX1_P
J41 — 32K10K-400E3 — 114_RX1_N
J40 — 32K10K-400E3 — 114_TX1_P
J39 — 32K10K-400E3 — 114_TX1_N
J47 — 32K10K-400E3 — C52 — 114_REFCLK_P — 0.1UF 16V X7R
J38 — 32K10K-400E3 — C53 — 114_REFCLK_N — 0.1UF 16V X7R

MGT_PWR

1.0V AVCC
1.2V AVCC_PLL
1.2V AVTTTX
1.2V AVTTRX

114_AVCC_PLL — L15 FERRITE-220 — X7R 10V 0.22UF C45
114_AVCC — L16 FERRITE-220 — X7R 10V 0.22UF C42
114_VTTTX — L13 FERRITE-220 — X7R 10V 0.22UF C43
114_VTTRX — L14 FERRITE-220 — X7R 10V 0.22UF C44

U1

FF665 BANK114

114_REFCLK_N	T3	REFCLKN_114	
114_REFCLK_P	T4	REFCLKP_114	
114_RX0_N	T1	RXN0_114	
114_RX0_P	R1	RXP0_114	
114_RX1_N	U1	RXN1_114	
114_RX1_P	V1	RXP1_114	
114_TX0_N	R2	TXN0_114	
114_TX0_P	P2	TXP0_114	
114_TX1_N	V2	TXN1_114	
114_TX1_P	W2	TXP1_114	
AVCCPLL_114	V3	114_AVCC_PLL	
AVCC1_114	U3	114_AVCC	
AVCC2_114	U4		
AVTTRX_114	R3	114_VTTRX	
AVTTTX1_114	P3	114_VTTTX	
AVTTTX2_114	W3		

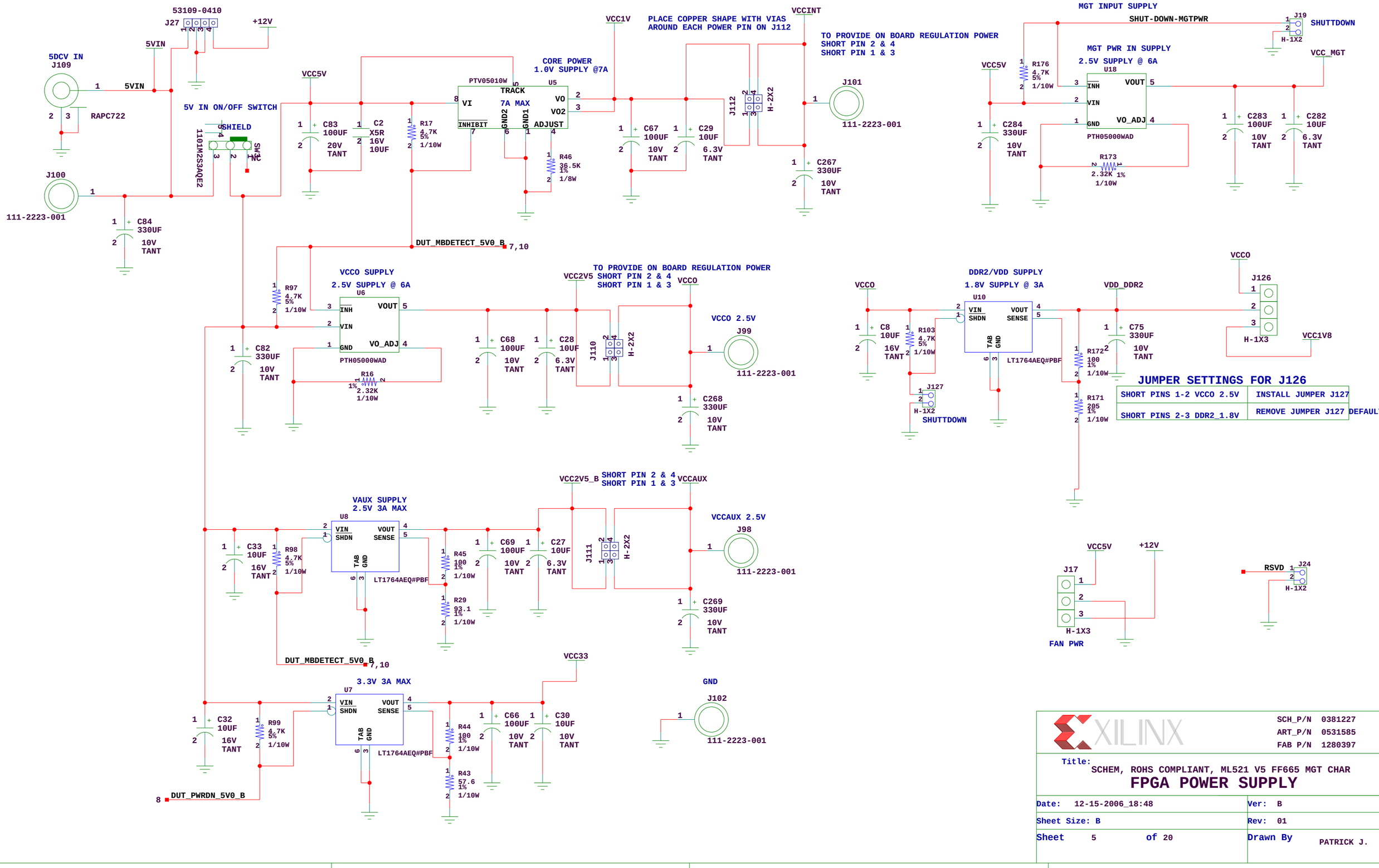
FF665

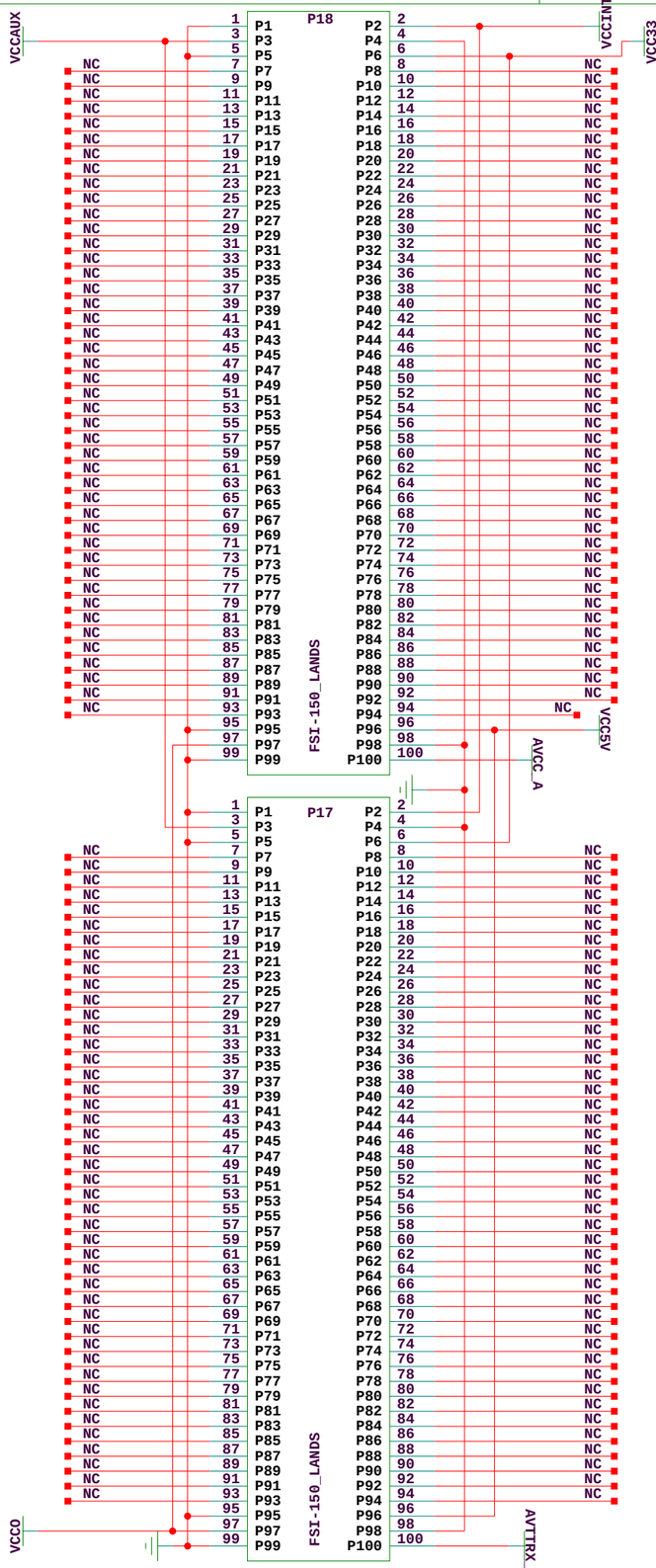
XILINX

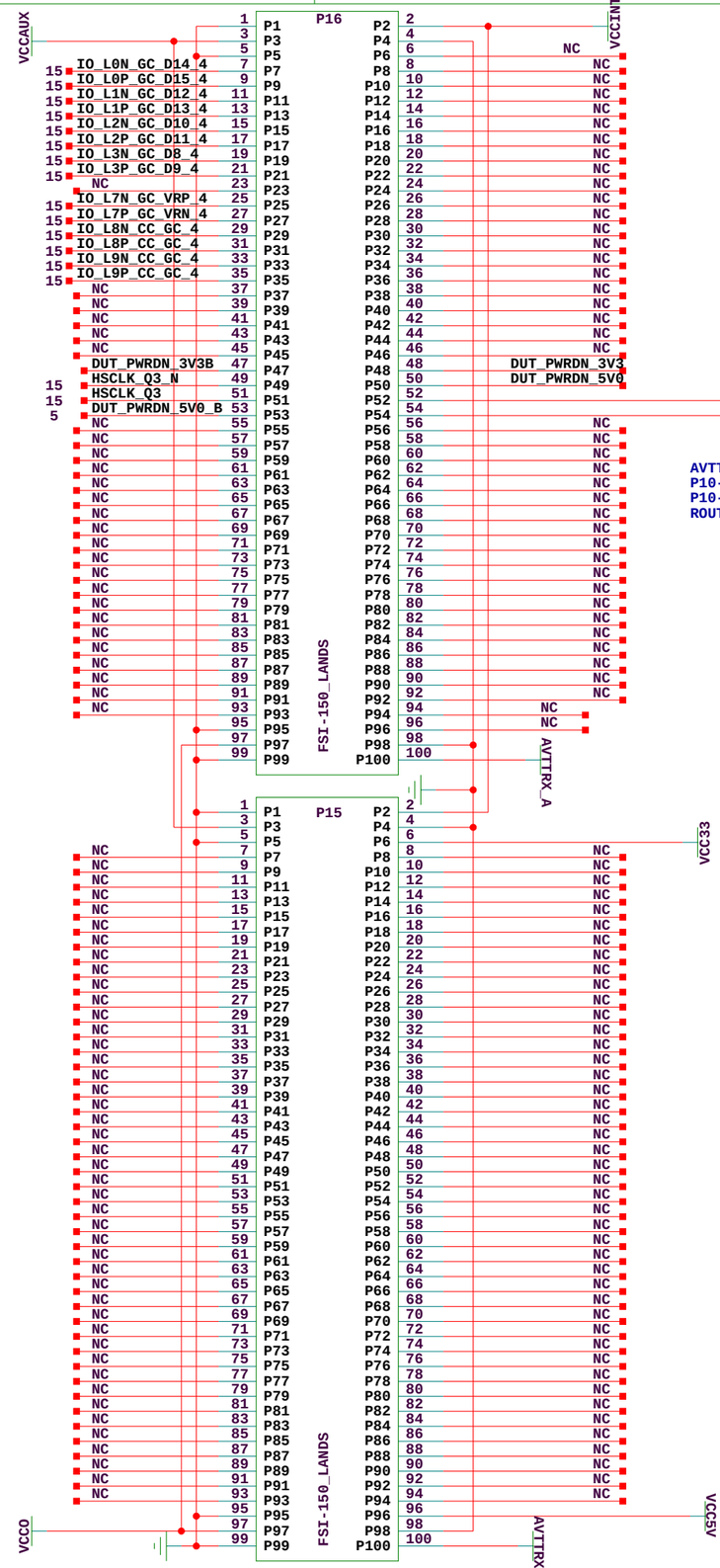
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title: SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
MGT'S 112 & 114

Date: 12-15-2006_18:48	Ver: B
Sheet Size: B	Rev: 01
Sheet 4 of 20	Drawn By PATRICK J.


5DCV IN
J109
RAPC722
5VIN
53109-0410
J27
+12V
5V IN ON/OFF SWITCH
SHIELD
1101M2S3AQE2
SW-NC
J100
111-2223-001
C84
330UF
10V
TANT
VCC5V
C83
100UF
20V
TANT
C2
X5R
16V
10UF
R17
4.7K
5%
1/10W
PTV05010W
U5
TRACK
7A MAX
VI
VO
VO2
INHIBIT
GND2
GND1
ADJUST
R46
36.5K
1%
1/8W
CORE POWER
1.0V SUPPLY @7A
VCC1V
C67
100UF
10V
TANT
C29
10UF
6.3V
TANT
J112
H-2X2
PLACE COPPER SHAPE WITH VIAS
AROUND EACH POWER PIN ON J112
VCCINT
TO PROVIDE ON BOARD REGULATION POWER
SHORT PIN 2 & 4
SHORT PIN 1 & 3
J101
111-2223-001
C267
330UF
10V
TANT
DUT_MBDETECT_5V0_B
7,10
MGT INPUT SUPPLY
SHUT-DOWN-MGTPWR
J19
SHUTTDOWN
H-1X2
MGT PWR IN SUPPLY
2.5V SUPPLY @ 6A
VCC5V
R176
4.7K
5%
1/10W
U18
INH
VIN
GND
VOUT
VO_ADJ
PTH05000WAD
C284
330UF
10V
TANT
R173
2.32K
1%
1/10W
VCC_MGT
C283
100UF
10V
TANT
C282
10UF
6.3V
TANT
VCCO SUPPLY
2.5V SUPPLY @ 6A
R97
4.7K
5%
1/10W
U6
C82
330UF
10V
TANT
R16
2.32K
1%
1/10W
TO PROVIDE ON BOARD REGULATION POWER
SHORT PIN 2 & 4
SHORT PIN 1 & 3
VCC2V5
VCCO
C68
100UF
10V
TANT
C28
10UF
6.3V
TANT
J110
VCCO 2.5V
J99
111-2223-001
C268
330UF
10V
TANT
DDR2/VDD SUPPLY
1.8V SUPPLY @ 3A
VCCO
C8
10UF
16V
TANT
R103
4.7K
5%
1/10W
U10
VIN
SHDN
VOUT
SENSE
TAB
GND
LT1764AEQ#PBF
J127
H-1X2
SHUTTDOWN
VDD_DDR2
C75
330UF
10V
TANT
R172
100
1%
1/10W
R171
205
1%
1/10W
VCCO
J126
H-1X3
VCC1V8
JUMPER SETTINGS FOR J126
SHORT PINS 1-2 VCCO 2.5V
INSTALL JUMPER J127
SHORT PINS 2-3 DDR2_1.8V
REMOVE JUMPER J127 DEFAULT
VAUX SUPPLY
2.5V 3A MAX
U8
R98
4.7K
5%
1/10W
C33
10UF
16V
TANT
R45
100
1%
1/10W
R29
93.1
1%
1/10W
C69
100UF
10V
TANT
C27
10UF
6.3V
TANT
J111
VCC2V5_B
SHORT PIN 2 & 4
SHORT PIN 1 & 3
VCCAUX
VCCAUX 2.5V
J98
111-2223-001
C269
330UF
10V
TANT
DUT_MBDETECT_5V0_B
7,10
3.3V 3A MAX
U7
R99
4.7K
5%
1/10W
C32
10UF
16V
TANT
R44
100
1%
1/10W
R43
57.6
1%
1/10W
C66
100UF
10V
TANT
C30
10UF
10V
TANT
VCC33
GND
J102
111-2223-001
DUT_PWRDN_5V0_B
8
VCC5V
+12V
J17
H-1X3
FAN PWR
RSVD
J24
H-1X2
XILINX
SCH_P/N 0381227
ART_P/N 0531585
FAB P/N 1280397
Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
FPGA POWER SUPPLY
Date: 12-15-2006_18:48
Ver: B
Sheet Size: B
Rev: 01
Sheet 5 of 20
Drawn By PATRICK J.





AVTTRX

AVTTRX VOLTAGE SENSE
P10-52 WAS VDCPS6_SNS_P
P10-54 WAS VDCPS6_SNS_N
ROUTE DIFF TO DUT

AFXII MOUNTING HOLES

MH4 1 MH_125_250
MH5 1 MH_125_250
MH6 1 MH_125_250
MH7 1 MH_125_250
MH8 1 MH_125_250
MH9 1 MH_125_250
MH15 1 MH_125_250
MH14 1 MH_125_250
MH13 1 MH_125_250
MH12 1 MH_125_250
MH11 1 MH_125_250
MH10 1 MH_125_250

AFXII GUIDE HOLES

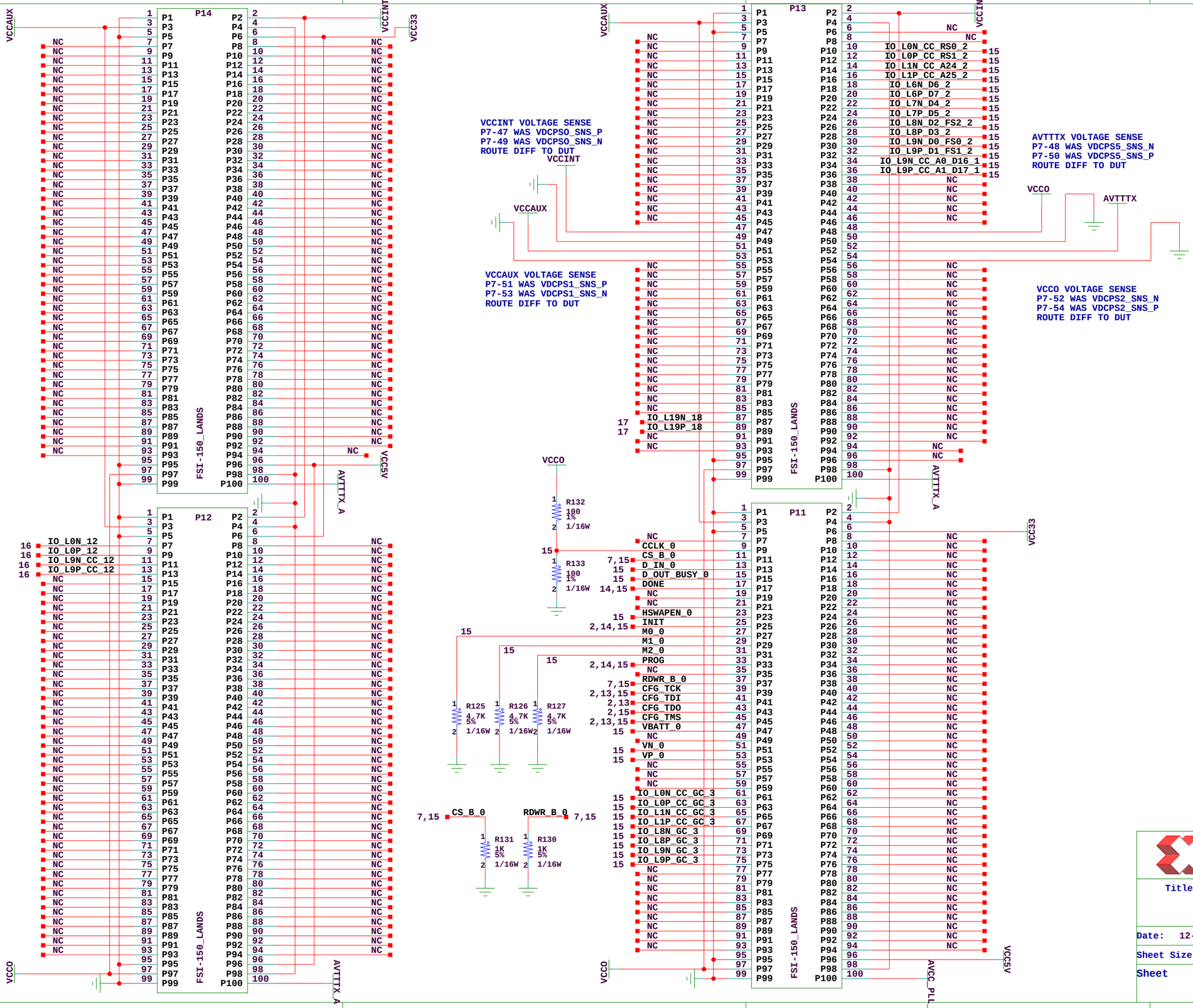
MH1 1 MH_190_250
MH2 1 MH_190_250
MH3 1 MH_190_250

XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
AFX2_CON P15-P18

Date: 12-15-2006_18:48	Ver: B
Sheet Size: B	Rev: 01
Sheet 6 of 20	Drawn By PATRICK J.

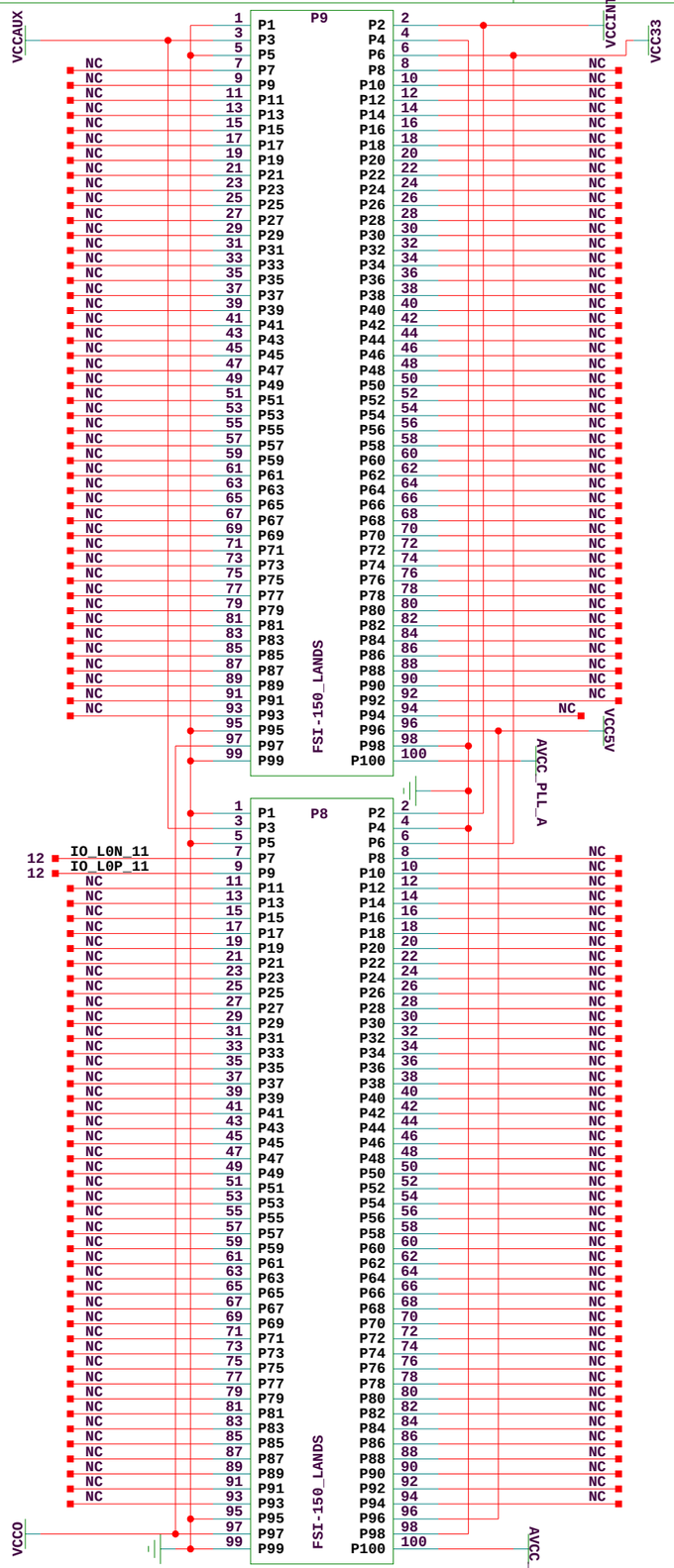


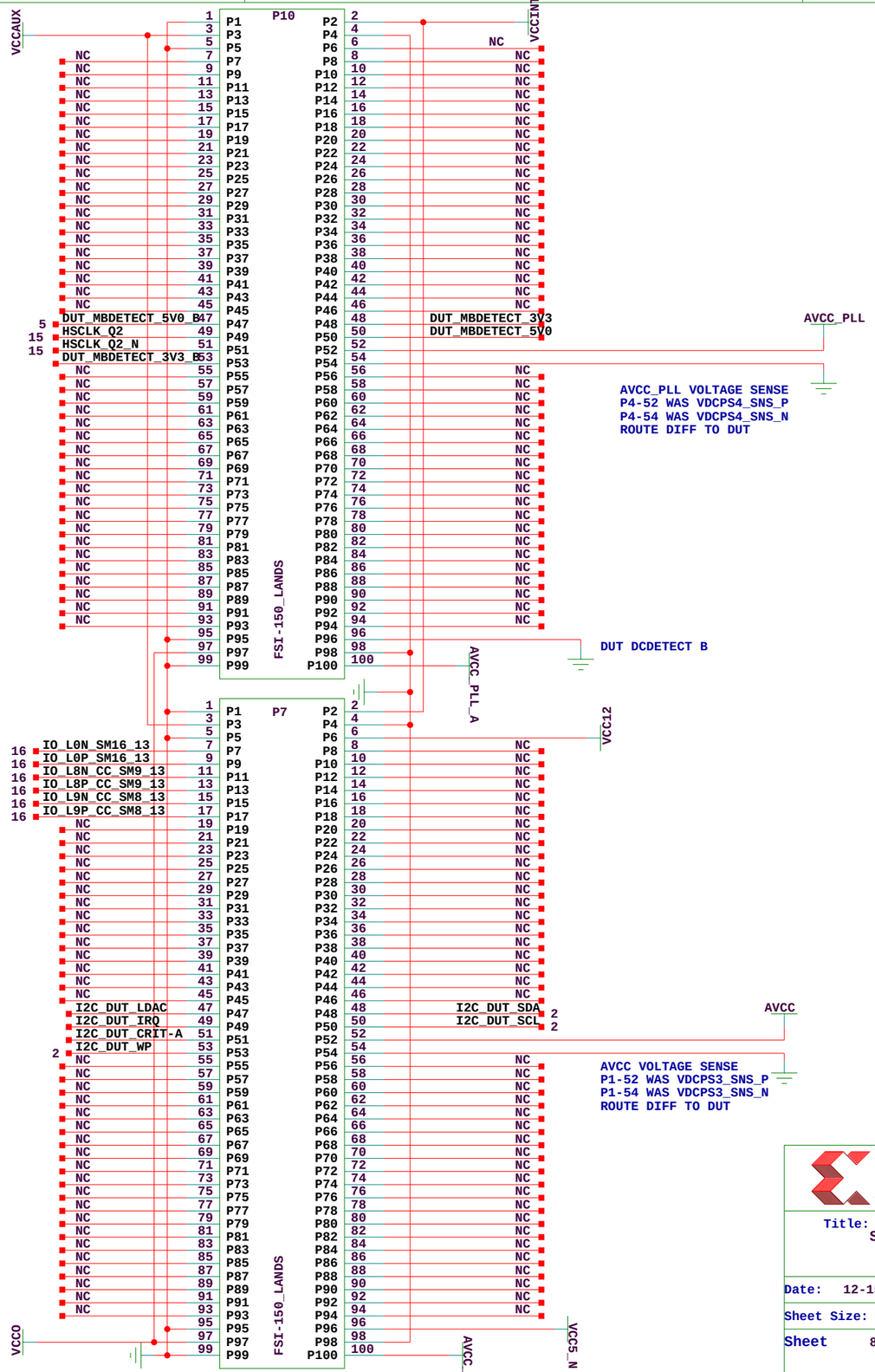
XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
AFX2_CON P11-P14

Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 7 of 20	Drawn By PATRICK J.



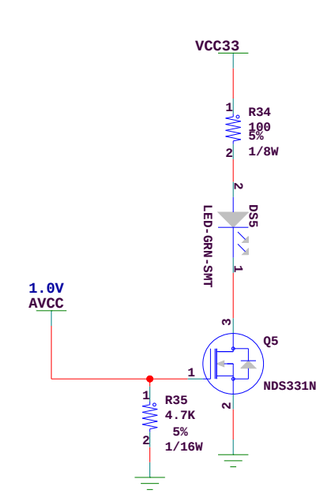


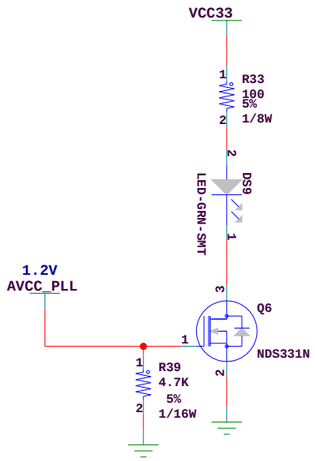
XILINX

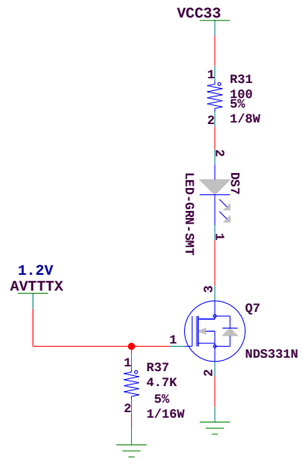
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

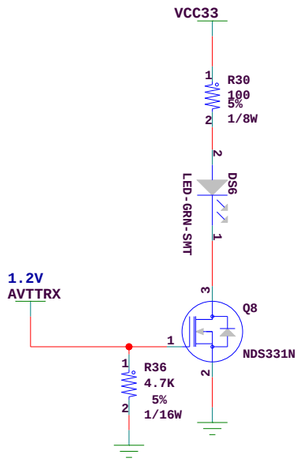
Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
AFX2_CON P7-P10

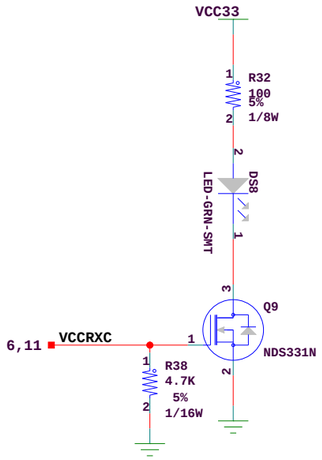
Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 8 of 20	Drawn By PATRICK J.

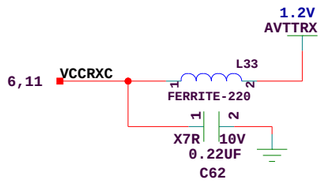


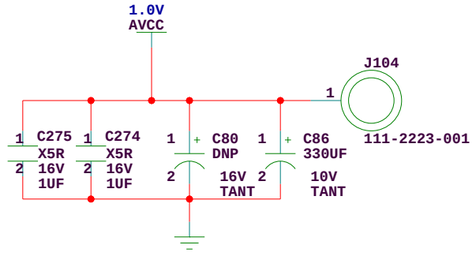


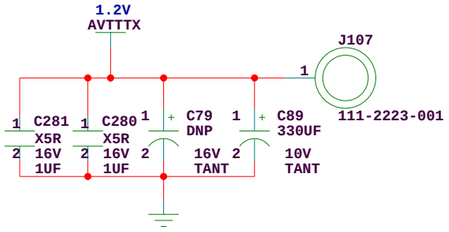


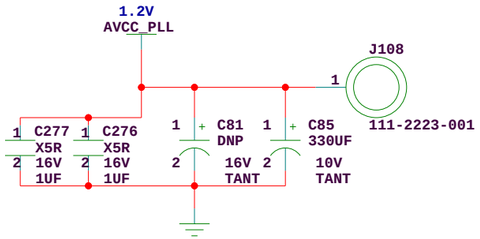


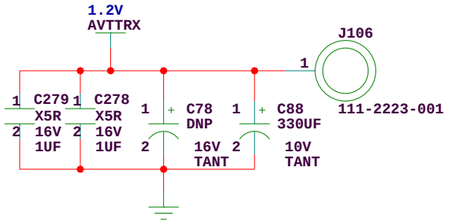




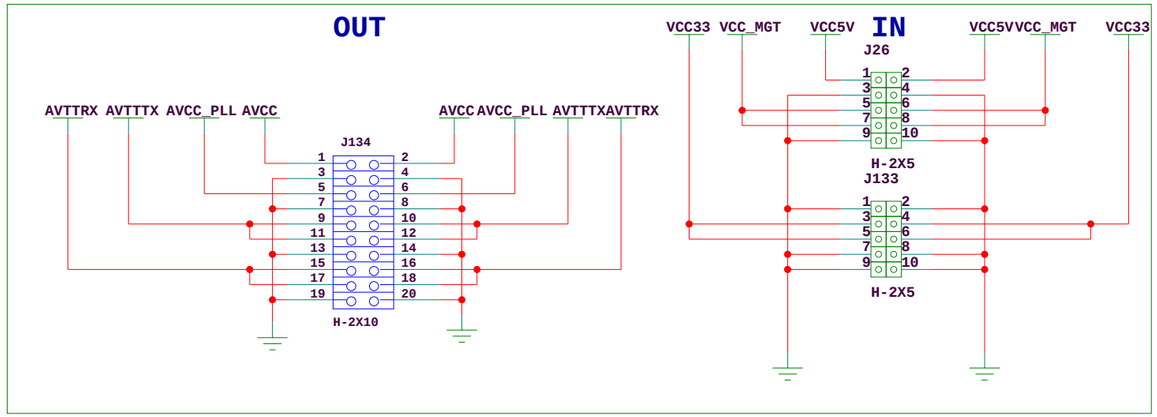




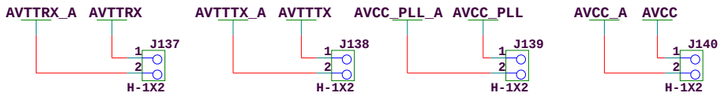




POWER SUPPLY MODULE



ISOLATION JUMPERS



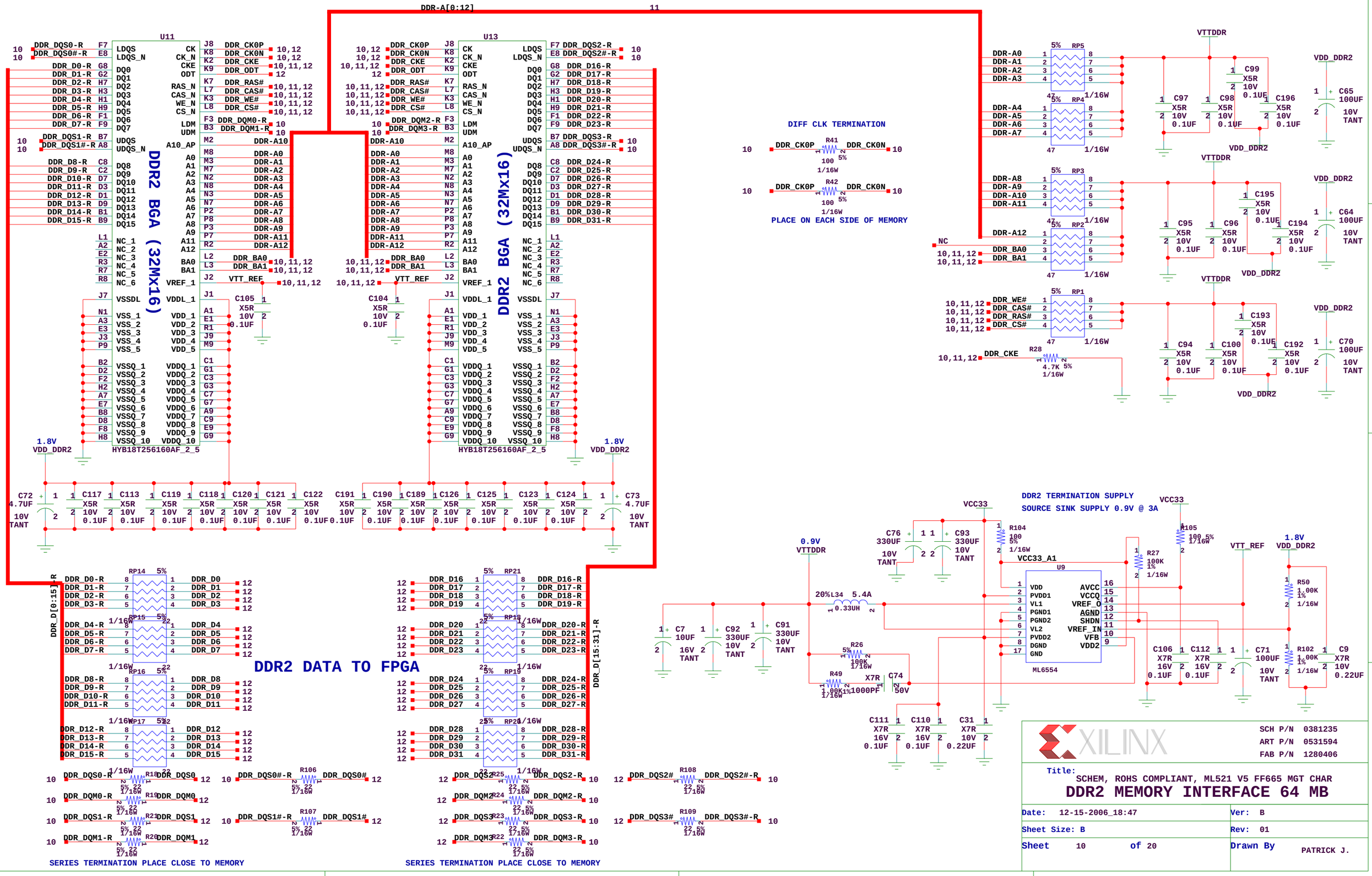
JUMPER ON FOR AFXII DCPS POWER FOR MGT'S
JUMPER OFF FOR ON BOARD REGULATION

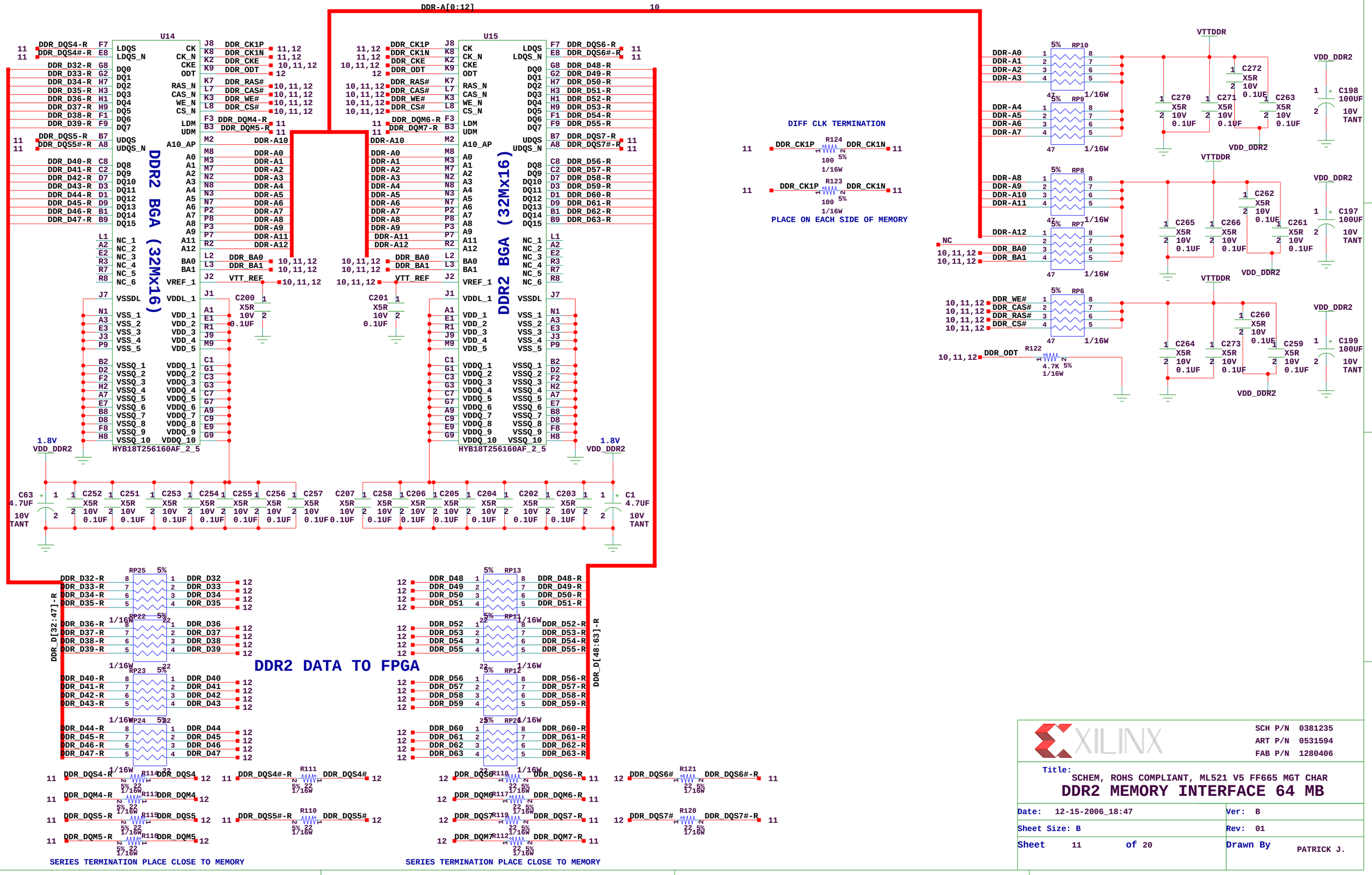
XILINX

SCH_P/N 0381227
ART_P/N 0531585
FAB P/N 1280397

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
MGT'S POWER SUPPLY

Date: 12-15-2006_18:52	Ver: B
Sheet Size: B	Rev: 01
Sheet 9 of 20	Drawn By PATRICK J.


DDR-A[0:12]
U11
U13
DDR2 BGA (32Mx16)
HYB18T256160AF_2_5
DDR_DQS0-R
DDR_DQS0#-R
DDR_DQS1-R
DDR_DQS1#-R
DDR_D0-R
DDR_D1-R
DDR_D2-R
DDR_D3-R
DDR_D4-R
DDR_D5-R
DDR_D6-R
DDR_D7-R
DDR_D8-R
DDR_D9-R
DDR_D10-R
DDR_D11-R
DDR_D12-R
DDR_D13-R
DDR_D14-R
DDR_D15-R
DDR_DQM0-R
DDR_DQM1-R
DDR_CK0P
DDR_CK0N
DDR_CKE
DDR_ODT
DDR_RAS#
DDR_CAS#
DDR_WE#
DDR_CS#
DDR_DQM0-R
DDR_DQM1-R
DDR_DQM2-R
DDR_DQM3-R
DDR_BA0
DDR_BA1
DDR-A10
DDR-A0
DDR-A1
DDR-A2
DDR-A3
DDR-A4
DDR-A5
DDR-A6
DDR-A7
DDR-A8
DDR-A9
DDR-A11
DDR-A12
VTT_REF
DDR_DQS2-R
DDR_DQS2#-R
DDR_DQS3-R
DDR_DQS3#-R
DDR_D16-R
DDR_D17-R
DDR_D18-R
DDR_D19-R
DDR_D20-R
DDR_D21-R
DDR_D22-R
DDR_D23-R
DDR_D24-R
DDR_D25-R
DDR_D26-R
DDR_D27-R
DDR_D28-R
DDR_D29-R
DDR_D30-R
DDR_D31-R
1.8V
VDD_DDR2
DIFF CLK TERMINATION
PLACE ON EACH SIDE OF MEMORY
DDR2 DATA TO FPGA
DDR_D[0:15]-R
DDR_D[15:31]-R
SERIES TERMINATION PLACE CLOSE TO MEMORY
DDR2 TERMINATION SUPPLY
SOURCE SINK SUPPLY 0.9V @ 3A
0.9V
VTTDDR
VCC33
VCC33_A1
ML6554
XILINX
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406
Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
DDR2 MEMORY INTERFACE 64 MB
Date: 12-15-2006_18:47
Ver: B
Sheet Size: B
Rev: 01
Sheet 10 of 20
Drawn By PATRICK J.


DDR-A[0:12]
U14
U15
DDR2 BGA (32Mx16)
HYB18T256160AF_2_5
1.8V
VDD_DDR2
C63 4.7UF 10V TANT
C252 C251 C253 C254 C255 C256 C257 X5R 10V 0.1UF
C207 C258 C206 C205 C204 C202 C203 X5R 10V 0.1UF
C1 4.7UF 10V TANT
DIFF CLK TERMINATION
DDR_CK1P
DDR_CK1N
R124 100 5% 1/16W
R123 100 5% 1/16W
PLACE ON EACH SIDE OF MEMORY
VTTDDR
VDD_DDR2
RP10 RP9 RP8 RP7 RP6 47 5% 1/16W
C270 C271 C263 C272 C262 C265 C266 C261 C260 C264 C273 C259 X5R 10V 0.1UF
C198 C197 C199 100UF 10V TANT
NC
DDR_BA0
DDR_BA1
DDR_WE#
DDR_CAS#
DDR_RAS#
DDR_CS#
DDR_ODT
R122 4.7K 5% 1/16W
DDR_D[32:47]-R
DDR_D[48:63]-R
RP25 RP22 RP23 RP24 RP13 RP11 RP12 RP21 22 5% 1/16W
DDR2 DATA TO FPGA
SERIES TERMINATION PLACE CLOSE TO MEMORY
DDR_DQS4-R
DDR_DQM4-R
DDR_DQS5-R
DDR_DQM5-R
DDR_DQS4#-R
DDR_DQS5#-R
DDR_DQS6-R
DDR_DQM6-R
DDR_DQS7-R
DDR_DQM7-R
DDR_DQS6#-R
DDR_DQS7#-R
R114 R113 R115 R116 R111 R110 R118 R117 R119 R112 R121 R120
XILINX
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406
Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
DDR2 MEMORY INTERFACE 64 MB
Date: 12-15-2006_18:47
Ver: B
Sheet Size: B
Rev: 01
Sheet 11 of 20
Drawn By PATRICK J.

NOTE:

DCI IS NOT REQUIRED

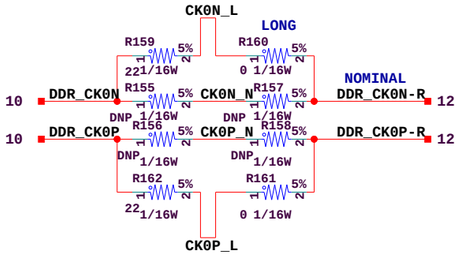
WILL USE EXTERNAL SERIES TERMINATION

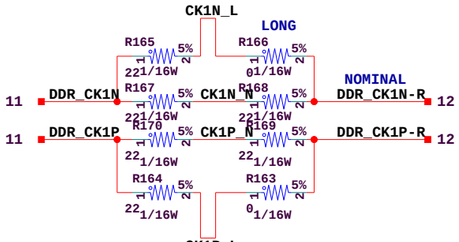
VREF PINS ARE TIED TO VEREF TERMINATION

CHECK TO SEE IF CC PINS ARE CAPABLE

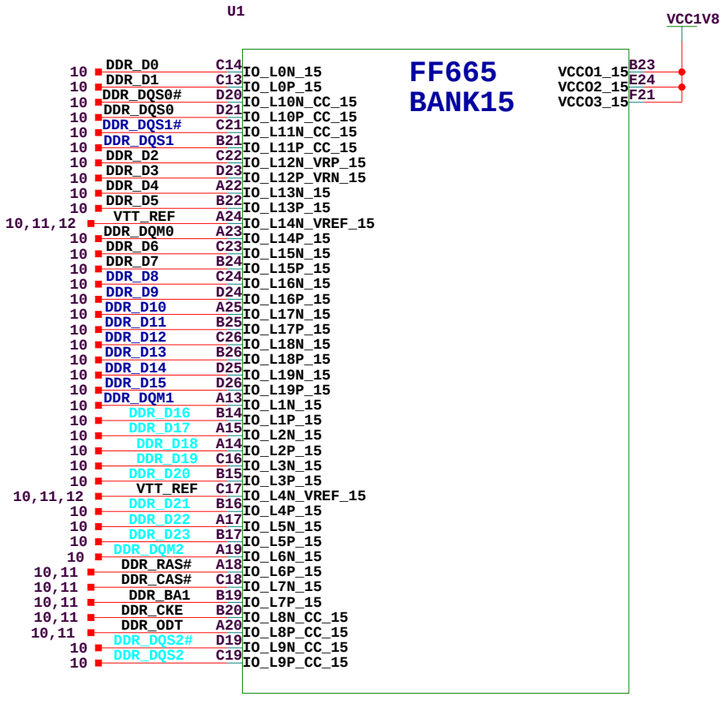
OF DRIVING DIFFERENTIAL CLOCKS

DDR CLK OPTIONS NOMINAL, LONG

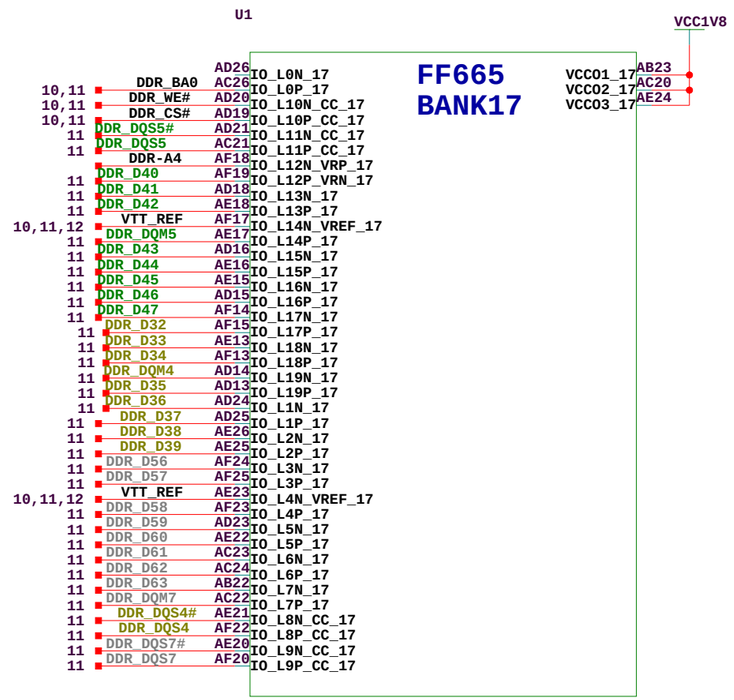




FF665



FF665



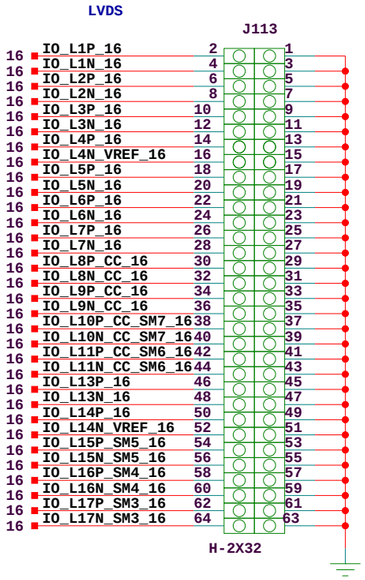
FF665

XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
DDR2 MEMORY INTERFACE FPGA SIDE

Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 12 of 20	Drawn By PATRICK J.

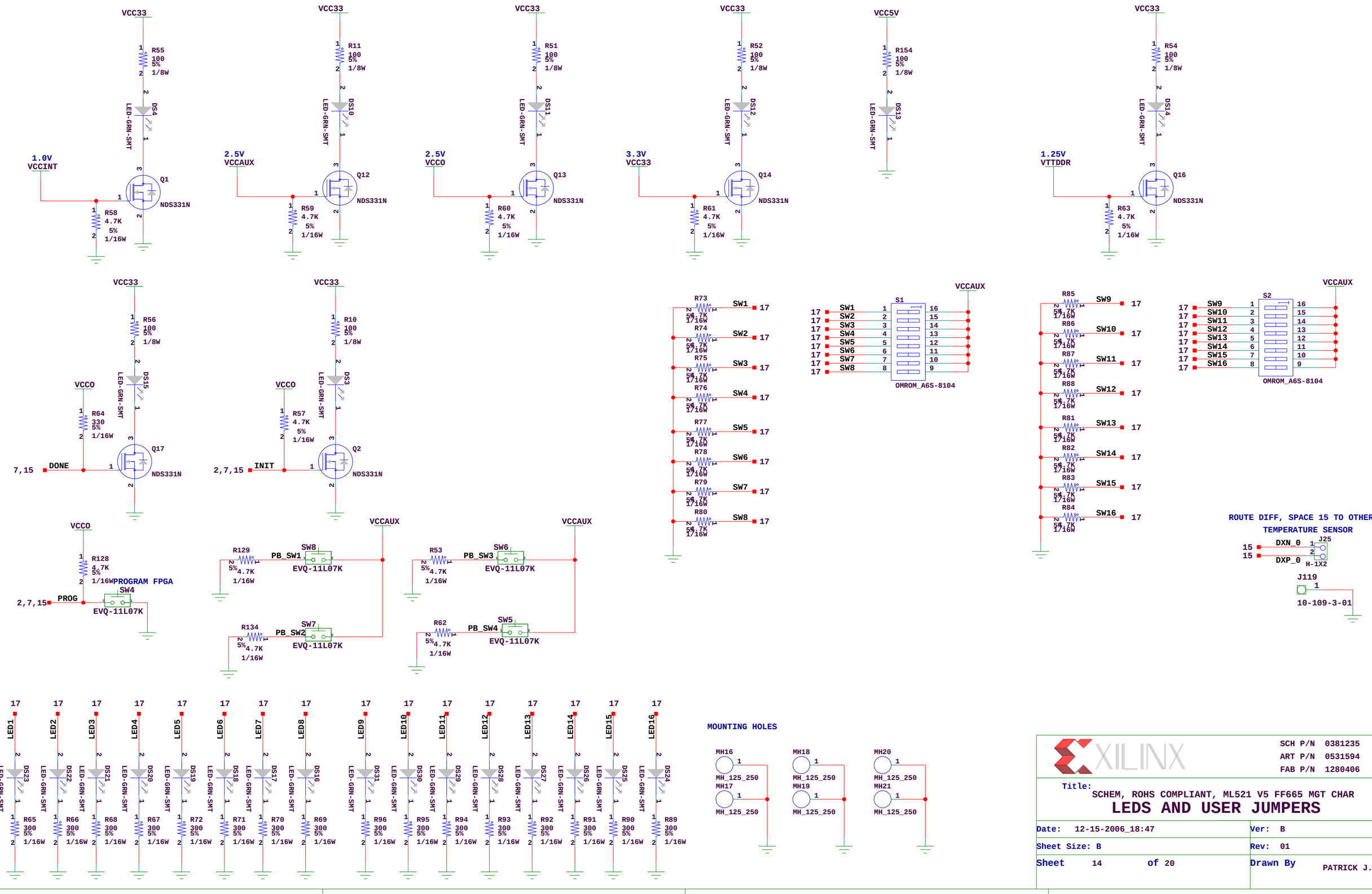


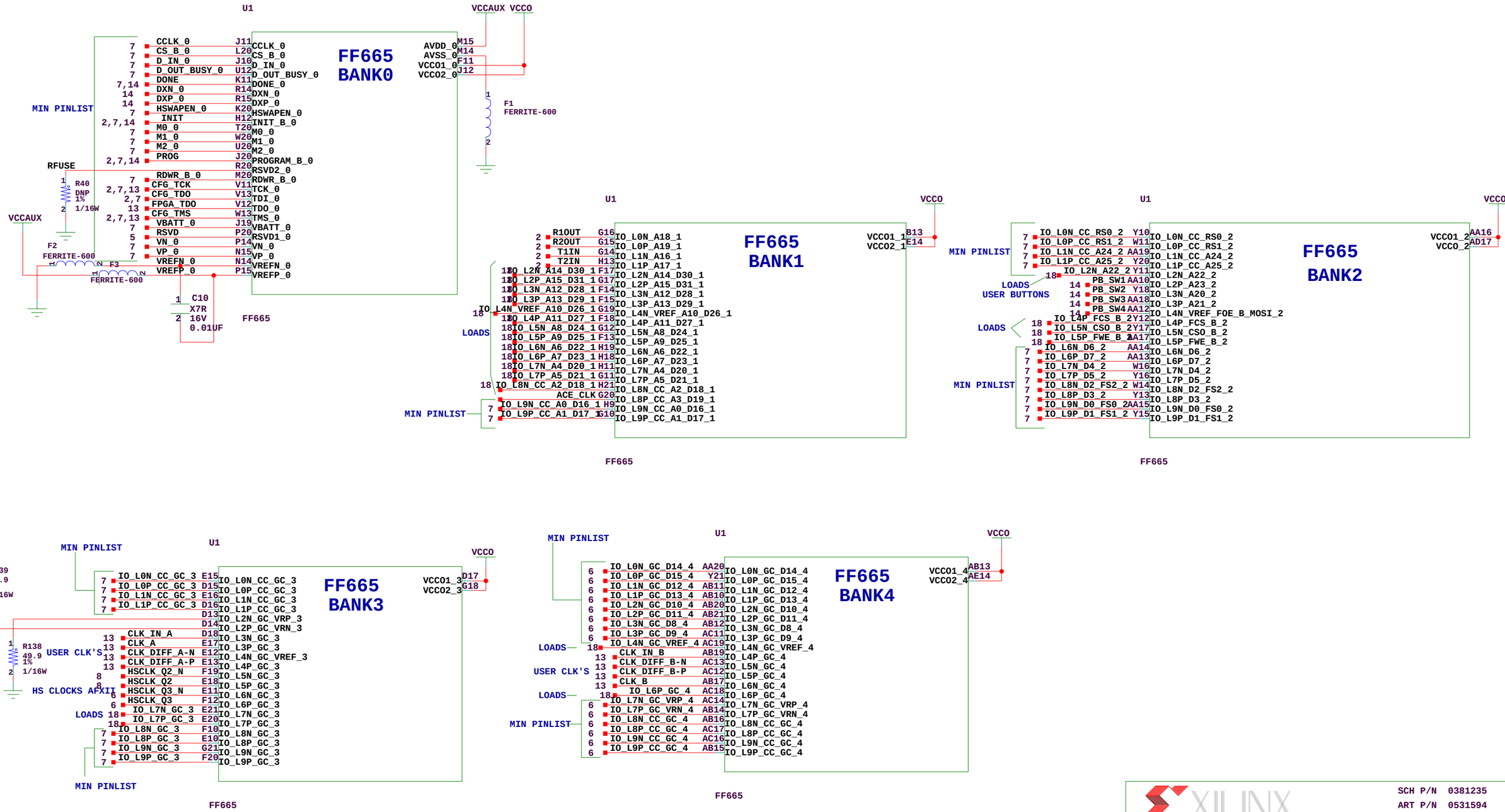
XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
XGI INTERFACE & GLOBAL CLOCKS

Date: 12-22-2006_11:36	Ver: B
Sheet Size: B	Rev: 01
Sheet 13 of 20	Drawn By PATRICK J.


VCC33
R55 100 5% 1/8W
DS4 LED-GRN-SMT
1.0V VCCINT
Q1 NDS331N
R58 4.7K 5% 1/16W
VCC33
R11 100 5% 1/8W
DS10 LED-GRN-SMT
2.5V VCCAUX
Q12 NDS331N
R59 4.7K 5% 1/16W
VCC33
R51 100 5% 1/8W
DS11 LED-GRN-SMT
2.5V VCCO
Q13 NDS331N
R60 4.7K 5% 1/16W
VCC33
R52 100 5% 1/8W
DS12 LED-GRN-SMT
3.3V VCC33
Q14 NDS331N
R61 4.7K 5% 1/16W
VCC5V
R154 100 5% 1/8W
DS13 LED-GRN-SMT
VCC33
R54 100 5% 1/8W
DS14 LED-GRN-SMT
1.25V VTTDDR
Q16 NDS331N
R63 4.7K 5% 1/16W
VCC33
R56 100 5% 1/8W
DS15 LED-GRN-SMT
VCCO
R64 330 5% 1/16W
Q17 NDS331N
7,15 DONE
VCC33
R10 100 5% 1/8W
DS3 LED-GRN-SMT
VCCO
R57 4.7K 5% 1/16W
Q2 NDS331N
2,7,15 INIT
R73 SW1 17
R74 SW2 17
R75 SW3 17
R76 SW4 17
R77 SW5 17
R78 SW6 17
R79 SW7 17
R80 SW8 17
R85 SW9 17
R86 SW10 17
R87 SW11 17
R88 SW12 17
R81 SW13 17
R82 SW14 17
R83 SW15 17
R84 SW16 17
5% 4.7K 1/16W
S1 OMROM_A6S-8104
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8
VCCAUX
S2 OMROM_A6S-8104
SW9 SW10 SW11 SW12 SW13 SW14 SW15 SW16
VCCAUX
VCCO
R128 4.7K 5% 1/16W
PROGRAM FPGA
SW4 EVQ-11L07K
2,7,15 PROG
VCCAUX
R129 PB_SW1 SW8 EVQ-11L07K
R134 PB_SW2 SW7 EVQ-11L07K
VCCAUX
R53 PB_SW3 SW6 EVQ-11L07K
R62 PB_SW4 SW5 EVQ-11L07K
ROUTE DIFF, SPACE 15 TO OTHER
TEMPERATURE SENSOR
J25 DXN_0 DXP_0 H-1X2
15 15
J119 1
10-109-3-01
LED1 LED2 LED3 LED4 LED5 LED6 LED7 LED8
DS23 DS22 DS21 DS20 DS19 DS18 DS17 DS16
R65 R66 R68 R67 R72 R71 R70 R69
300 5% 1/16W
LED9 LED10 LED11 LED12 LED13 LED14 LED15 LED16
DS31 DS30 DS29 DS28 DS27 DS26 DS25 DS24
R96 R95 R94 R93 R92 R91 R90 R89
300 5% 1/16W
MOUNTING HOLES
MH16 MH17 MH18 MH19 MH20 MH21
MH_125_250
XILINX
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406
Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
LEDS AND USER JUMPERS
Date: 12-15-2006_18:47
Ver: B
Sheet Size: B
Rev: 01
Sheet 14 of 20
Drawn By PATRICK J.


U1
FF665 BANK0
VCCAUX VCCO
AVDD_0 M15
AVSS_0 M14
VCCO1_0 F11
VCCO2_0 J12
F1
FERRITE-600
MIN PINLIST
RFUSE
R40
DNP
1%
1/16W
VCCAUX
F2
FERRITE-600
F3
FERRITE-600
C10
X7R
16V
0.01UF
CCLK_0 J11
CS_B_0 L20
D_IN_0 J10
D_OUT_BUSY_0 U12
DONE K11
DXN_0 R14
DXP_0 R15
HSWAPEN_0 K20
INIT H12
M0_0 T20
M1_0 W20
M2_0 U20
PROG J20
RDWR_B_0 M20
CFG_TCK V11
CFG_TDO V13
FPGA_TDO V12
CFG_TMS W13
VBATT_0 J19
RSVD P20
VN_0 P14
VP_0 N15
VREFN_0 N14
VREFP_0 P15
CCLK_0
CS_B_0
D_IN_0
D_OUT_BUSY_0
DONE_0
DXN_0
DXP_0
HSWAPEN_0
INIT_B_0
M0_0
M1_0
M2_0
PROGRAM_B_0
RSVD2_0
RDWR_B_0
TCK_0
TDI_0
TDO_0
TMS_0
VBATT_0
RSVD1_0
VN_0
VP_0
VREFN_0
VREFP_0
U1
FF665 BANK1
VCCO
VCCO1_1 B13
VCCO2_1 E14
R1OUT G16
R2OUT G15
T1IN G14
T2IN H13
IO_L0N_A18_1
IO_L0P_A19_1
IO_L1N_A16_1
IO_L1P_A17_1
IO_L2N_A14_D30_1 F17
IO_L2P_A15_D31_1 G17
IO_L3N_A12_D28_1 F14
IO_L3P_A13_D29_1 F15
IO_L4N_VREF_A10_D26_1 G19
IO_L4P_A11_D27_1 F18
IO_L5N_A8_D24_1 G12
IO_L5P_A9_D25_1 F13
IO_L6N_A6_D22_1 H19
IO_L6P_A7_D23_1 H18
IO_L7N_A4_D20_1 H11
IO_L7P_A5_D21_1 G11
IO_L8N_CC_A2_D18_1 H21
ACE_CLK G20
IO_L9N_CC_A0_D16_1 H9
IO_L9P_CC_A1_D17_1 G10
IO_L0N_A18_1
IO_L0P_A19_1
IO_L1N_A16_1
IO_L1P_A17_1
IO_L2N_A14_D30_1
IO_L2P_A15_D31_1
IO_L3N_A12_D28_1
IO_L3P_A13_D29_1
IO_L4N_VREF_A10_D26_1
IO_L4P_A11_D27_1
IO_L5N_A8_D24_1
IO_L5P_A9_D25_1
IO_L6N_A6_D22_1
IO_L6P_A7_D23_1
IO_L7N_A4_D20_1
IO_L7P_A5_D21_1
IO_L8N_CC_A2_D18_1
IO_L8P_CC_A3_D19_1
IO_L9N_CC_A0_D16_1
IO_L9P_CC_A1_D17_1
LOADS
MIN PINLIST
FF665
U1
FF665 BANK2
VCCO
VCCO1_2 AA16
VCCO_2 AD17
IO_L0N_CC_RS0_2 Y10
IO_L0P_CC_RS1_2 W11
IO_L1N_CC_A24_2 AA19
IO_L1P_CC_A25_2 Y20
IO_L2N_A22_2 Y11
PB_SW1 AA10
PB_SW2 Y18
PB_SW3 AA18
PB_SW4 AA12
IO_L4P_FCS_B_2 Y12
IO_L5N_CSO_B_2 Y17
IO_L5P_FWE_B_2 AA17
IO_L6N_D6_2 AA14
IO_L6P_D7_2 AA13
IO_L7N_D4_2 W16
IO_L7P_D5_2 Y16
IO_L8N_D2_FS2_2 W14
IO_L8P_D3_2 Y13
IO_L9N_D0_FS0_2 AA15
IO_L9P_D1_FS1_2 Y15
IO_L0N_CC_RS0_2
IO_L0P_CC_RS1_2
IO_L1N_CC_A24_2
IO_L1P_CC_A25_2
IO_L2N_A22_2
IO_L2P_A23_2
IO_L3N_A20_2
IO_L3P_A21_2
IO_L4N_VREF_FOE_B_MOSI_2
IO_L4P_FCS_B_2
IO_L5N_CSO_B_2
IO_L5P_FWE_B_2
IO_L6N_D6_2
IO_L6P_D7_2
IO_L7N_D4_2
IO_L7P_D5_2
IO_L8N_D2_FS2_2
IO_L8P_D3_2
IO_L9N_D0_FS0_2
IO_L9P_D1_FS1_2
LOADS
USER BUTTONS
MIN PINLIST
FF665
VCCO
R139
49.9
1%
1/16W
R138
49.9
1%
1/16W
USER CLK'S
HS CLOCKS AFXII
U1
FF665 BANK3
VCCO1_3 D17
VCCO2_3 G18
IO_L0N_CC_GC_3 E15
IO_L0P_CC_GC_3 D15
IO_L1N_CC_GC_3 E16
IO_L1P_CC_GC_3 D16
IO_L2N_GC_VRP_3 D13
IO_L2P_GC_VRN_3 D14
IO_L3N_GC_3 D18
IO_L3P_GC_3 E17
IO_L4N_GC_VREF_3 E12
IO_L4P_GC_3 E13
IO_L5N_GC_3 F19
IO_L5P_GC_3 E18
IO_L6N_GC_3 E11
IO_L6P_GC_3 F12
IO_L7N_GC_3 E21
IO_L7P_GC_3 E20
IO_L8N_GC_3 F10
IO_L8P_GC_3 E10
IO_L9N_GC_3 G21
IO_L9P_GC_3 F20
CLK_IN_A
CLK_A
CLK_DIFF_A-N
CLK_DIFF_A-P
HSCLK_Q2_N
HSCLK_Q2
HSCLK_Q3_N
HSCLK_Q3
IO_L7N_GC_3
IO_L7P_GC_3
LOADS
USER CLK'S
HS CLOCKS AFXII
MIN PINLIST
FF665
U1
FF665 BANK4
VCCO
VCCO1_4 AB13
VCCO2_4 AE14
IO_L0N_GC_D14_4 AA20
IO_L0P_GC_D15_4 Y21
IO_L1N_GC_D12_4 AB11
IO_L1P_GC_D13_4 AB10
IO_L2N_GC_D10_4 AB20
IO_L2P_GC_D11_4 AB21
IO_L3N_GC_D8_4 AB12
IO_L3P_GC_D9_4 AC11
IO_L4N_GC_VREF_4 AC19
IO_L4P_GC_4
IO_L5N_GC_4
IO_L5P_GC_4
IO_L6N_GC_4
IO_L6P_GC_4
IO_L7N_GC_VRP_4 AC14
IO_L7P_GC_VRN_4 AB14
IO_L8N_CC_GC_4 AB16
IO_L8P_CC_GC_4 AC17
IO_L9N_CC_GC_4 AC16
IO_L9P_CC_GC_4 AB15
CLK_IN_B
CLK_DIFF_B-N
CLK_DIFF_B-P
CLK_B
IO_L6P_GC_4
LOADS
USER CLK'S
LOADS
MIN PINLIST
FF665
XILINX
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406
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SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
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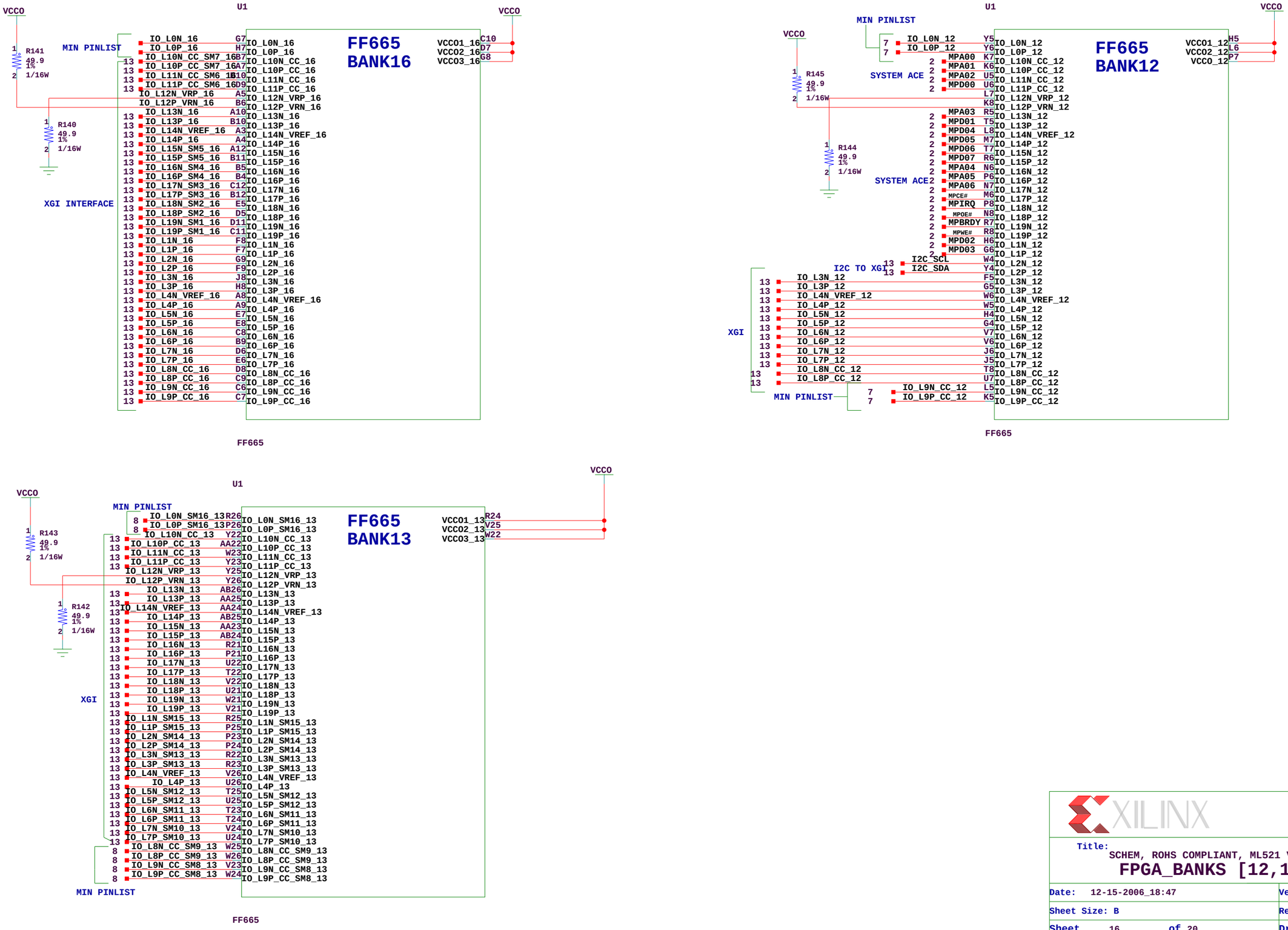
Sheet Size: B
Rev: 01
Sheet 15 of 20
Drawn By PATRICK J.



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Title: SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR

FPGA_BANKS [12,13 & 16]

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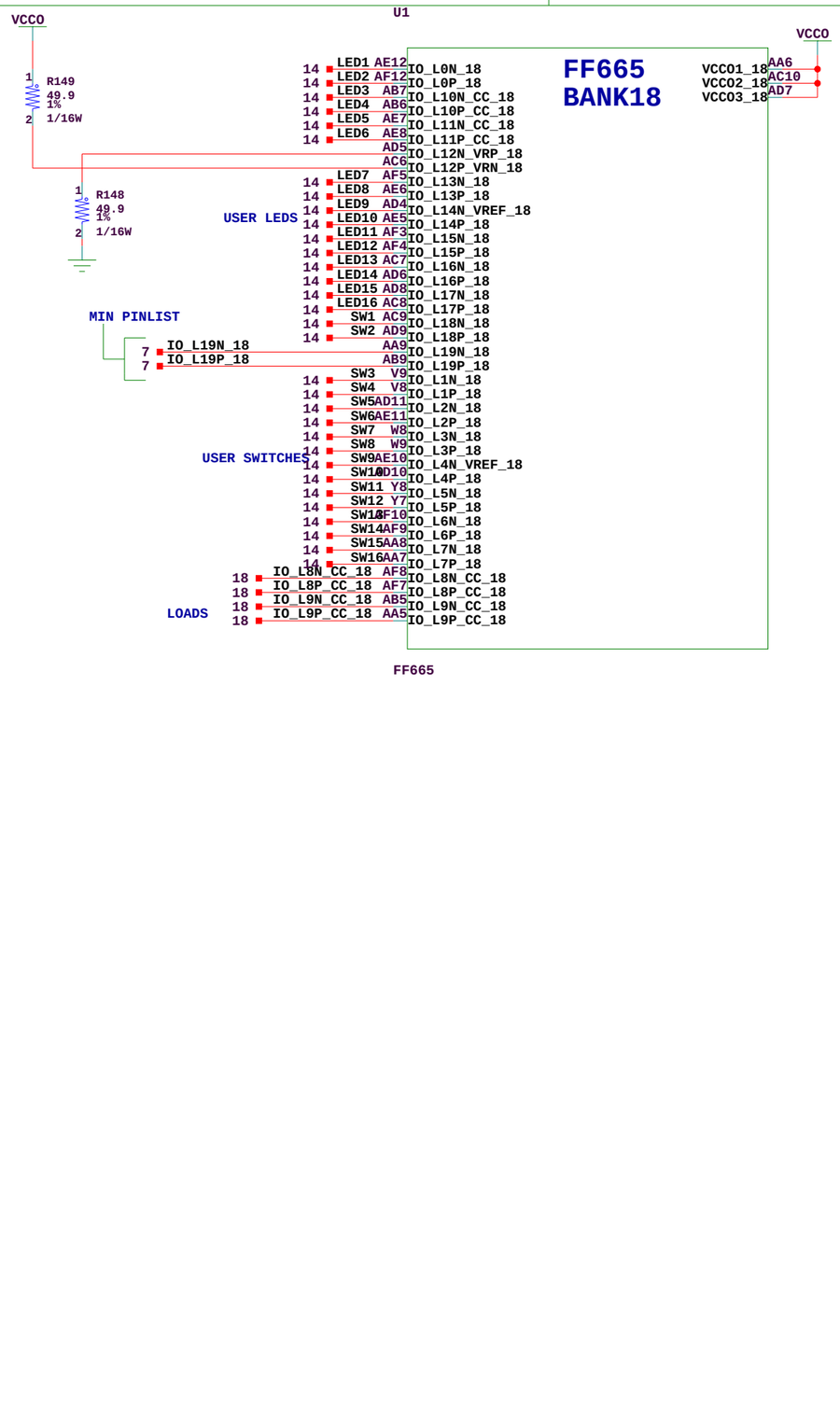

XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
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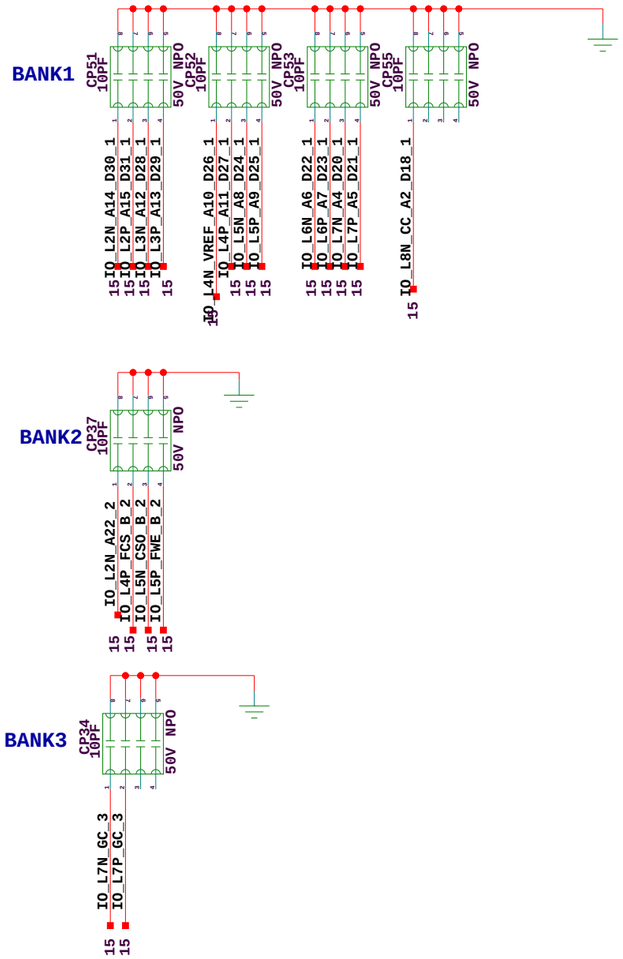
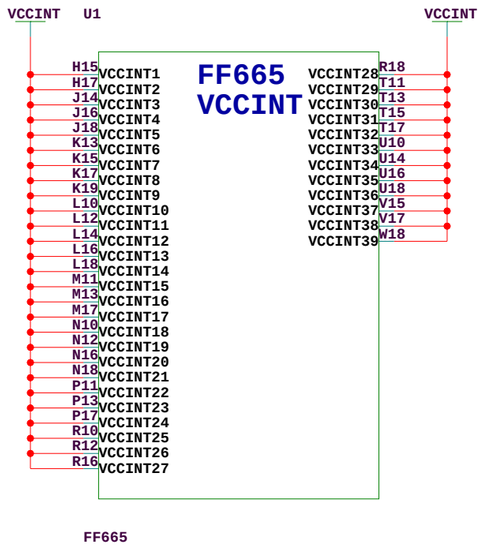


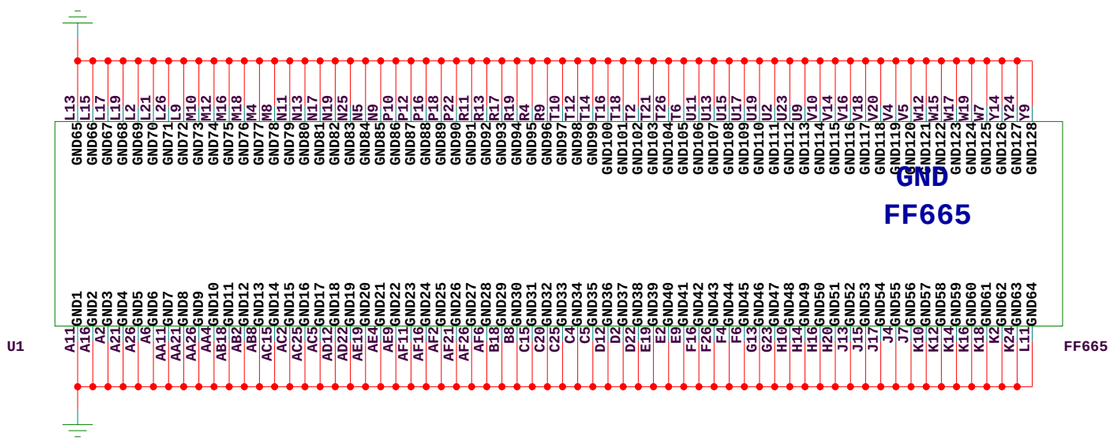
XILINX

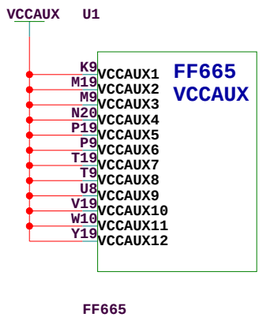
SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
CAPACITIVE LOADS

Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 18 of 20	Drawn By PATRICK J.





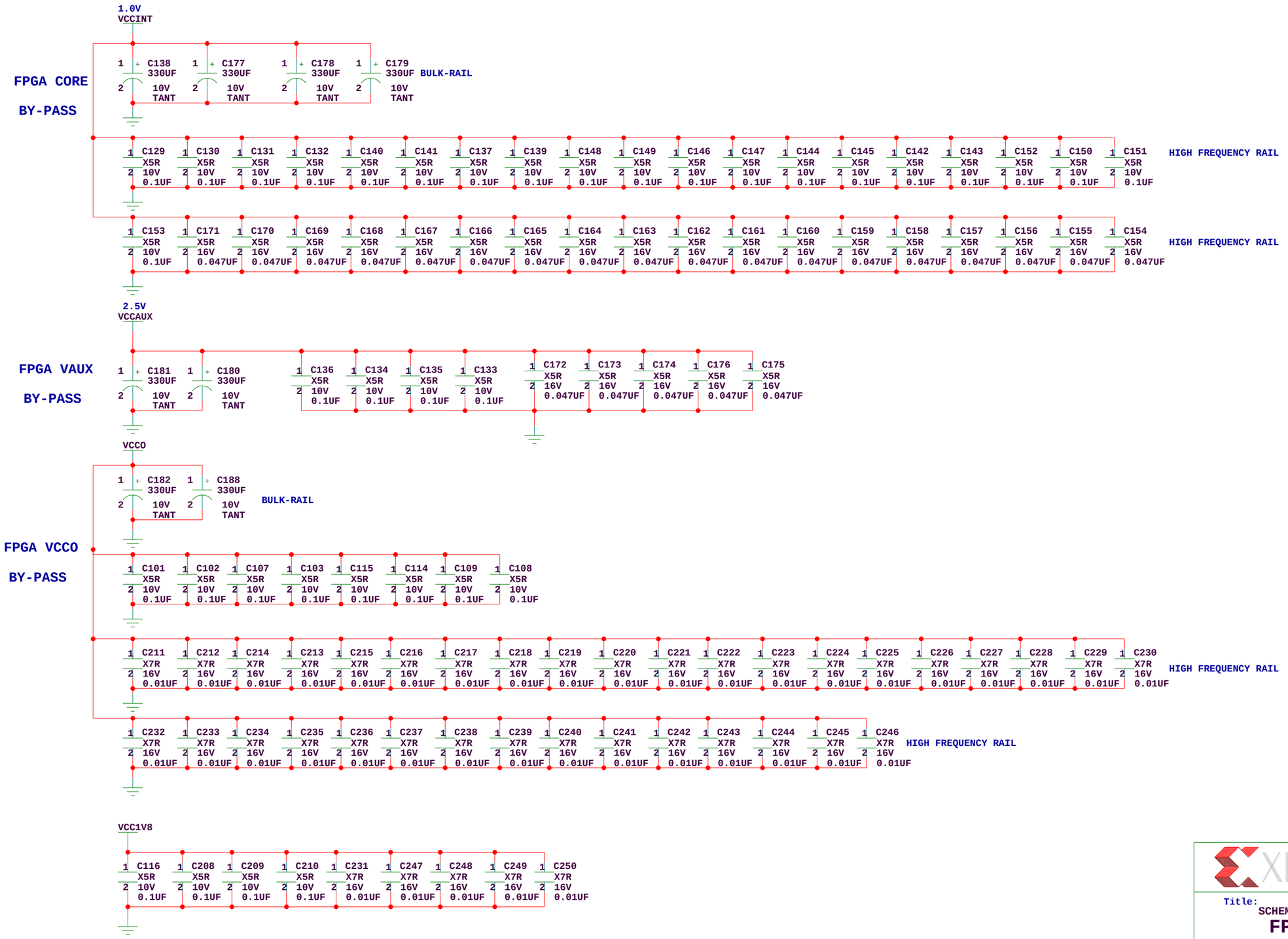


XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR
FPGA PWR/GND

Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 19 of 20	Drawn By PATRICK J.



XILINX

SCH P/N 0381235
ART P/N 0531594
FAB P/N 1280406

Title:
SCHEM, ROHS COMPLIANT, ML521 V5 FF665 MGT CHAR

FPGA_DECOUPLING NETWORK

Date: 12-15-2006_18:47	Ver: B
Sheet Size: B	Rev: 01
Sheet 20 of 20	Drawn By PATRICK J.